Comprehensive 'Atomistic' Simulation of Statistical Variability and Reliability in 14 nm Generation FinFETs

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Abstract*—In this paper, by using comprehensive statistical device simulation methodology, we investigate the effect of Statistical variability and reliability on the state of the art 14nm FinFET technology on important device figures of merit. Important sources of statistical variability have been considered in all simulation of fresh devices and various degradation levels are included in the reliability simulation cases. The interplay between the initial statistical variability introduced by random discrete dopants, line edge roughness and metal gate granularity and the statistical variability introduced by different level of trapped charges resulting from BTI degradation is studied in details. Results related to the time dependent variability and the correlation of key transistor figures of merit are also presented.

Keywords — FinFET; Statistical Variability; Degradation; Charge Confinement;

I. INTRODUCTION

Statistical variability related to the discreetness of charge and matter is of critical importance in advanced CMOS technology. This was one of the main motivations for the introduction of new transistor architectures including FDSOI MOSFETs and FinFETs [1, 2], which tolerate low channel doping, and have the potential to drastically reduce the unfavorable level of mismatch in the traditional bulk MOSFETs dominated by random discrete dopants. The first generation of 22 nm technology CMOS FinFETs, somehow it fell short of this promise delivering a threshold voltage mismatch factor of A_{VT} = 2.08 mV.µm [3] that is a higher value when compared to typical figures reported for FDSOI [4]. However, the second-generation 14 nm CMOS FinFETs have one of the lowest mismatch factor of A_{VT} = 1.07 mV-µm as reported [5]. In this abstract, using the GSS 'atomistic' TCAD simulator GARAND [6], we analyze in detail the statistical variability in 14 nm Intel FinFET technology. It is also well known that some of the benefits that have been achieved as a result of low statistical variability can rapidly be eroded by progressive bias-temperature instability (BTI) degradation. Therefore, we also study the time dependent variability in the 14 nm CMOS FinFETs resulting from the progressive increase

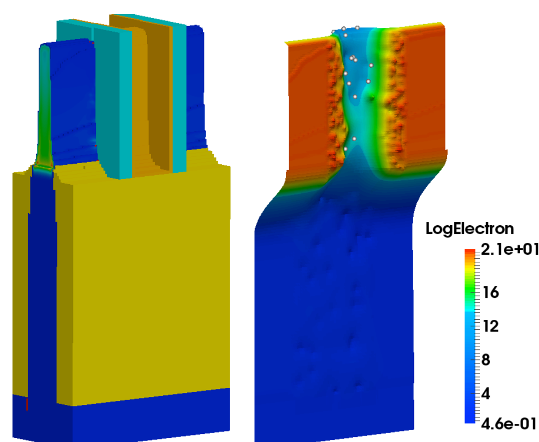

Fig1. A simulated 14nm FinFET device structure (left) and highlighted charge distribution and trap position along the channel direction in one of the extreme devices (right).

in the number of discrete trapped charges and their interaction with the underlying sources of initial 'virgin' statistical variability [5]. We show that the combination of statistical variability and statistical BTI effects result in progressive local variability increase threatening the yield and the reliability of mismatch sensitive system designs [7]

II. SIMULATION APPROACH

The target n-FinFET simulated in this study has a metal gate length L_G of 20 nm, the spacer is 8 nm thick, fin height is 42 nm and fin width is 8 nm [5]. Low channel doping of 1×10^{17} cm^{-3} is adopted for this work. Prior to running the statistical simulation, the device shown in Fig. 1, is reverse engineered and well calibrated against available experimental current voltage characteristics (Fig. 2 and Fig. 3) to reflect the important physical behavior. A current voltage characteristic for an ensemble of 1000 atomistic device that is based on the calibrated deck of device is shown in Fig. 4.

Random Discrete Dopants (RDD), Metal Grain Granularity (MGG), Gate Edge Roughness (LER) and Fin Edge Roughness (FER) are introduced as described in [8] to the calibrated simulation deck with values

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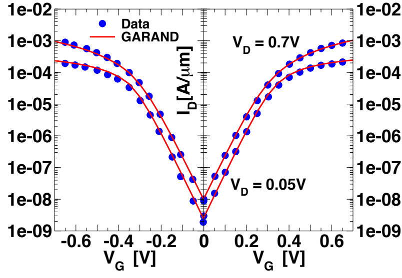

Fig. 2 *Id-Vg*: Garand atomistic device simulator calibrated to experimental data of 14nm FinFET [5]

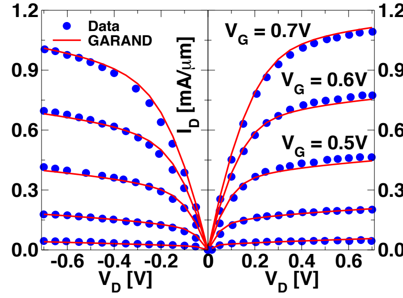

Fig. 3 *Id-Vd* Garand atomistic device simulator calibrated to experimental data of 14nm FinFET [5]

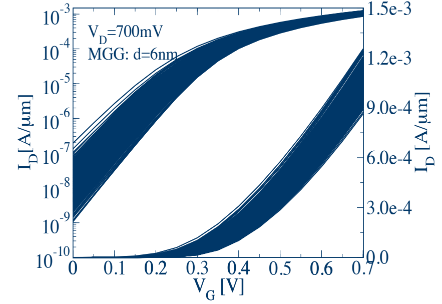

Fig. 4 *Id-Vg* curve of a simulated ensemble of 1000 microscopically different atomistic devices

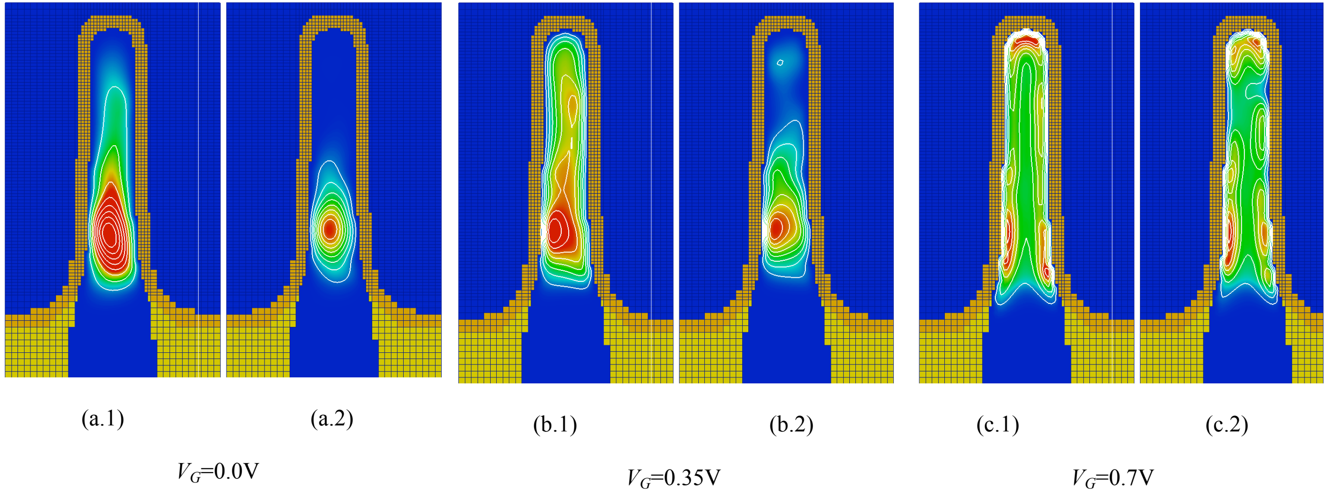

Fig. 5 Current density profile in the fin at low drain bias of 50mV at different gate voltages. The pair of pictures illustrates a profile for fresh 'atomistic' (left) and degraded (right) instances of the same device.

typical to the corresponding technology, individually and in combination, capturing the impact of statistical variability. Five levels of bias temperature instability (BTI) degradation corresponding to trapped charge densities. In this work, the sheet density is varied in the range of $n_T = 1.0\times10^{11}$ cm^{-2} (low level of degradation) to $n_T = 2.0\times10^{12}$ cm^{-2} (high level of degradation). In order to accurately capture the statistical device properties 1000 statistical samples of 'atomistic' devices per scenario have been simulated.

III. Results and Discussions

The current voltage transfer characteristic of an ensemble of 1000 atomistic devices is shown in Fig. 4. Fig. 5 illustrates the combined effect of statistical variability and interface charge trapping on the distribution of current density within a single 'atomistic' transistor. Quantum confinement effects are captured in the simulations using orientation dependent density gradient quantum corrections [8]. The set of pictures in Fig. 5 (a.1, b.1, c.1) illustrate the charge density profile for fresh atomistic devices when all sources of statistical variability are considered, and the charge density profile after degradation with an applied sheet density of interface traps $n_T = 2.0\times10^{12}$ cm^{-2} is shown in Fig. 5 (a.2, b.2, c.2). It is clear that due to statistical variability sources, in this case mainly the discrete random dopants, that maximum and irregular current charge density "islands" are produced in the body of the fin along the channel direction. Figures 6 and Fig. 7 presents the distribution of V_T in fresh 'atomistic' transistors and degraded transistors at both high (V_D=700mV) and low (V_D=50mV) drain biases, with the average grain diameter of 4 and 6 nm respectively. It is apparent that from Fig. 6 and Fig. 7 the introduction of trapped charge introduces significantly more variation in in V_T. Figure 8 shows the distribution of I_{DSAT} for different gate material grain sizes. As can be observed from Fig.8, the variation of average metal grain size has minimal impact on the distribution of on current. However, the introduction of statistical discrete trapped charges significantly degrades the drive current. On average, the degraded devices deliver about

0.26 mA/µm less drain current than the atomistic fresh devices. Figure 9 depicts the cumulative distribution plots for threshold voltage shift that is based on five degradation levels ranging from the lowest value of trap density, $n_T = 1.0\times10^{11}$ cm^{-2}, to the maximum value of trap density, $n_T = 2.0\times10^{12}$ cm^{-2}. The dispersion of threshold voltage shift reaches more than 100 mV for some extreme devices in the case of the highest degradation level of $n_T = 2.0\times10^{12}$ cm^{-2}. Figures 10 and 11 show the dependence of the threshold voltage standard deviation (σV_T) as a function of the level of trapped charge density. σV_T is directly proportional to the average metal grain size as is in the case with degradation level. Depending on the chosen average metal grain size, A_{VT} is in the range of (1.07 - 1.25) mV.µm which is in a good agreement with the value of A_{VT} = 1.07 mV.µm published in [5]. In the case of low drain biases, σV_T increases of about 29% from low to high degradation levels and an increase of about 20% is observed at high drain bias

CONCLUSION

The interplay between the initial statistical variability introduced by RDD, LER, and the statistical variability that is introduced by different levels of trapped charges resulting from BTI degradation has negative impact on important figures of merit of advanced 14nm FinFET technology. Simulation results show that the dispersion of threshold voltage shift reaches more than 100 mV for a statistical ensemble of 1000 devices in the case of devices with highest degradation trap density of n_T=2.0×10^{12} cm^{-2}. Moreover, the introduction of statistical discrete trapped charges significantly degrades the drive current. On average, the degraded devices deliver about 0.26 mA/µm less drain current than the atomistic fresh devices. Depending on the average metal grain diameter of the gate material, the threshold voltage variation factor is in the range of A_{VT} = (1.07 - 1.25) mV.µm which is in a good agreement with the published experimental value of A_{VT} = 1.07 mV.µm. In the case of low drain biases, σV_T increases by about 29% from low to high degradation levels and an increase of about 20% at high drain bias conditions.

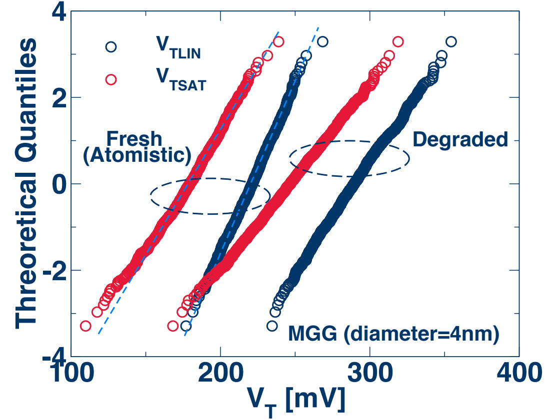

Fig. 6 V_T shift as a result of degradation with a given average metal grain diameter of 4 nm.

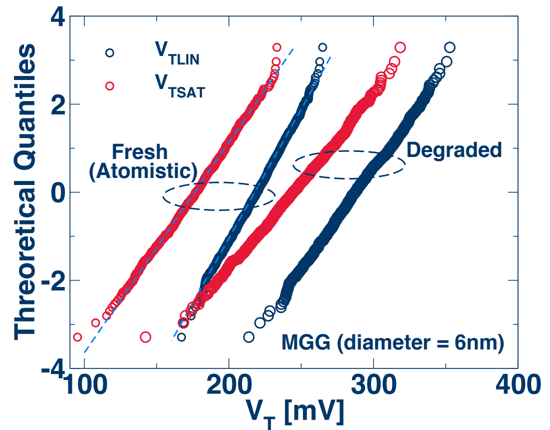

Fig.7 V_T shift as a result of degradation with a given average metal grain diameter of 6 nm.

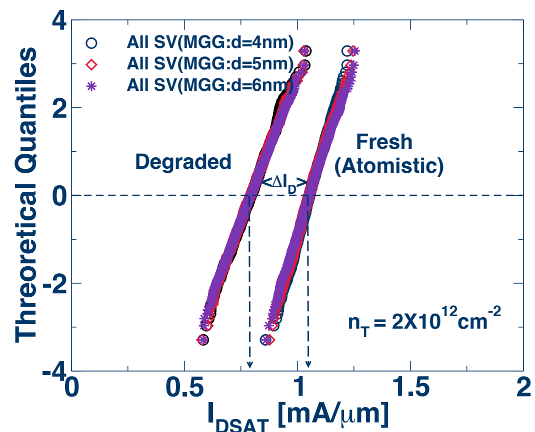

Fig.8 I_{DSAT} distribution considering all sources of variability (ALL SV) and different grain diameters of 4,5 and 6 nm. The degradation level of charge sheet density is n_T=2×10^{12}

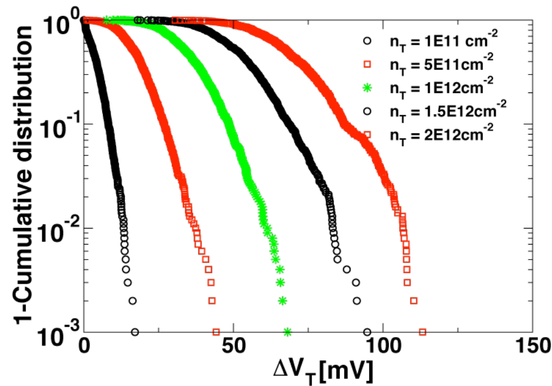

Fig. 9 Cumulative distribution plot for ΔV_T for five degradation levels. The dispersion reaches more than 100 mV in the case of the highest degradation level of 2x10^{12} cm^{-3}

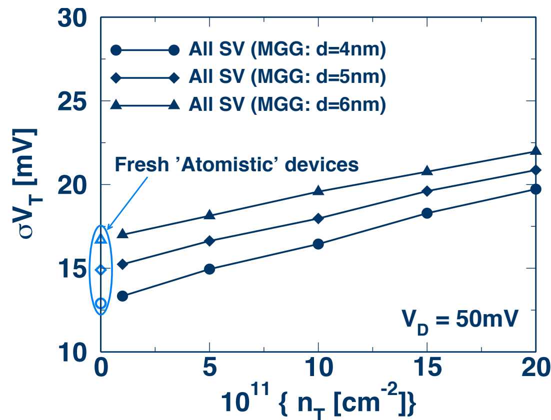

Fig. 10 Threshold voltage variation as a function of degradation levels. All sources of variability are considered with different values of MGG grain sizes at V_D = 50 mV

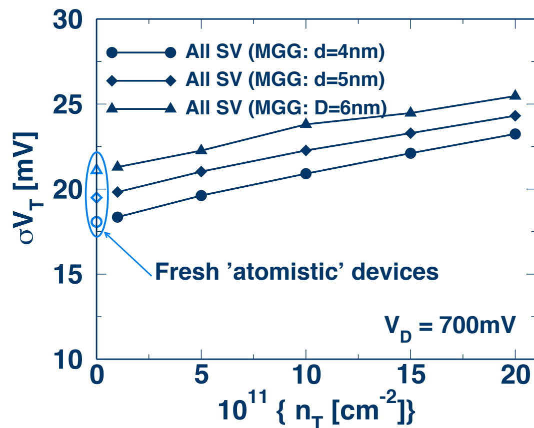

Fig.11 Threshold voltage variation as a function of degradation levels. All sources of variability are considered with different values of MGG grain sizes at V_D = 700 mV.

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