3D Electro-Thermal Simulations of Bulk FinFETs with Statistical Variations

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***Abstract*—This paper investigates the impact of self-heating on the statistical variability of bulk FinFETs. 3D electro-thermal simulations have been performed using the GSS statistical-variability-aware device simulator GARAND, recently enhanced with a thermal simulation module. A bulk FinFET, designed to meet the specifications for the 14/16nm CMOS technology generation, is used as a test bed, taking into account the combined effects of gate edge roughness, fin edge roughness and metal gate granularity. The statistical distribution of key figures of merit, especially the on-current, under the influence of thermal effects, is analysed.**

Keywords—FinFETs; self-heating effects; electrothermal simulations; statistical variability

I. INTRODUCTION

The introduction of CMOS FinFETs represents a radical shift in the semiconductor industry. The 3D FinFET architecture (a schematic of a bulk FinFET is shown in Fig. 1) excels in the control of short-channel effects and delivers superior scalability. However, in terms of thermal behaviour and reliability the FinFET paradigm introduces challenges, focusing the attention on modelling and analysis of self-heating effects in FinFETs [1-3].

Recently the GSS 'atomistic' simulator GARAND [4] has been enhanced with advanced 3D electro-thermal simulation capability, which has been demonstrated in FinFET simulation examples [5-6]. In this work, we further investigate the impact of self-heating on statistical variability of bulk FinFETs using 3D coupled electro-thermal 'atomistic' simulations. In section II, the methodology for the coupled electro-thermal simulation, as well as the modelling of statistical variations are presented. In Section III, the bulk FinFET used as a test bed in this work is introduced. In Section IV, the simulation results for the bulk FinFET are presented, including the lattice temperature profile due to self-heating effects and the impact of self-heating on the statistical variability is analysed, with a focus on the on-current.

The research leading to these results has received funding from the European Union Seventh Framework Programme (FP7/2007 – 2013) under grant agreement no. 318458 SUPERTHEME.

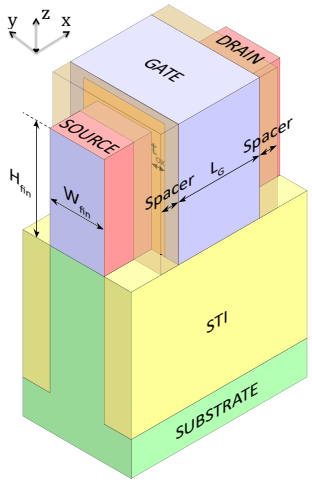

Fig. 1. Schematic of a bulk FinFET.

II. 3D ELECTRO-THERMAL SIMULATION

We have developed an efficient thermal simulation module, which is implemented in the GSS 'atomistic' simulator GARAND. The coupled system of equations describing the heat generation and flow, potential distribution and current density is solved self-consistently [5]. Furthermore, we employ a new, approximate formula for the calculation of the thermal conductivity in the confined Fin region, the thickness / width of which is of the order of 10 nm, to take account of the significant reduction of the thermal conductivity compared with bulk transistors due to phonon-boundary scattering. This model of thermal conductivity extends the previous 1D formula [7] to 2D applications [5]. Different mobility models can be used in the electro-thermal simulations. Here we employ the Masetti model for doping-dependent low-field mobility, enhanced Lombardi model for perpendicular field dependent mobility and Caughey-Thomas model for lateral field-dependent mobility [8-10]. Temperature dependence is included in the mobility models and saturation velocity. External thermal resistances can be employed to account for heat dissipation into interconnects, the wafer, the case, etc. while the electrical characteristics of the device are calculated in a simulation domain restricted to the active device region in order to maximize computational efficiency.

978-1-4673-7860-4/15/$31.00 ©2015 IEEE

The framework of the GSS statistical-variability-aware simulator GARAND provides the natural integration of the thermal simulation with the statistical variability simulation. LER can be modelled through randomly generated lines assuming it follows a Gaussian autocorrelation function [11]. LER is characterised by two parameters: the root mean square (rms) amplitude of the line, Δ, and the longitudinal correlation length, Λ. For FinFETs, both gate edge roughness (GER) and fin edge roughness (FER) can be included in the simulations. In the modelling of metal gate granularity (MGG), we consider that metal grains with different crystallographic orientations have different work functions at the metal/oxide interface. MGG [12] can be modelled through the generation of a random 3D grain pattern with a given average grain diameter, where each grain is statistically assigned a work function based on the occurrence probability and number of different grains specified by the user. GARAND, enhanced with the new electro-thermal capability, can be used for comprehensive investigations of self-heating effects in 3D nanoscale devices with statistical variations.

III. Bulk FinFET Example

In this paper, a bulk FinFET designed to meet the specifications for the 14/16nm CMOS technology generation is used as a test bed. The material and structure of the transistor is shown in Fig. 2. It features a high-k metal gate, nitride spacers, silicon fin and shallow trench isolation (STI). Its channel length is assumed conservatively to be 25 nm, while the fin width and the fin height are 12nm and 30nm respectively. Spacers of 6nm are located on both sides of the gate, and the depth of the STI is 30nm. The equivalent oxide thickness of the gate oxide is 0.8nm. The supply voltage is 0.9 Volts. The source and drain regions are highly doped with peak concentration of 1×10^{20} cm^{-3}. The channel doping is 1×10^{15} cm^{-3} and a 5×10^{18} cm^{-3} channel stop implant is introduced below the channel.

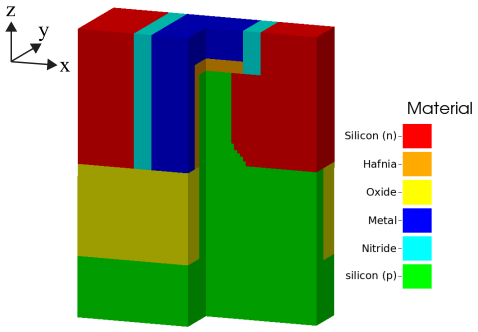

Fig. 2. Material and structure of the bulk FinFET electrical simulation domain, cutting out a quarter to show half of the middle plane.

IV. Impact of Self-Heating on Statistical Variability

3D coupled electro-thermal simulations have been performed on the test-bed FinFET, where a new formula for the thermal conductivity of the fin region is used in the electro-thermal module and external thermal resistances are included. The resultant lattice temperature profile at Vg=Vd=0.9V for the nominal device is illustrated in Fig. 3 (a). The simulations show that a significant hot spot is produced near the drain, with peak lattice temperature exceeding 430K, also indicating strong temperature gradients in the region. The maximum temperature in the fin, varying with gate voltage and drain voltage, is shown in Fig.3 (b) as a response surface. As expected the lattice temperature increases with the increase of drain voltage and gate voltage. For comparison, simulations without self-heating are also performed at uniform room temperature of 300 K, at the maximum temperature (433.1K) obtained in the entire electro-thermal simulations, and at temperature defined by the maximum temperature at each individual bias condition obtained from the electro-thermal simulations ("step max T"). The corresponding Id-Vg curves are illustrated in Fig. 4, showing the impact of self-heating on the device characteristics.

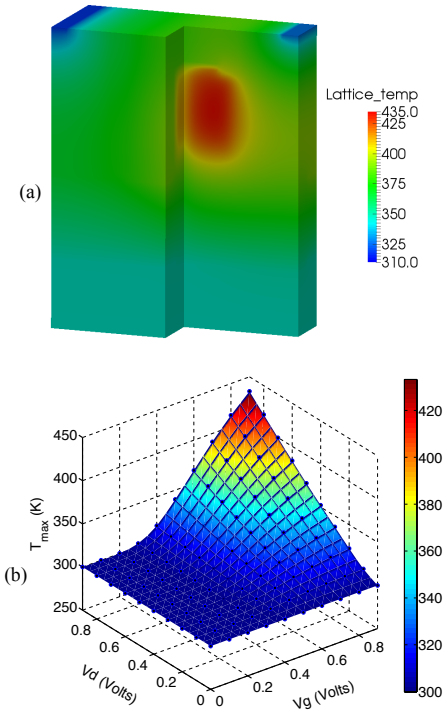

Fig. 3. (a) Lattice temperature profile at Vg=Vd=0.9V (cutting out a quarter to show half of the middle plane); (b) maximum temperature in the fin at different drain and gate bias.

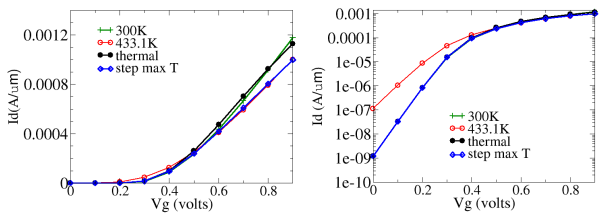

Fig. 4. Simulated Id-Vg characteristics at high drain voltage for the bulk FinFET (a) on linear scale (b) on log scale.

Statistical 'atomistic' GARAND simulations have been performed for an ensemble of 400 statistically different devices, considering the combined impact of statistical sources of GER (3Δ=2 nm, Λ=30nm), FER (3Δ=2 nm, Λ=30nm) and MGG. For MGG, a TiN metal gate with an average grain diameter ∅=5nm and two major grain orientations which lead to a work-function (WF) difference of 0.2 V is assumed, and the probability for the lower and higher WF is 0.4 and 0.6 respectively. The simulation results for one instance from the statistical ensemble are illustrated in Fig. 5, illustrating the lattice temperature distribution, Joule heat, and potential distribution from the electro-thermal simulation. The hot spot and temperature gradient in the fin channel are clearly shown. The Id-Vg characteristics at high drain voltage (Vd=0.9V) are shown in Fig.6 (a), from which the figures of merit (FOM) are extracted. The distribution of on-current is shown in Fig. 6 (b).

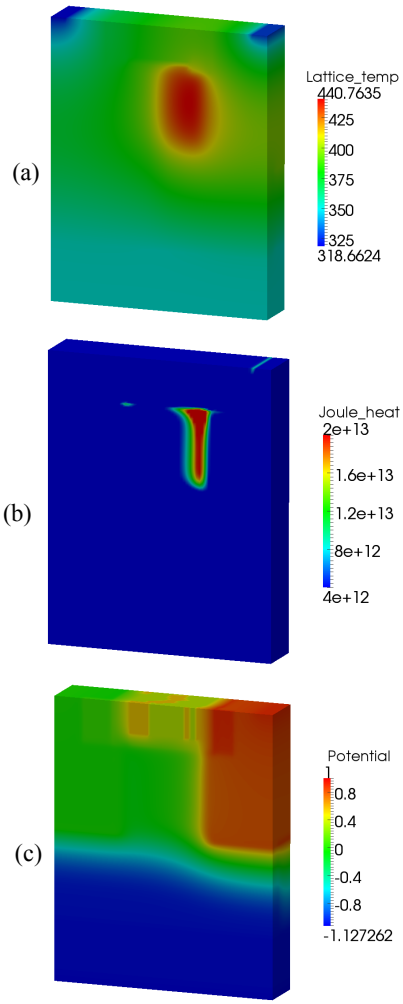

Fig. 5. Simulated lattice temperature distribution, Joule heat, and potential distribution for one instance from the statistical ensemble of 400 for the bulk FinFET (cutting the fin in half to show the middle plane).

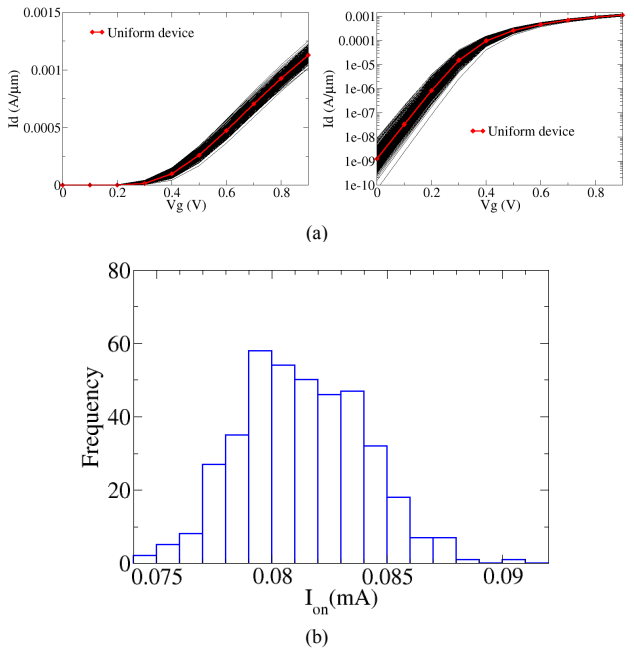

Fig. 6. (a) Id-Vg characteristics at high drain voltage (Vd=0.9V) for a statistical ensemble of 400 for the bulk FinFET example and (b) the distribution of on-current.

For comparison, FOM are also extracted from the simulation results at uniform room temperature of 300 K, at the maximum temperature (433.1K) obtained in the entire electro-thermal simulations, and at "step max T" case as defined previously. The Q-Q plots of the statistical distributions of on-current and threshold voltage for the four cases are given in Fig.7. Comparing the electro-thermal simulations with the uniform room temperature simulation, the self-heating only affects the distribution of the on-current (I_{on}) in the case of DC operation, while has negligible impact on the other FOM which are related to the subthreshold. The mean value and standard deviation of the distribution of the on-current for this bulk FinFET example are summarised in Table 1. The electro-thermal simulation results show that the average on-current has been reduced because of the self-heating effects, while at the same time the standard deviation has also been reduced (by 0.7 μA). In other words, self-heating significantly reduces the I_{on} variability, due to negative feedback. On the other hand, simulations with a uniform high temperature predict a larger reduction in on-current with comparable standard deviation. Overall they result an overestimation of the statistical variability from the viewpoint of the normalized standard deviation. This is because the strong temperature gradients in the fin channel region, which affect the local current density through the additional part related to thermal gradient, can not be taken into account in the uniform temperature simulations, unlike in the 3D electro-thermal simulations.

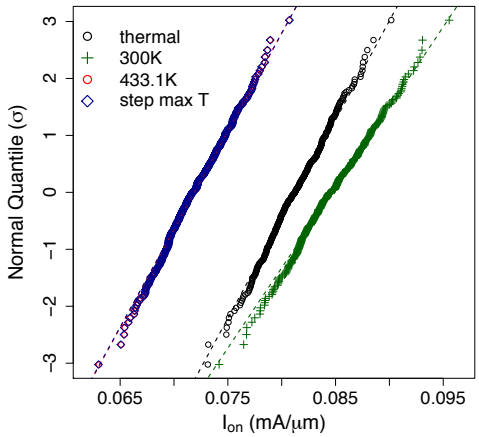

Fig. 7. (a) QQ plots for the distributions of on-current and (b) threshold voltage, clearly showing deviation from the standard Gaussian distribution especially above 1.5 sigma.

TABLE I. THE MEAN AND STANDARD DEVIATION FOR THE ON-CURRENT DISTRIBUTION, EXTRACTED FORM THE STATISTICAL SIMULATION RESULTS

	On-current		
	Mean (mA)	***Std. Dev. (mA)***	***Std. Dev. (%)***
Electro-thermal simulations	0.0813	0.0027	3.3
Uniform 300K	0.0847	0.0034	4.0
Uniform temperature at 433.1K	0.0719	0.0028	3.9
Step max T	0.0719	0.0028	3.9

V. CONCLUSIONS

3D electro-thermal simulations have been performed on a bulk FinFET example with statistical variations, using the recently developed thermal simulation module integrated in GSS statistical-variability-aware device simulator GARAND. Combined sources of statistical variation including GER, FER and MGG are considered in the simulation. The impact of self-heating on the statistical variability in the bulk FinFET has been investigated, with comparison of results between the electro-thermal simulation and simulations at different uniform temperatures. Our simulations indicate that the self-heating has a strong impact on reducing the on-current variability but does not significantly affect the threshold voltage, subthreshold slope and off-current variability. The results also show a uniform increase in temperature within the whole device region will give misleading information on the trends of I_{on} variation, and the temperature gradient in the channel needs to be included when considering the full picture of self-heating effects.

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