New Perspective on Lifetime Prediction Approach for BTI and HCI Stressed Device and Its Impact on Circuit Lifetime

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***Abstract*— Device and circuit lifetime is investigated for poly silicon gated MOSFET. New findings are: (1) More than 1 order lifetime is increased by quantifying the influence of poly depletion effect (PDE) and accumulated trap charge effect (ATCE). (2) We demonstrate that conventional lifetime model produce an incorrect and reverse lifetime result for each degradation data measured by fast and slow method. (3) We evaluate the impact on circuit parameter, propagation delay time (t_{PD}), degradation in the light of new findings.**

Keywords—lifetime prediction, poly depletion, trapping charge effect, NBTI, HCI, circuit lifetime prediction

I. INTRODUCTION

Recently device lifetime target, generally defined as conservative, is hard to meet with aggressive and continuous device scaling. In order to decide lifetime specification, it is important to analyze device lifetime and also its impact on circuit because lifetime target have to guarantee successful chip operation during the specific period. However, there are many limitations to get accurate lifetime. A lifetime is typically obtained by extrapolation from high stress voltage (V_{GST}) to nominal operation voltage (V_{GOP}). Measurements possibly affected by subsidiary effects, i.e., poly depletion and trapped charge during degradation because degradation test is carried out at out of nominal device operation range, usually high voltage and temperature. From the limitations, questions on the validation of the prediction model have risen [1, 2]. On the other hand, physical origin of NBTI model is still under debate. Usual approaches for lifetime modeling are modifying or adding equations into degradation model to explain its complicated behavior [3, 4].

In this paper, we focus on quantitative approach to evaluate subsidiary effects which influence oxide electrical field (E_{ox}) during degradation. We investigated the Poly-Si depletion [5], the effect of accumulated charge by trap generation and trapping/de-trapping behavior of dynamic NBTI [4]. Based on device level degradation modeling, circuit parameter degradation also evaluated. Finally, we delivered the conclusion that these effects should be careful considered to estimate accurate device and circuit lifetime.

II. EXPERIMENTAL SET UP AND DEGRDATION MODEL

A. Experimental Setup

The polycrystalline-silicon gate NMOS and PMOS were made using a standard process with a 2nm gate oxide and 55nm gate length. A 21 stage R/O circuit of same technology is evaluated. Only HCI and NBTI are considered because they are the dominant degradation mode for these devices technology.

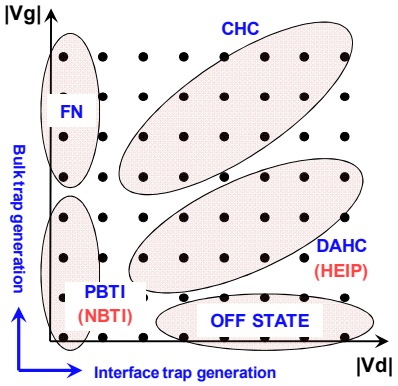

Fig. 1. Degrdation modes for gate and drain voltage

B. NBTI Model

Reaction diffusion (RD) theory is widely accepted to explain the NBTI mechanism. Recent works proposed a new NBTI mechanism related to charge trapping / de-trapping [11, 12]. For NBTI modeling, the composition model [6] using latest concept of NBTI [7~10] is adapted. In this model, two main physical mechanisms are considered for NBTI modeling . The first one is slow component, permanent part due to interface trap generation and the other one is fast component, recoverable part due to hole trapping / de-trapping. Interface trap and trapped hole induce threshold voltage shift. The equation for interface trap density (N_{IT}) and trapping hole density (N_{OT}) main equation are respectively represented in the (1, 2).

$$N_{IT,NBTI}(t) \propto K_p E_{OX}^{A} \exp\left(-\frac{E_\alpha}{kT}\right) t^n \quad (1)$$

$$N_{OT,NBTI}(t) \propto K_r E_{OX}^{B} \ln\left(1+\frac{t_s \tau_e}{t_r \tau_c}\right) \quad (2)$$

where E^{A}_{OX} and E^{B}_{OX} denote an electric field of P and R part and E_a indicate an activation energy.

The slow component of NBTI, N_{IT}, is measured by Measure-Stress-Measure due to its second level measure delay between stress and measure. So we call the slow method in the following. On the other hand, On-The-Fly method [13], is able to measure all NBTI components including the fast one, N_{OT} because its measuring delay is very short. We call it fast method.

C. HCI Model

In the proposed method, the following power model (3) is used for HCI since our device shows a general HCI voltage dependent degradation behavior [14].

$$N_{IT,HCI}(t) \propto \exp\left(-\frac{\alpha}{E_{lateral}}\right) t^n \quad (3)$$

where $E_{lateral}$ denotes lateral component of electrical field.

III. RESULTS AND DISCUSSION

A. *Poly depletion effect on Oxide Electrical Field*

It is well-known that poly depletion affects electrical field. The poly depletion makes a potential drop in the Poly-Si gate which reduces E_{ox} shown below.

$$E_{OX} = V_{OX}/T_{OX} = \{V_{GS} - V_{FB} - (\Psi_{Si} - \Psi_{PolySi})\}/T_{OX} \quad (4)$$

where Ψ_{PolySi} denotes potential drop in poly silicon. E_{ox} reduction is more serious when poly doping levels is low. However, poly depletion is not easy suppresed because doping concentration is limited by low dopant solubility and high boron penetration especially for PMOS.

TCAD simulation shows that E_{ox} starts to decrease gradually above nominal operation voltage (Fig. 2) by poly depletion effect (4). We can see that the slope of E_{ox} is changed for different Vg bias. Blue dot line which is extrapolated from gate bias -3V, is larger than rectified E_{ox} by the poly depletion effect. A lifetime calculation model also use extrapolation method based on experimental data obtained at V_{GOP}. It indicates that lifetime can be underestimated if poly depletion is not considered.

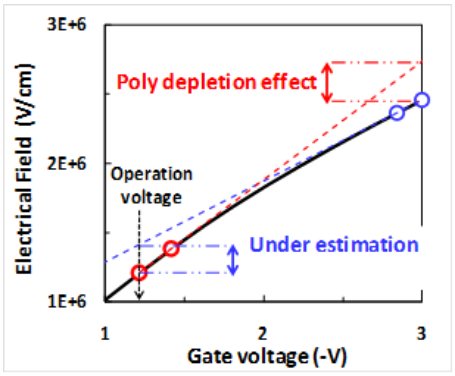

Fig. 2. Electrical field slope against Vg. Eox slope decrease as gate bias higher due to PDE.

B. *Effect of Accumulated Charge on Eox*

Figure 3 shows calibrated results for various stress bias. Fast and slow in Fig. 4 represents the threshold voltage shift obtained by fast and slow method respectably. Fast method can measure both N_{IT} and N_{OT}. and slow method measure only N_{IT}.

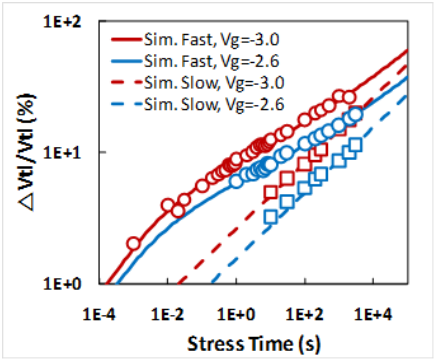

Fig. 3. NBTI calibration results with experimental obtained by fast and slow method. Fast includes N_{IT} and N_{OT}. Slow includes N_{OT}.

The threshold voltage shift during NBTI degradation indicates continuous formation of trap and accumulation of negative trapped charge. As a result, E-field is reduced due to trapped charge and Fig. 4 shows the E-field reduction mechanism by trapped charge. Actually E_{OX} is not changed much. However, inversion hole which is a little separated from interface by quantum effect, feel reduced E-field because accumulated trapped charge at interface screen E-field.

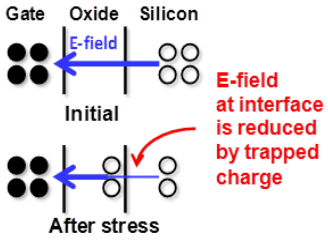

Fig. 4. Simple schematic diagram for trapped charge effect on Eox. The Eox at interface is reduced due to trapped charge.

Previously mentioned, there are two components in NBTI model. The fast component of NBTI is only measured by fast measure method. That mean the ATCE on E_{ox} obtained by slow method is underestimated because only N_{IT} of NBTI is measured by slow method. However, N_{OT} is also increased during the degradation. Therefore, both N_{IT} and N_{OT} of NBTI charge should be considered to evaluate the total E-field reduction.

Figure 5 shows TCAD results of ATCE on E-field. Our simulation condition is that trapped charge is obtained by fast method and time to 20% of threshold shift is device lifetime. In other words, both N_{IT} and N_{OT} cause 20% of threshold voltage shift. At low gate bias, the contribution of E_{ox} reduction is much larger than at high gate bias condition. Similar to the poly depletion effect, ATCE significantly affect lifetime.

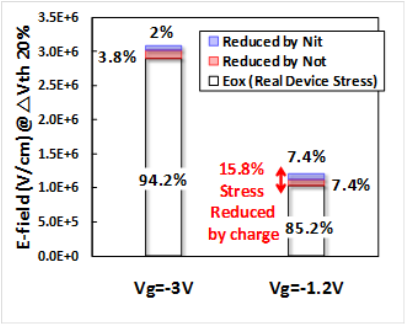

Fig. 5. Trapped charge effect on E_{ox} reduction. Same V_{TH} degradation case is assumed but different stress reduction is shown.

C. *Prediction of Device Lifetime*

Both PDE and ATCE are considered by TCAD. To solve ATCE, full transient simulations are performed self-consistently: The E_{ox} reduction by ATCE increases due to time dependent trap generation. Figure 6 shows excellent correlation between simulation and measurement. Two conclusions came out: (1) Lifetime extracted by fast method is lower than the one extracted by slow method. Conventional lifetime extrapolation model predicts an opposite result as shown in Fig. 6. (2) More than 1 order lifetime shift is observed due to E_{ox} reduction by PDE and ATCE (Fig. 7).

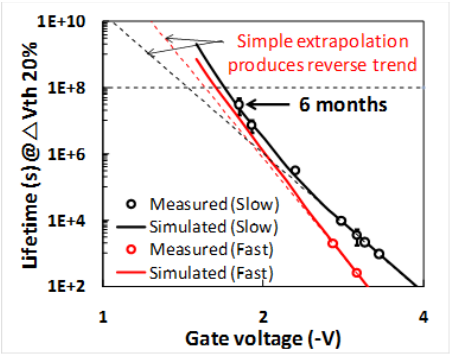

Fig. 6. Lifetime prediction by simulation and conventional method. Extrapolation underestimate lifetime and produce reversal lifetime.

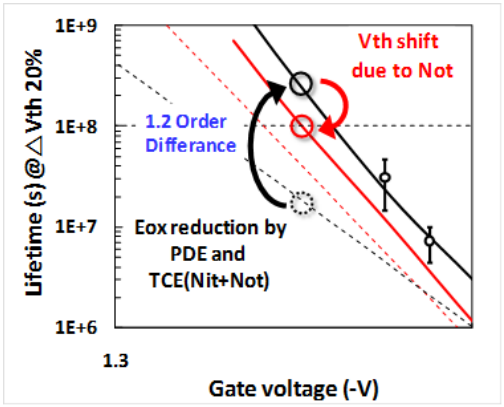

Fig. 7. Lifetime shift mechanism. Extrapolation model based on slow method underestimate lifetime more than 1 order.

D. *Prediction of Circuit Lifetime*

For propagation delay time (t_{PD}) degradation simulation for HCI and NBTI stressed R/O circuit, Samsung reliability simulator (SRSIM) [15] was adopted. The SRSIM calculate circuit level reliability based on AC waveform and degradation model.

The same compact model parameter as the one calibrated on device data is used for circuit degradation simulation. To estimate accurate NBTI and HCI lifetime, Eq. (1~3) are updated with E_{ox} that include PDE and ATCE. For practical simulation time, V_{TH} shift due to N_{OT} is considered constant after saturation (Fig. 8a). The t_{PD} degradation simulation results well matched the measurements (Fig. 8b).

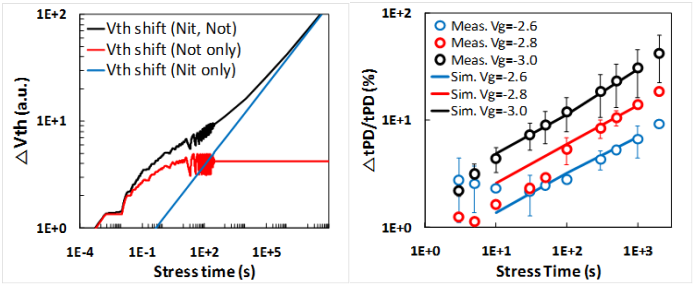

Fig. 8. Circuit simulation method and tPD degrdation calibration results.

(a) Circuit simulation method for Not calculation of NBTI under AC bias at MHz Freq. To reduce simulation time to practical level, N_{OT} is set as constant after saturated.

(b) tPD simulation of 21 stage R/O. It shows an excellent match with measurement.

Each degradation component of degradation has difference bias and time dependence. Figure 9 shows each components of t_{PD} degradation separately. With the passage of time, The N_{OT} component NBTI is lower comparing to other mechanism because of its early saturation by AC bias condition as shown in Fig. 8a.

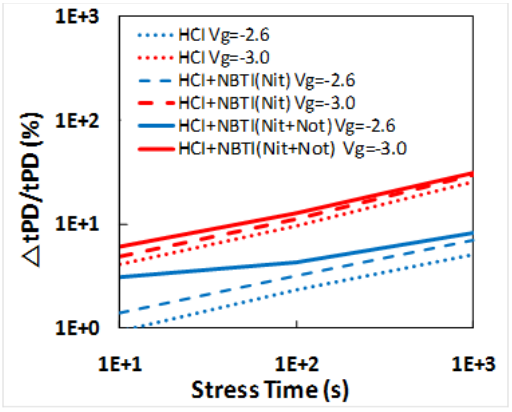

Fig. 9. t_{PD} lifetime simulation for various gate voltage.

A simulation of t_{PD} lifetime in Fig. 10 shows that conventional lifetime extrapolation model underestimates t_{PD} lifetime similarly to device lifetime simulation trend. However, the N_{OT} effect on t_{PD} degradation is relatively smaller than V_{TH} degradation of device because of its early saturation.

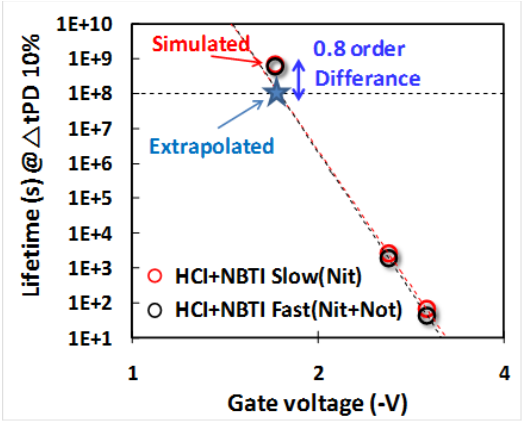

Fig. 10. t_{PD} lifetime prediction results. Extrapolation model which doesn't include PDE and ATCE, underestimate t_{PD} lifetime. N_{OT} effect at circuit is lower than one at device.

IV. CONCLUSIONS

By quantitative approach for poly depletion and degradation charge, we clarify that the debate in the difference NBTI lifetime behavior between fast and slow method. We demonstrated that conventional model underestimate lifetime more than 1 order and produce reverse lifetime trend for fast and slow measured experimental due to incorrect modeling. We verify that its impact on circuit parameter degradation by applying our methodology.

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