Variability-Aware Compact Model Strategy for 20-nm Bulk MOSFETs

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***Abstract*—In this paper a variability-aware compact modeling strategy is presented for 20-nm bulk planar technology, taking into account the critical dimension long-range process variation and local statistical variability. Process and device simulations and statistical simulations for a wide range of combinations of L and W are carefully carried out using a design of experiments approach. The variability aware compact model strategy features a comprehensively extracted nominal model and two groups of selected parameters for extractions of the long-range process variation and statistical variability. The unified variability compact modeling method can provide a simulation frame for variability aware technology circuit co-optimization.**

Keywords—compact model, MOSFET, variability

I. Introduction

Ever increasing nano-scale MOSFET variability brings significant challenges to circuit design, necessitating accurate trade-offs between performance and power. On the process induced variability side, for example, focus variations in lithography or inhomogeneities in etching or deposition equipment can cause long-range process variation (PV) of critical dimensions (CDs) [1]. On the other hand, random dopants (RDD), line edge roughness (LER), and metal gate granularity (MGG) introduce uncontrollable purely statistical variation (SV) [2]. Variability compromises the design margins of energy and timing of circuits [3], and it greatly affects the SRAM cell read/write margins [4]. Tight design margins of advanced nanoscale MOSFET technology circuits require accurate compact modeling of device variability in order to achieve optimized performance and power tradeoff. Therefore, we propose a unified compact modeling strategy combining process and statistical variability for the purpose of accurate statistical circuit simulation and verification [5] based on solid and consistent simulations and model extractions. We demonstrate our strategy using a realistic 20-nm bulk planar MOSFET.

II. TCAD Atomistic Device Simulations

A. Device Description

The 20-nm bulk planar CMOS technology is coming to mass production, although FinFETs and SOI MOSFETs have been introduced already. The nominal testbed device is a bulk MOSFET with *23.5 nm* gate length and *33 nm* channel width and *1.0 nm* of equivalent oxide thickness. The realistic three-dimensional (3D) device structure including the shallow trench isolation (STI) and high-k/metal gate stack is presented in Fig. 1(a). 3D process simulation was carried out using Sentaurus Process [6]. The channel is doped with a concentration of $\sim 5/3\times10^{18}$ cm^{-3} respectively for n-/p-channel device, and source/drain regions are doped with peak concentration of 3×10^{20} cm^{-3} and the extension regions have a peak density of $\sim 4\times10^{19}$ cm^{-3}. The device structure and doping profiles were transferred to the GSS atomistic simulator Garand [7], which was employed for physical simulations of the interplay between process and statistical variability [8]. Details on the interface are being published elsewhere [9]. The device simulation features mobility models with strain enhancement and density gradient quantum corrections. The n-channel transistor achieves on-current *790 μA/μm* at off-current *0.14 nA/μm* at high drain bias of supply voltage *0.9V*.

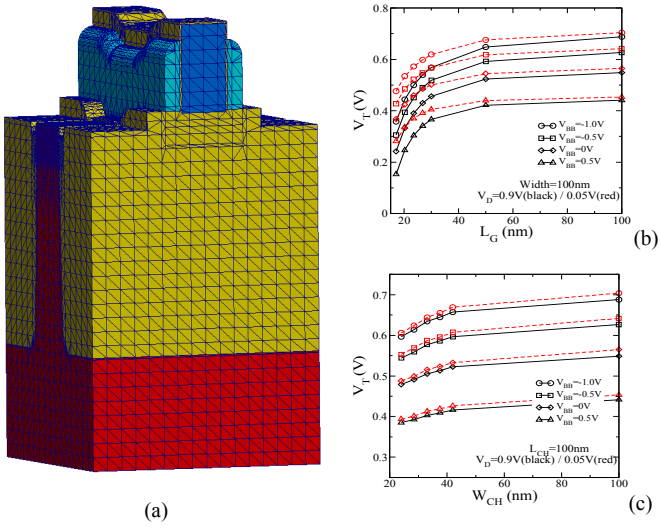


Fig. 1. (a) Simulation domain of a bulk planar n-channel MOSFET, including the realistic structures of high-k/metal gate stack and STI into simulations. The gate-length variation simulation (b), and channel width variation simulations (c).

The research leading to these results has received funding from the European Union Seventh Framework Programme (FP7/2007 – 2013) under grant agreement no. 318458 SUPERTHEME.

We first examine the short-channel effect and width effect. In order to decouple these two effects two series of transistors, with gate geometries of wide W or long L but the other variable varying, are simulated under various bias conditions. The short-channel effect is shown in Fig. 1(b) and reverse back bias enhances the threshold-voltage roll-off effect. Narrow width effect is also shown in Figure 1(c) due to early turn on by the enhanced electric field at width end in the presence of STI. The simulations are beneficial to compact model extraction since it facilitates the separate capturing of two effects in the model.

B. Simulations of Process and Statistical Variability

The long-range process induced variations of L and W are simulated using a design of experiment (DoE) approach. Table 1 lists the distinct values of L and W considered, and the transistor transfer characteristics are simulated for Cartesian product of these values. The figures of merit (FoM) of the DoE simulations are extracted. The threshold voltage is extracted using a constant sub-threshold current of $10^{-7}\times W/L$ Amps. As illustrated in Fig. 2, the FoM response surfaces of L and W indicate large variations of transistor electrical characteristics as gate geometry varies. The channel length variation causes major V_T fluctuations compared with width variation, and short channel transistors have larger on-current and worse SS and DIBL as expected. The L and W dependences of the figures of merit are used to monitor the accuracy of the process dependent part of the compact model.

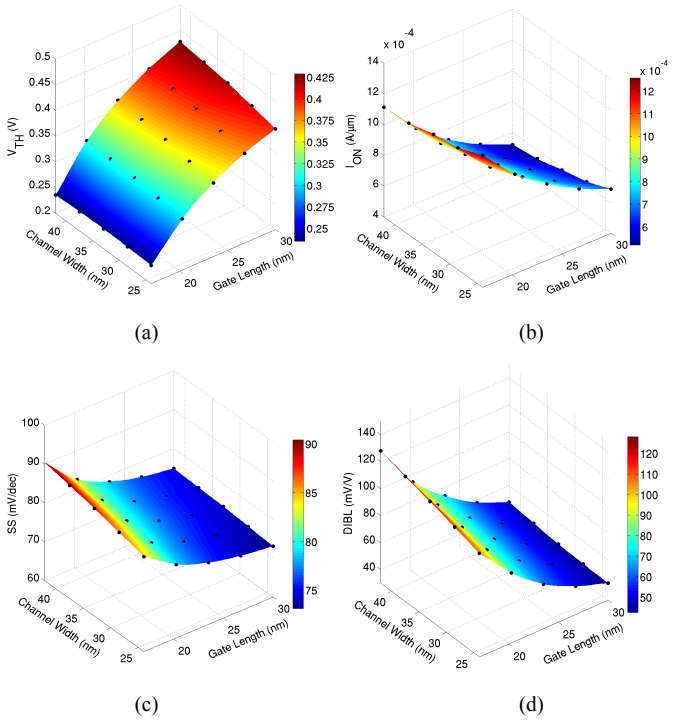


Fig. 2. The figures of merit of an array of simulated devices with L and W process variations, including threshold voltage (a), on-current (b), subthreshold-slope (c) and drain induced barrier lowering (DIBL) (d).

TABLE I. THE L AND W PROCESS VARIATIONS.

L [nm]	17	20.25	23.5	26.75	30
W [nm]	24	28.5	33	37.5	42

Statistical simulations including RDD, LER and MGG are carried out for each node of the DoE matrix for samples of 1,000 statistically different transistors. LER is parameterized with three RMS of 2 nm and correlation length of 30 nm [10], and MGG has average grain diameter of 5 nm and two work-functions differing by 200 mV [11][12]. The simulation results for one of the 25,000 statistically different transistors in Fig. 3 illustrates the impact of the metal grains, gate edge fluctuations and random dopants. The variations in electrical characteristics and threshold voltage fluctuations for the four extreme corners of L and W and the nominal design are shown in Fig. 4(a) and 4(b). The V_T standard deviation varies from the smallest *38.3 mV* at the slow corner (L=30nm, W=42nm) to the largest *66.9 mV* at the fast corner (L=17nm, W=24nm), compared to *45.4 mV* for the nominal design. Those simulated are used for statistical compact model extraction in next section.

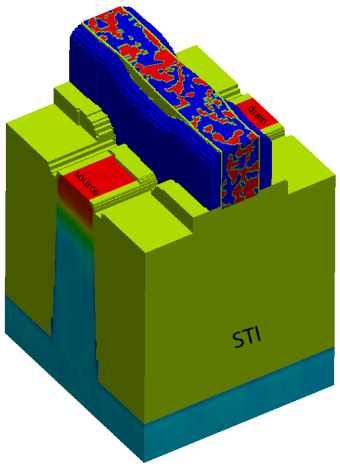


Fig. 3. An example of 3D atomistic device simulated with major statistical variability sources RDD, LER and MGG.

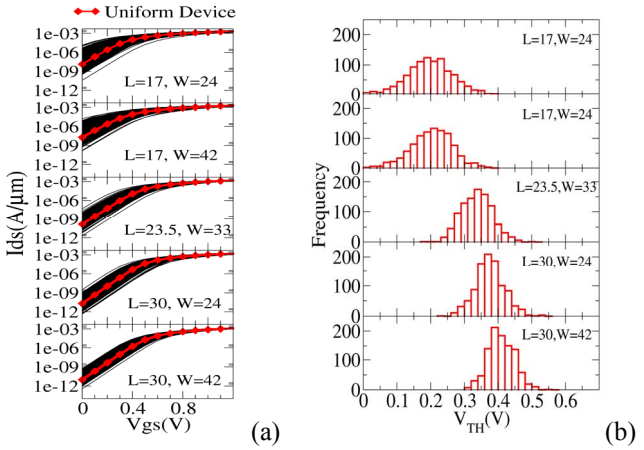


Fig. 4. (a) Transfer characteristics at four CD process corners and nominal design, and corresponding threshold voltage distributions (b).

III. Unified Compact Model Approach

A. Extraction of Unified Variability Compact Models

In this section, the compact models are extracted to capture PV and SV simultaneously following the above simulation strategy. The proposed unified compact modeling strategy consists of three steps: 1) nominal uniform model extraction; 2) extension of the model to cover process variation in the DoE space; 3) extraction of statistical variability correlated to the process variations (Fig. 5). The GSS compact model extractor Mystic [7] is used to extract BSIM4 compact models. Mystic is integrated in the GSS tool chain and links to Garand through a database that contains the results of the 25,000 DoE statistical simulations. Two distinct groups of parameters are used to capture the effects of process and statistical variations, respectively.

First an L and W dependent nominal compact model is extracted and its accuracy is illustrated in Fig. 6. Sub-threshold and over-drive parts of I_G-V_D and their back bias dependence are well captured and output I_D-V_D is reproduced. Process corners of L (23.5±6.5 nm) and W (33±9 nm) fully enclose the range of realistic process variations, and are used for the extraction of Group 1 compact model parameters to form the more accurate process extended model. The $L \times W$ distributions of key figures of merit were used to monitor accuracy of process extended model in Fig. 7(a) demonstrating that the error in the threshold voltage from compact model is minimized. Building on the extended process model, the second group of parameters is used to extract the corresponding statistical variability at each DoE point. The Group 2 statistical compact parameters capture the distinct impact of statistical variability sources on the device characteristic. As shown by Fig. 7(b), the extracted statistical sets of compact models accurately follow the TCAD simulated statistical variability of figures of merit, and their correlations. Later, PV parameters and SV parameter distributions are interpolated in $L \times W$ space, and are continuous with L and W. The described compact model strategy satisfies the requirements for nominal design, process variation aware design and fully statistical design in a wide range of CD variations.

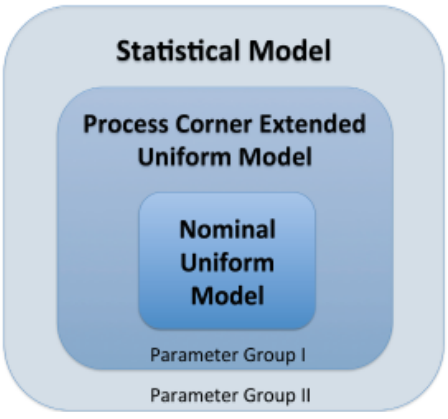
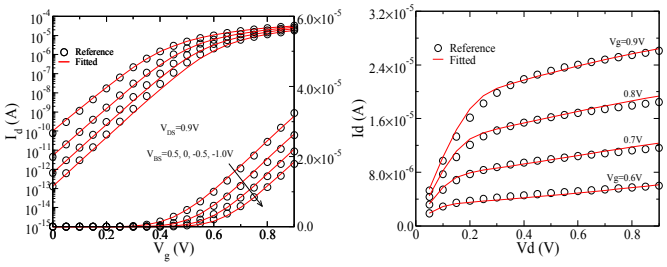
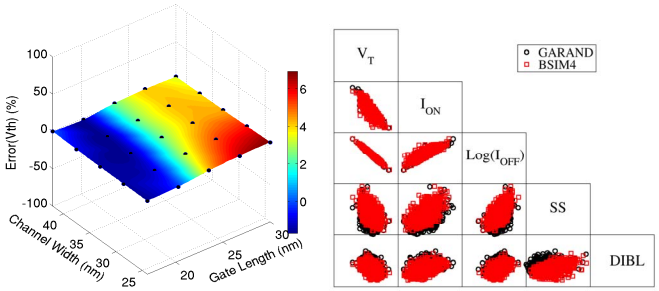


Fig. 5. Schematic view of the unified compact modelling strategy. It features nominal uniform model, and two groups of compact model parameters, and enhanced statistical models.



(a) (b)

Fig. 6. Comparison of transfer characteristics I_D-V_G (a) and I_D-V_D (b) from comprehensively extracted nominal uniform BSIM4 model and GARAND simulations..



(a) (b)

Fig. 7. (a) The V_T error control of process model compared with device simulations over L and W space. (b) The scatterplots of figures of merit obtained from statistical models and GARAND.

B. Demonstrations

Based on this variability-aware compact model extraction strategy the statistical GSS circuit simulation engine RandomSpice [7] can generate correlated process-aware and statistical compact models. First, process variation distributions of L and W are assumed for the further simulations (Fig. 8). For each (L, W) input the first group of process variation parameters and the second group of statistical extraction parameters are generated and applied, through the following algorithm:

Step 1: For each circuit, (L, W) ~ Distribution (here Gaussian distribution with sigmas of 1.5nm and correlation of 0.5);

Step 2: Determine process variations by applying $P = f(L, W)$ to group I parameters;

Step 3: For each transistor, apply SV (group II parameters orthogonal to PV parameters).

An additional approach to trace variations by process simulations and to combine the results with Garand and Mystic is described elsewhere [13]. For the gate dimension data assumed in Fig. 8 it is evident the PV and SV act together leading to larger spread of threshold voltage (Fig. 9) and heavily skewed distribution (Fig. 10) compared with only SV present. DIBL can also seriously degrade since V_T rolls off steeply when process variations act in reducing the gate length (Fig. 10).

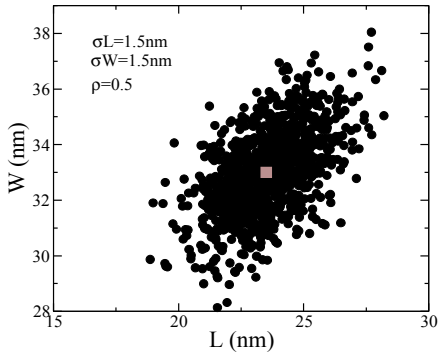


Fig. 8. Assumed generation of correlated Gaussian distributions of L and W process variations.

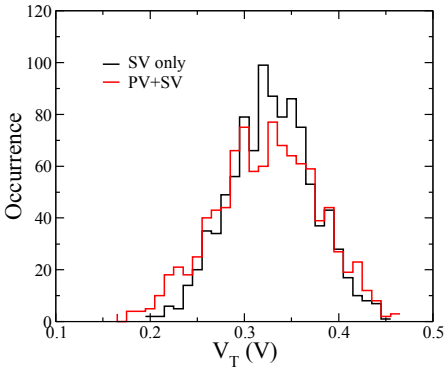
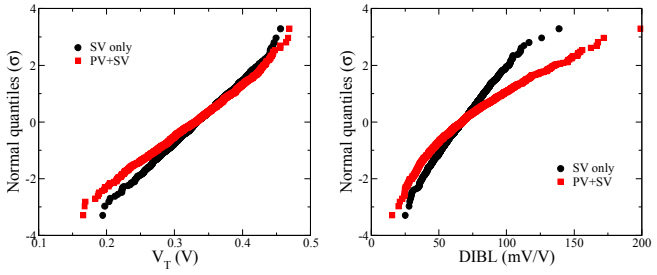


Fig. 9. Vt distributions from model with SV-only vs from models with PV and SV together.



(a) (b)

Fig. 10. Normal Q-Q plots of V_T (a) and DIBL (b) from SV-only models vs PV and SV together models.

IV. Conclusions

We illustrated that our unified variability compact model strategy in a realistic bulk 20 nm MOSFET through advanced TCAD simulations. It can efficiently provide the compact models simultaneously capturing accurate effects of long-range process variation and local statistical variability on transistors' electrical characteristics. Through a demonstration of unified variability compact models, the transistor subject to two types of variability undergoes larger FoM variation compared to only statistical variability, and FoM distributions are significantly changed.

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