

The Discrepancy Between the Uniform and Variability Aware Atomistic TCAD Simulations of Decananometer Bulk MOSFETs and FinFETs

F. Adamu-Lema¹, S. M. Amoroso¹, X. Wang¹, B. Cheng^{1,2},

¹University of Glasgow, School of Engineering, Oakfield Ave., Glasgow, UK, G12 8LT

L. Shifren³, R. Aitken³, S. Sinha³, G. Yeric, A. Asenov^{1,2}

³ARM Ltd, Cambridge UK, ²Gold Standard Simulations L.td., Oakfield Ave, Glasgow, UK, G128LT

Abstract— In this paper we discuss results from ‘atomistic’ and continuous simulation of decananometer scale bulk MOSFETs and FinFETs. We study the behaviour of important figures of merit including threshold voltage, off current and on current. We provide physical explanation for the origin of the discrepancies between the averaged values obtained from the statistical simulations and the results from the continuous doping simulation. Based on our analysis we clearly demonstrate that there are increasing errors in the doping distributions when device TCAD simulations are calibrated using continuous doping profiles. This questions the use of continuous doping profiles in the routine calibration and TCAD based optimisation of decananometer scale bulk MOSFETs and FinFET.

Index Terms—Atomistic doping; continuous doping; density gradient; statistical simulations; random dopants, FinFET

I. INTRODUCTION

With the scaling of the CMOS transistors to decananometer dimensions, atomic scale effects start to play increasingly important role in their behavior [1]. The discreteness of charge and granularity of matter introduces unavoidable, purely statistical variations in the transistor characteristics that increase progressively with the reduction of the device dimensions [2][3]. The saturation of performance in bulk MOSFETs associated with high channel doping and the corresponding increase in statistical variability is one of the main factors facilitating the introduction of new transistor architectures that tolerate low channel doping with improved electrostatic integrity like FinFETs [4][5] and Fully Depleted SOI (FDSOI) transistors [6]. Although the impact of different variability sources on key figures of merit like V_T , I_{ON} , I_{OFF} , [7][8] RTN and on the time dependent statistical reliability related to PBTI/NBTI [9][10] are well understood and factored in transistor and circuit simulation and design, it is still not completely clear what is the impact of atomic scale effects on the TCAD simulation technology and practices. Currently, the bulk of the TCAD usage is based on continuous treatment of doping and uniform material composition at both process and device simulation stages. In this paper we examine the progressively increasing discrepancies

in the transistor behavior when simulated using continuous methods and when using ‘atomistic’ techniques that reflect more accurately the physical reality.

Using both bulk MOSFETs and FinFETs as examples we show that the use of continuous doping leads to misleading and erroneous results, significantly affecting the process and device TCAD calibration, and by yielding wrong dopant distributions negatively affect the TCAD guided technology development.

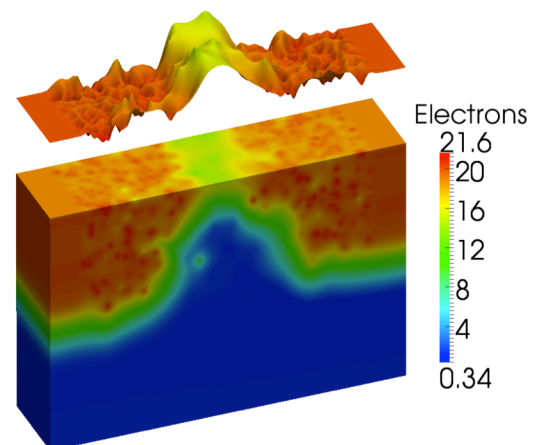


Fig. 1 A typical 3D profiles of electron distributions of the atomistic simulation of one individual 25nmx25nm transistor picked from a sample of the 1000 transistors

II. TEMPLATE TRANSISTORS AND SIMULATION METHODOLOGY:

The ‘template’ transistors used in this study are n-channel MOSFETs designed to meet the requirements of the 20nm bulk CMOS technology (Fig.1) and a p-channel FinFET representative for 10nm CMOS technology generation (Fig. 5). The TCAD based transistor design is performed using the GSS ‘atomistic’ device simulator GARAND [11]. While the nominal channel length is 25 nm, in the case of bulk MOSFET,

transistors with multiple channel lengths and widths are simulated (Fig. 2a, b, c) to highlight the discrepancies between the continuous and atomistic dopant simulation. Similarly, a bulk FinFET with 64nm gate pitch (Fig. 5), 40nm fin pitch, channel length of 28nm, 8nm thick spacer, 44nm fin height and a fin width of 8nm (with an ideal square fin shape and simplified doping profile) is

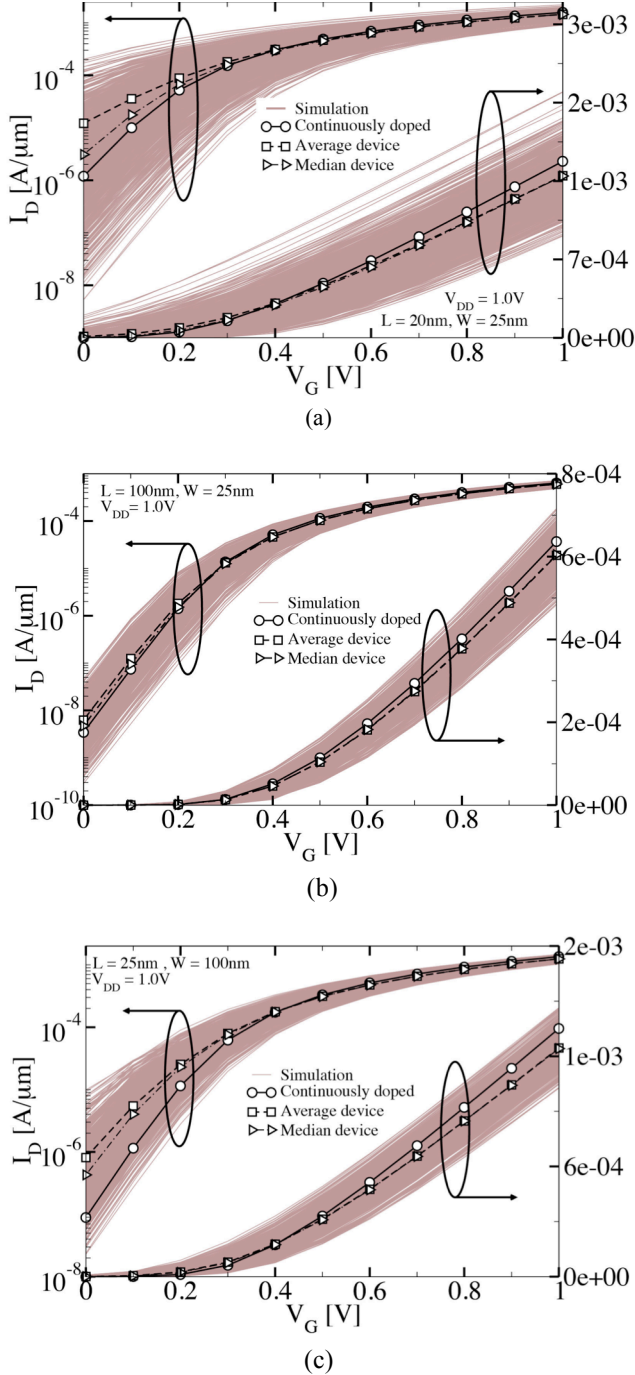


Fig. 2 Simulated I_D - V_G characteristics of 25(L) \times 25(W) nm (a), 100(L) \times 25(W) nm (b) and 25 \times 100(W) nm (c) for an ensemble of 1000 microscopically different transistors at high V_D

considered. The atomistic simulations in the FinFET case are performed for various doping levels to highlight the difference between the results of the continuous doping simulation and the average ‘atomistic’ simulations at different channel doping concentrations.

III. RESULTS AND DISCUSSION – BULK MOSFET:

The impacts of the individual and combined statistical variability sources on the distribution of key transistors figures of merit are reported in [12]. This abstract focus solely on the discrepancies between the ‘atomistic’ and the continuous drift diffusion (DD) simulations. Fig. 2a depicts the I_D - V_G characteristics of an ensemble of 1000 devices of bulk MOSFET with physical gate dimensions of 25 \times 25nm². The averaged, the median across the statistical ensemble and the continuously doped transistor current voltage characteristics are also included in the plot. It is clear that there are substantial differences between the ‘continuous’, the average and the median characteristics. In Fig. 2b-2c we plot the same set of characteristics for a 100(L) \times 25(W) nm² and for a 25(L) \times 100(W) nm² transistors respectively. There are several important physical differences between the average/median and the continuous characteristics. Firstly, the V_T extracted using both linear interpolation or current criterion in the sub-threshold region is lower for the average curve (Fig. 3) and secondly, the V_T lowering is independent on the channel width but depends strongly on the channel length as illustrated in Fig. 3. This is well known physical effect in the ‘atomistic’ simulations or indeed real life measurements due to potential fluctuations and current percolations in the valleys between the discrete dopants. Moreover, the combination of V_T lowering and degradation of sub-threshold slope results in dramatic

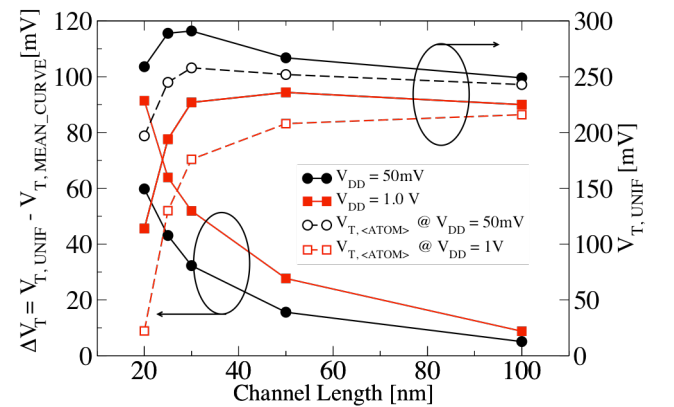


Fig. 3 V_T lowering at low and at high V_D as a function of the channel length, with width of 25nm (right axis)

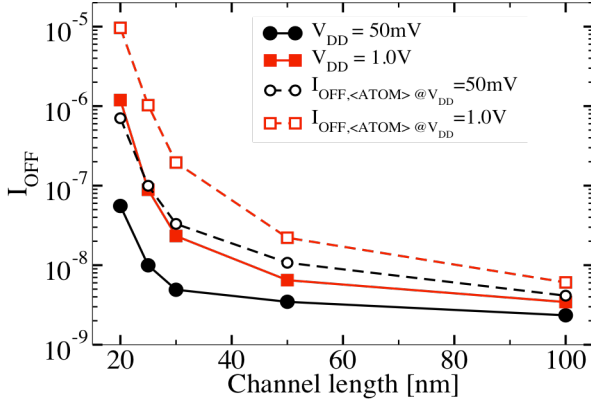


Fig. 4 I_{OFF} comparison between continuous doping and atomistic simulations

differences in I_{OFF} as shown in Fig. 4.

IV. RESULTS AND DISCUSSION – P-TYPE FINFET

The characterization of the difference between the results of the continuous doping simulation and the average ‘atomistic’ simulations of FinFETs is depicted in figure 8. This quantifies the error made when using continuous doping TCAD in assisting the design of FinFETs (Fig. 6) and corresponding CMOS technology as discussed earlier.

Figure 7 presents the dependence of the threshold voltage lowering on the fin doping concentration, comparing results from continuous doping simulations with averages of statistical simulations. There is practically no V_T lowering at doping concentration of $1 \times 10^{17} \text{ cm}^{-3}$ at high drain bias and even a slight inversion of the threshold voltage lowering at low drain bias. On the other hand, V_T lowering at high drain bias reaches approximately 20 mV at channel doping of $N_D = 4.5 \times 10^{18} \text{ cm}^{-3}$. A close inspection of the discrepancies between the uniform and the average atomistic simulations in Fig. 8 shows that the magnitude and the sign of the estimated threshold voltage lowering depends on the current criterion used to determine the threshold voltage. It is clear from Fig. 8 that even without threshold voltage lowering the average statistical simulations yields higher leakage current when compared with the continuous doping simulation. This highlights further the magnitude of the corresponding errors.

The presence of statistical variability results in a gradual extension of the transition region between sub-threshold and above-threshold regions of operation. Fig. 11 shows the I_{OFF}/I_{ON} tradeoff where off-current for

low power applications is reduced by increasing the channel doping and the same effect is achieved by changing the metal gate work-function. Finally Fig. 10 demonstrate the impact of the increased leakage current from the average ‘atomistic’ simulation on the I_{OFF}/I_{ON} tradeoff in comparison with the results previously presented in Fig. 9.

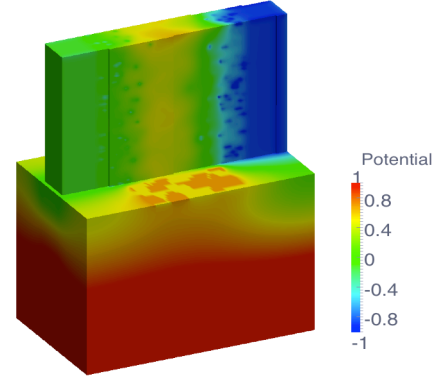


Fig. 5 A typical 3D potential profile of p-channel FinFET at $V_G = -750 \text{ mV}$, with channel doping of 1×10^{17} .

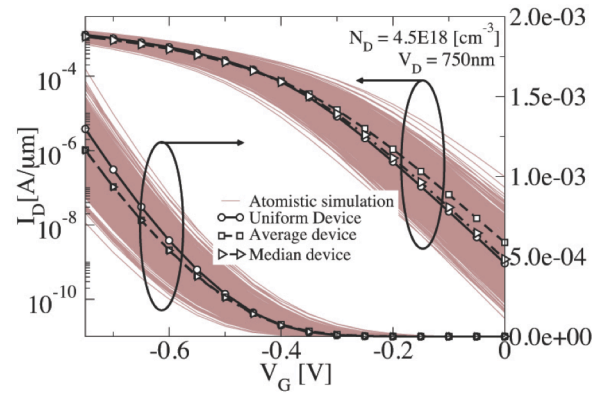


Fig. 6 $I_D V_G$ characteristics of ensemble of 1000 FINFETs transistors with fin doping of $N_D = 4.5 \times 10^{18} \text{ cm}^{-3}$ depicting the atomistic average, the median and the uniform device at high drain bias.

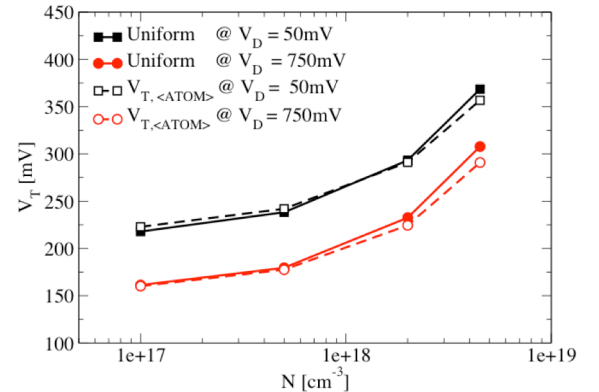


Fig. 7 Dependence of the threshold voltage lowering on the fin doping concentration

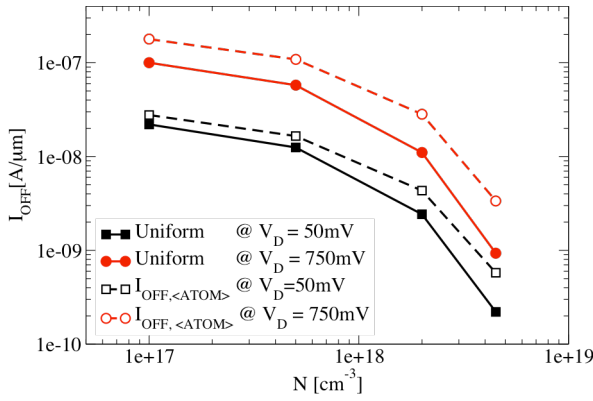


Fig. 8 Dependence of the I_{OFF} on the fin doping concentration: The difference at high V_D is already two times at a doping of $N_D=1 \times 10^{17} \text{ cm}^{-3}$ and increases to more than 3 times at a doping concentration of $N_D=4.5 \times 10^{18} \text{ cm}^{-3}$

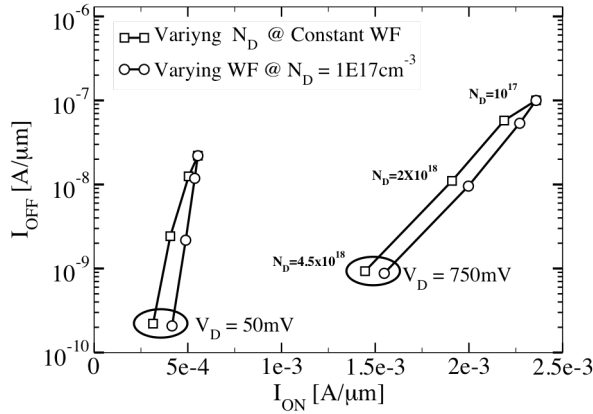


Fig. 9 I_{OFF}/I_{ON} tradeoff, where the filled symbols show the decrease in the off current as a result of increasing channel doping and the open symbols show a similar effect could be achieved by using workfunction engineering

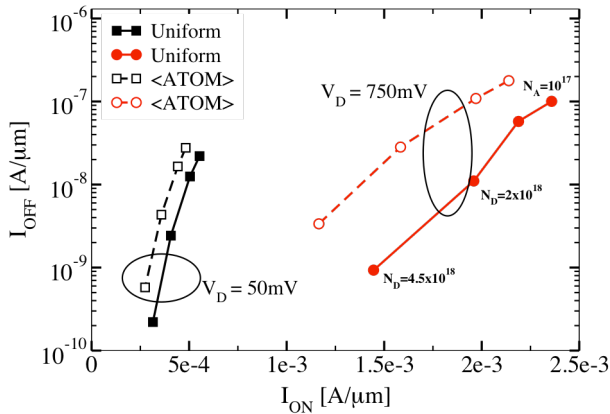


Fig. 10 I_{OFF}/I_{ON} tradeoff, a comparison between results that are obtained from continuous doping simulations and from the statistical simulations of atomistic average device

Based on the results for bulk MOSfets and FinFETS let us summarize the problems associated with the use of continuous doping profile in the TCAD simulation of the transistor characteristics:

- (i) If an accurate doping profile obtained from TCAD simulations or measurements is used in the continuous doping transistor simulations the results will be different compared to the self averaged measurements of the transistor characteristics and therefore wrong.
- (ii) The difference between simulated and measured characteristics increases with the reduction of the channel length due to the 'atomistic' threshold voltage lowering.
- (iii) In order to achieve agreement between the characteristics from the continuous doping TCAD simulations the 'true' doping profile has to be changed (adjusted) and this adjusted doping profile will no longer represent the real doping profile in the simulated transistor.
- (iv) The required alteration (massaging) of the doping profile is different at different channel lengths and is bigger for shorter devices.

V. CONCLUSION

We have clearly demonstrated that in particular the presence of discrete dopants, in decananometer bulk MOSFETs and FinFETs transistors results in a real physical changes in their average characteristics compared to the simulated characteristics obtained using continuous doping distribution despite the fact that this may be the average of the real atomistic doping distribution. This discrepancy creates problems when the continuous TCAD device simulations need to be calibrated to experimentally measure doping profiles, which always are average of atomistic doping distribution. This leads to increasing differences between the real doping profiles and the continuous doping profiles needed to achieve agreement between measurements and TCAD device simulations. The difference widens with scaling of transistors and puts into question the use of continuous TCAD in the device design and technology optimization loop. The solution is to use self-averaged 'atomistic' simulations in the calibration and in the design process.

Acknowledgment: This work has been partially supported by the European Commission through the FP7 grant agreement 261868 MORDRED.

REFERENCES

- [1] K. J. Kuhn, IEDM Tech. Dig., pp.471-474, 2007
- [2] A. Asenov, *Trans. Elec. Dev.*, pp.2505-2513,1998
- [3] O. Weber, et al., IEDM Tech. Dig., pp.10.4.1-10.4.4, 2008.
- [4] C. Auth, et al., VLSI Tech. Sym., 2012, pp.131-132.
- [5] X. Wang, et al., IEDM, 2011, pp.5.4.1-5.4.4.
- [6] N. Planes, et al., Sym. VLSI Tech., 2012, pp.133-134.
- [7] C. L. Alexander, *Trans. Electron Devices*, pp. 3251-3258, 2008.
- [8] S. Markov, *Trans. Electron Devices*, pp. 3106-3114, 2010.
- [9] F. Adamu-Lema, *Trans. Electron Devices*, pp. 833-839, 2013.
- [10] S. M. Amoroso, *Solid State Electronics*, Mar. 2013.
- [11] www.goldstandardsimulations.com/products/garand/, 2013.
- [12] X. Wang, et al., *Trans. Electron Devices*, pp. 1547-1554, 2013.