Large-scale 3D TCAD study of the impact of shorts in Phase Controlled Thyristors

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***Abstract*—Continuous advances in computer hardware and solving algorithm enable more pervasive use of 3D TCAD simulations for both nanoscale and power semiconductor devices. However, while BiMOS power semiconductor devices such as IGBTs require relatively small 3D simulated structures (of the order of ≈ 10x10x1000 μm^3), bipolar power devices such as thyristors require much larger simulated structures of the order of ≈ 10 mm^3. This work presents large scale 3D simulations of Phase Controlled Thyristors and describes the technique used to reduce computation times to extents compatible with industrial practice. 3D TCAD is used to understand the impact of cathode shorts on figures of merit such as the breakdown voltage and dV/dt.**

I. Introduction

Thyristors, initially called Silicon Controlled Rectifier (SCR) , are among the most widely used power semiconductor devices [1][2]. They are excellent devices for a wide variety of applications by virtue of their optimal carrier density configuration in the conducting state (resulting in very low on-state losses), device area up to 6 inches (large conduction current), and relatively straightforward fabrication process (lower cost).

Reaching blocking voltages in excess of 8.5 kV and on-state currents of 7 kA with a forward voltage drop lower than 2 V, thyristors are the device of choice for converter valves for the next generation UHVDC systems to be operated at power breaking level of 10 GW and with DC link voltages rated over 1000 kV [3]. 2D TCAD simulations are routinely used for power devices such as diodes, MOSFETs, and IGBTs to understand the physical behavior, reduce the need for expensive prototype lots and shorten the design cycle. The vertical dimensions of high power devices span from several hundreds to more than a thousand microns, resulting in finite element meshes of several tens of thousands points. However, analysis of asymmetric features such as cathode shorts in PCTs requires large scale (several cubic millimeters) full 3D TCAD simulations. Because of the curse of dimensionality, straightforward extension of 2D meshes in the 3rd dimension results in meshes of several million points, which cannot be solved in reasonable times for an industrial R&D environment. This work presents, for the first time, 3D simulations of devices of volume of several mm^3 and describes techniques to simulate such devices with reasonable accuracy in 1-2 days using commercial simulators and conventional hardware

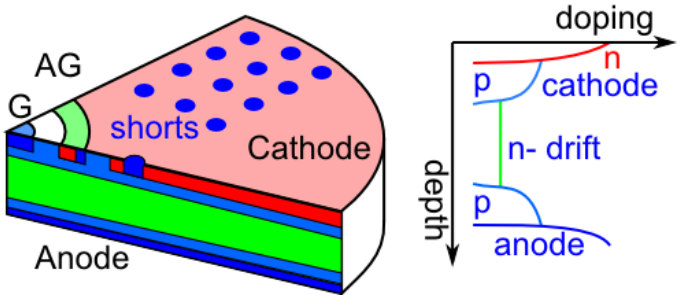

Fig. 1. Sketch of the typical structure of a modern PCT (left). The top side shows the Gate and Cathode contacts and the amplifying gate structure. The cross section indicates the doping regions. A schematic representation of the doping profiles under the cathode is presented on the right side.

[4][5][6]. Additionally, the impact of cathode shorts on key device parameters such as breakdown voltage (BV), dV/dt, and plasma spreading velocity is investigated with 3D TCAD and the relevant physical phenomena are discussed, obtaining additional insight over analytical models [7][8].

II. Thyristor device structure and behavior

The typical structure of a modern PCT is shown in Fig. 1 (left). The device is composed of an n^- drift region with p deep diffusions at the top and bottom sides [8]. The bottom side features a uniform p^+ diffusion for the anode (A) while the top side is patterned with p^+ and n^+ diffusions.

The p diffusions provide blocking junctions in both the forward and reverse bias conditions. The device is turned on injecting a current pulse in the p^+ main gate region (G) which triggers the positive feedback in the *pnp-npn* loop (shown in Fig. 2 for a device with an amplifying gate), sustaining the high carrier modulation in the drift layer .

In a PCT with only the main gate, initially the gate current sustains the hole current into the p-base, resulting in a weak turn-on of the cathode p-base junction, resulting into the injection of electrons into the n^- drift layer. The time required for the carriers to reach the anode and result in a significant injection of holes from the anode is known as the delay time and it can be significant for high-voltage thyristors. During the following phase of turn-on (the rise time phase), the excess charge concentration in the drift layer increases significantly,

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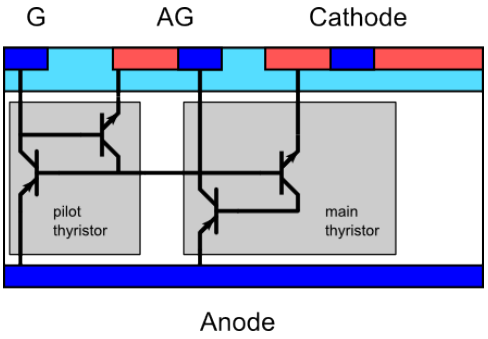

Fig. 2. Schematic representation of the *pnp-npn* positive loop and of the amplifying gate. The device cross section refers to Fig. 1

reducing the voltage drop across it and increasing current conduction. At the end of the rise time phase, the thyristor is ready to conduct in the region under the gate, which is heavily charge modulated [9]. During the plasma spreading phase a combination of the drift and diffusion mechanisms extends the conducting area from the edge of the cathode to the whole cathode area [7]. This process requires up to a few hundred microseconds for large area thyristors.

An additional amplifying gate (shown in Fig. 1 as AG) around the main gate is used to reduce the triggering current. The amplifying gate initiates conduction during the rise time phase of the main gate (since the lateral separation of the G and AG region is a small fraction of the thickness of device). As conduction is achieved in the main gate, the AG turns on very fast due to the high current provided from the pilot thyristor to the main thyristor, speeding up the turn-on process, as illustrated in Fig. 2. Modern amplifying gates are interdigitated or patterned to ensure fast spreading of the current (di/dt capability) during the turn-on process. Such designs result in a larger amount of cathode periphery in the proximity of the gate and therefore in a larger initial conductive region and in smaller plasma spreading times.

The cathode region (C) is characterized by several p^+ shorts (with typical diameter of $\approx$ 100 μm). Shorts provide a path to minimize the leakage current by reducing the *npn* current gain and hereby increase the forward BV [8]. They also improve the dV/dt capability of the device by removing displacement current which would otherwise turn on the thyristor when a rapidly changing voltage is applied (several kV/μs). However, a high short density reduces the cathode area (increasing the on-state voltage). The effective shorted area is greater than the sum of the individual areas of the shorts because the current flow lines bend in the proximity of the shorts increasing the unmodulated region.

Shorts also affect the plasma spreading during turn-on. While diffusion plays a role in plasma spreading, the dominating mechanism is drift due to the voltage difference between the conducting region of the *p*-base (at higher potential) and the non-conducting part, as shown in Fig. 3. Shorts reduce locally the potential, limiting the spreading velocity and consequently limiting the di/dt capability [10].

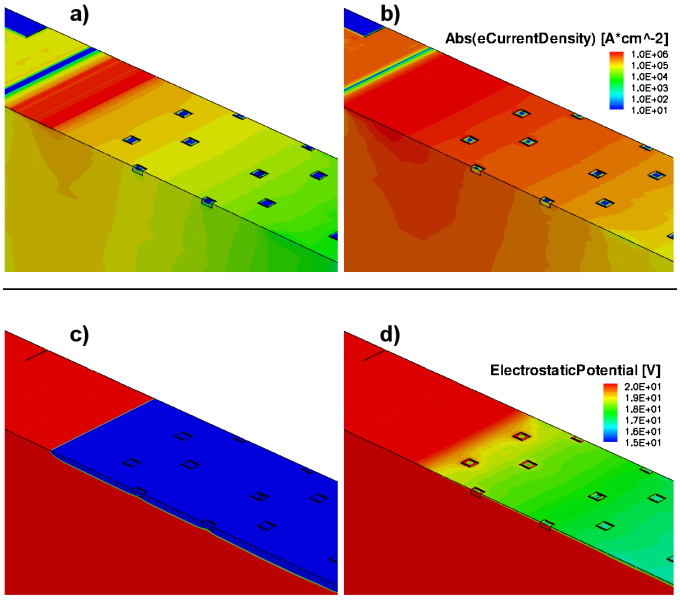

Fig. 3. 3D TCAD simulations showing the effect of shorts on plasma spread in the turn-on process. Plots a) and b) display the electron current density at successive instants. In plot a) the conduction through the cathode is small. In plot b) the portion of the cathode close to the AG is conducting significant current. Plots c) and d) show the corresponding electrostatic potential. Simulations indicate that the lateral voltage drop is mainly responsible for the plasma spreading velocity.

III. 3D PCT SIMULATIONS

A. Mesh generation procedure and optimal simulation setting

While 3D TCAD simulations are routinely used to simulate semiconductor devices, as described in [11], [12], the physical dimensions of bipolar power semiconductor devices such as thyristors pose significant challenges in terms of simulations time and convergence.

The device investigated in this work is a 2800 V, 620 A PCT with a diameter of 38 mm. The mesh spans $\approx$ 6x0.5x1.5 mm^3, a significant fraction of the full device. Approximations are introduced to reduce computation time. First, the simulation domain is a cuboid instead of a cylindrical sector. Then, the circular shorts are approximated by squares. In general, the mesh is extremely coarse but refinement boxes are judiciously applied in key areas to retain sufficient accuracy. A widely used rule of thumb is that the voltage drop in the forward mode across the edge of an element should be comparable to the thermal voltage V_{TH}.

Power semiconductors operate in a regime of ambipolar conduction where the electron and hole concentrations are identical in the drift region. Hence, the drift region is in a quasi-neutral condition and therefore the voltage drop over the modulated region is extremely low. Consequently, the discretization of the *Z*-axis of the device can be quite coarse. In the n^- drift region, the discretization of the *XY*-plane can also be coarse, since the carrier distribution is highly uniform. Given that commercial meshing software is based the OCTREE algorithm it is good practice to use powers of 2

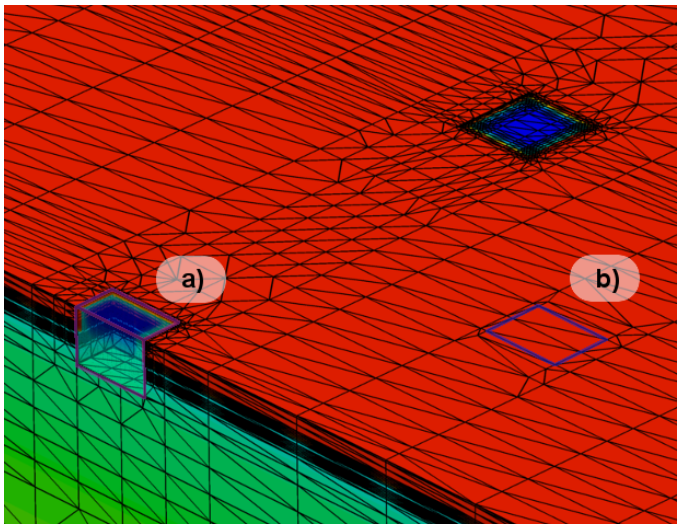

Fig. 4. Detail of a PCT mesh. Doping definitions for shorts are placed in both sites indicate by a) and b). However, due to the coarse initial grid definition chosen for the cathode in order to reduce the mesh size, the short at site b) is not correctly evaluated by the meshing algorithm and the mesh refinement specifications are ignored. To workaround this issue, a separate semiconductor region is defined in site a), forcing evaluation of the doping at the precise location of the short. This approach triggers the correct meshing refinement.

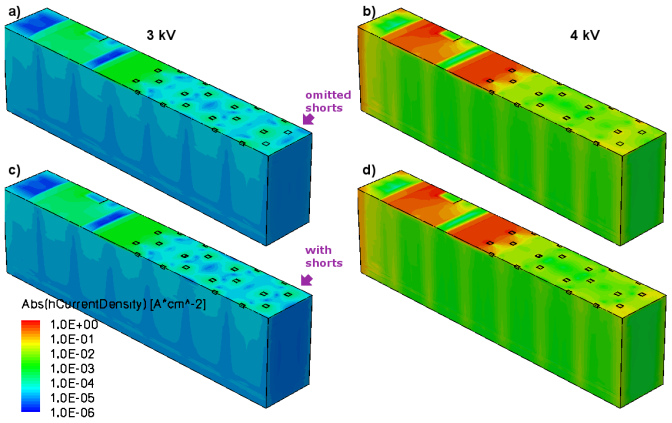

Fig. 5. Simulation of a PCT with 2 intentionally omitted shorts (structures a and b) and with complete shorts pattern (structures c and d). Plots a) and c) present the hole current density when the device is blocking 3 kV. Plots b) and d) show the device at 4 kV during breakdown. Simulations show that omission of shorts does not cause a failure in the cathode.

as the number of mesh divisions [13][4]. Finer refinement of the p / n^- drift junction is needed to acceptably reproduce BV. For forward conduction operation, it is necessary to refine the junctions near the gate, amplifying gate, and cathode.

Appropriate meshing of small features such as shorts can pose problems: refinement is increased evaluating on the analytical doping functions on the initial grid. If the initial grid is too coarse, the subsampling may cause small features like shorts to be ignored. This is shown in Fig. 4, where the refinement around the short labeled b) is ignored: the initial grid is so coarse that the local evaluation of the difference in doping concentration does not trigger additional refinements, resulting in a missing short. To avoid these problems, small cuboids are placed around the shorts to force the introduction of additional edges, as shown in Fig. 4. These edges trigger the refinement because doping profiles are evaluated at the manually introduced interface points. These techniques reduce the mesh size to less than 500,000 points.

Given the size of the mesh, it is possible to use only an iterative solver, which is less robust than a direct solver. Therefore, physical models should be chosen with care regarding convergence properties. For example, it is advised to use an effective, position-dependent lifetime instead of a full trap model to describe the effects of irradiation and lifetime engineering, which are typically employed to optimize the conduction / switching losses trade-off [14].

B. Discussion of results

In order to compare the effect of the short pattern on the breakdown voltage, several different short patterns are simulated, keeping the nominal total shorted area constant. As expected denser meshes with smaller shorts result in a modest increase of breakdown voltage. In fact, closer shorts reduce the voltage drop under the n^+ cathode. Therefore the leakage current needed to trigger the *npn* transistor is higher.

Structures with intentionally omitted shorts (Fig. 5) are also simulated to check whether this issue would cause a failure point in the cathode of the device.

This simulated case has practical relevance: in the case of a complex gate shape (like a hammer or spiral design [15]) the placement of the shorts is not trivial and some areas can be overshorted while others can be undershorted. Interestingly, meshes with intentionally omitted shorts (Fig. 5) show that the failure point of the PCT remains at the AG due to locally lower breakdown voltage, caused by doping curvature.

Triggering in the gate or in the amplifying gate is a desired feature, since the current pulse will rapidly trigger the whole device, preventing the formation of a filament carrying excessive current and potentially destroying the device.

The dV/dt is a critical key application parameter for a thyristor. It represents the steepest voltage rise between cathode and anode (with grounded gate) that the device can withstand without turning on. A large dV/dt means that the device is very rugged and cannot easily be spuriously fired. Fig. 6 shows a simulated dV/dt test over the capability of the device: the voltage waveform in Fig. 6 is applied to the PCT. The resulting displacement current triggers the device causing the rapidly increasing anode current.

Comparison of different shorting patterns show that the shorts near the amplifying gate play again a critical role in the device latch-up. The simulated hole current density is shown in Fig. 7.

The displacement current triggers the AG and then the cathode, even if the main gate is not triggered. This is in contrast to a conventional turn-on, where the gate conducts first, igniting almost instantly the amplifying gate as well.

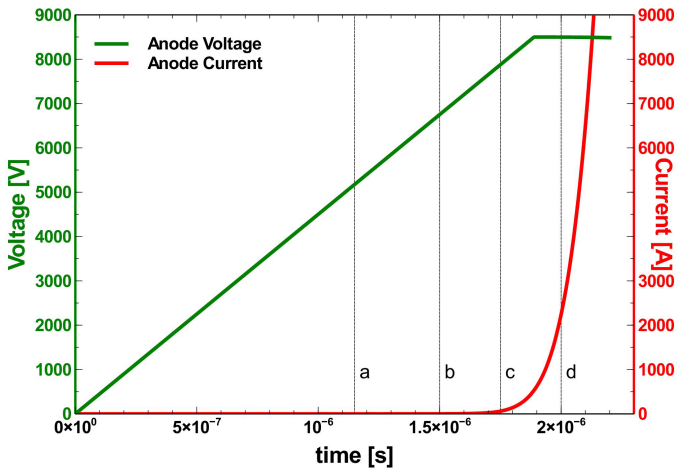

Fig. 6. Simulated *dV/dt* waveforms for a PCT.

IV. Conclusion

This work demonstrates the feasibility of large scale 3D simulations of Phase Controlled Thyristors and presents techniques apt to reduce computation times to reasonable extents for industrial practical applications. 3D TCAD is used to understand the physical behavior of PCTs in the blocking, turn-on and dV/dt operation modes. The short pattern affects strongly the plasma spread velocity, the speed of turn-on, and di/dt.

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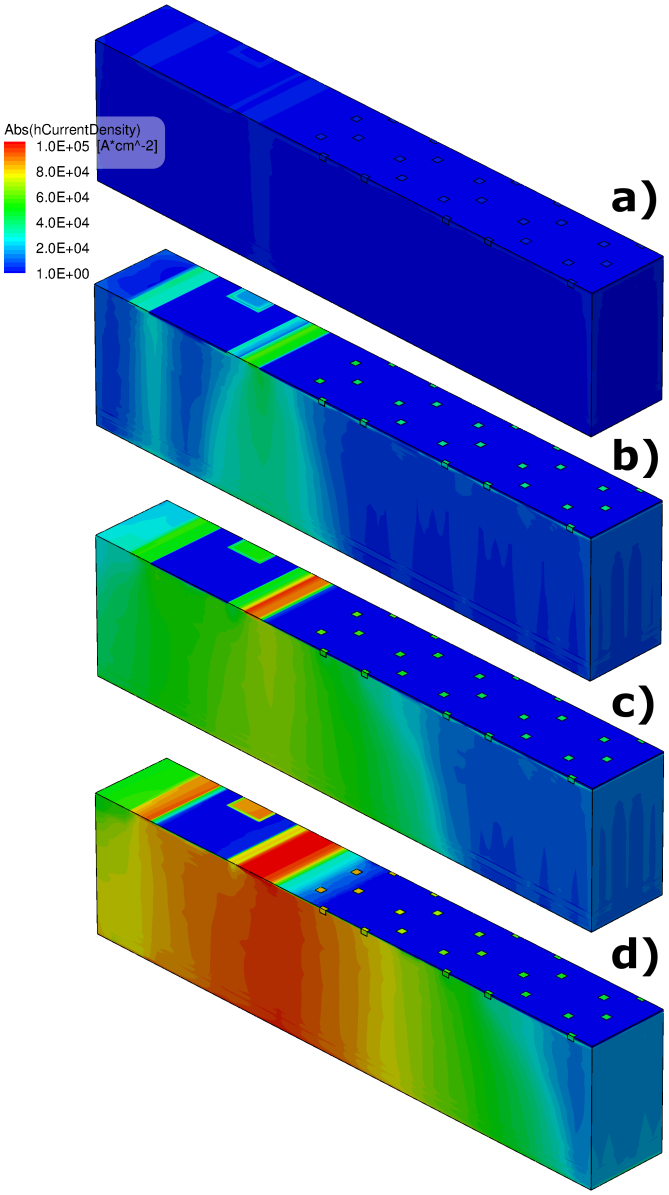

Fig. 7. Plots of hole current density during a *dV/dt* simulation of a PCT corresponding to time steps a), b), c), d) indicated in Fig. 6.

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