Electromigration in Solder Bumps: A Mean-Time-to-Failure TCAD Study

H. Ceric*†, W. H. Zisser†, M. Rovitto†, and S. Selberherr†
*Christian Doppler Laboratory for Reliability Issues in Microelectronics at the Institute for Microelectronics
†Institute for Microelectronics, TU Wien, Gußhausstraße 27-29, 1040 Wien, Austria
Email: {ceric|zisser|rovitto|selberherr}@iue.tuwien.ac.at

ABSTRACT

The mechanical and electrical properties of solder bumps influence the overall reliability of 3D ICs. A characteristic of solder bumps is that during technology processing and usage their material composition changes. This compositional transformation is enhanced by electromigration and leads to the formation of voids which can cause a complete failure of a solder bump. In this paper we present a compact model for prediction of the mean-time-to-failure of solder bumps under the influence of electromigration.

I. Introduction

Pure Sn has been identified as the best material for ultra fine pitch solder bumps for advanced three-dimensional interconnect applications due to its baseline advantages of being electrodeposited and exhibiting a low melting temperature. Many electromigration (EM) studies have been focused on the application of various combinations of under-bump-metallizations (UBM), solder compositions, and laminate surface finishes to reduce current crowding effects and improve reliability. An important feature of the EM failure mechanism in Sn-based solder bumps is its strong dependence on the Sn grain orientation [1]. Compared to Cu, Sn crystallization produces 100-1000 times larger grains. Correspondingly, the role of grain boundaries as fast diffusivity paths is much more pronounced. Sn solder bumps often consist of several large Sn grains, such that most solder bumps exhibit one or at most a few Sn grain orientations [2]. A clear dependence of the thermo-mechanical response of a Sn solder bump on microstructure and Sn grain orientation was also observed [2]. The coefficient of thermal expansion is higher in the c-axis direction than in the a- or b-axis directions. EM in Sn-based solder bumps is much more complicated than EM in Cu due to the presence of impurities [3]. In traditional EM studies, the devices under test are stressed to failure under a fixed temperature with a fixed current density. A typical EM failure is always enhanced with Joule heating so the exact time of the failure does not always reflect the process of EM progression under the set conditions. Also, time-to-failure measurement produces a broad distribution in results as the failure is associated with microstructural and compositional variations in the solder bumps. Failure analysis have shown that failures in Sn bumps occur by EM induced voiding at the interface between the intermetallic compound (IMC) and the solder. The development of a failure in a Cu interconnect takes place in two distinctive phases: a void nucleation phase and a void evolution phase [4]. During the first phase practically no resistance increase can be measured. The situation is quite different in the case of EM failure development in a Sn bump, where an IMC layer is also present [5]. From the beginning of EM stressing a continuous growth of the bump resistance (cf. Fig. 1) is observed. After a certain period of EM stressing, the bump resistance starts to rise with a significantly steeper slope. Chen *et al.* [5] assume that the two slopes of

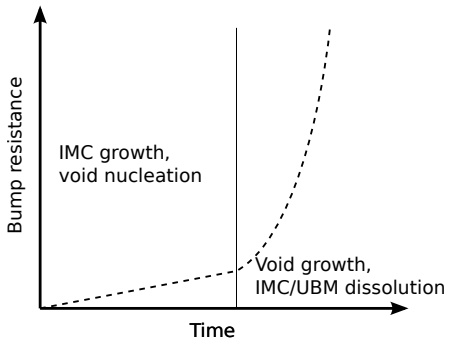

Fig. 1. Resistance change due to IMC growth and voiding with two different slopes.

the resistance growth represent two different stages of failure development: void nucleation combined with IMC growth and void propagation with IMC dissolution. The bump resistance increases due to void formation and microstructure changes during EM and can be precisely measured with Kelvin bump probes [5]. IMCs, such as Cu_6Sn_5 and Ni_3Sn_4, have a higher resistivity than pure Sn. In the case of Cu_6Sn_5, the resistivity is approximately 60% higher and in the case of Ni_3Sn_4, it is even 160% higher than the resistivity of Sn at room temperature. In our previous works we have studied the influences of the Sn anisotropy [6] and the influence of the intermetallic compound [7] on the EM failure. As a result of these studies, we have concluded that EM induced Sn vacancy transport is the dominating mechanism for the creation of void failure in solder bumps. The goal of the work presented here is to establish an accurate compact model for the prediction of the mean-time-of-failure of solder bumps by means of theoretical analysis and simulations.

II. Compact Modeling of Bump Failure

In the last decade some attempts have been made to investigate whether Black's equation can be used for the prediction of the mean-time-to-failure of solder bumps. For these investigations the standard form of Black's equations has been used [8]. While some authors have obtained a reasonable prediction of experimental mean-time-to-failure [9], others were forced to adapt the original equation in order to obtain good agreement [10]. Choi *et al.* [10] in their study of EM in

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eutectic SnPb and eutectic SnAgCu solder have adjusted the original equation to the form

$$t_f = \frac{A}{(cj)^n}\exp\Big(\frac{Q}{k(T+\Delta T)}\Big). \tag{1}$$

It is obvious that the coefficient c and the temperature increment ΔT in effect reduce the mean-time-to-failure t_f. The coefficient c is introduced to account for a local current density increase due to current crowding and ΔT includes an effect of Joule heating.

Both, the original work of Black [8] as well as the model of Shatzkes and Lloyd [11], which provides an explanation for Black's equation and its current density exponent, are considering only the one-dimensional problem of a straight aluminum strip. Besides the fact that they do not consider three-dimensional geometries of modern interconnect structures, they also do not take into account the mechanical stress and its interaction with EM, grain boundaries, and interfaces. These restrictions make the application of the Black's equation for studying solder bump EM failures highly questionable.

III. Analytical Solution of Korhonen

The model by Korhonen *et al.* [12] has already been successfully utilized for a derivation of EM compact models [13]. Compared to the above mentioned models [8], [11], Korhonen's model has a clear advantage, since it includes an influence of the microstructure and an effect of the mechanical stress. The central equation of Korhonen's model is

$$\frac{\partial\sigma}{\partial t} = \frac{\partial}{\partial x}\Big(\frac{D_a B\Omega}{kT}\Big(\frac{\partial\sigma}{\partial x} + \frac{|Z^*|e\rho j}{\Omega}\Big)\Big). \tag{2}$$

For a finite interconnect line of a length L with blocking boundary conditions on both ends of the line

$$J_v(0,t) = J_v(-L,0) = 0, \tag{3}$$

and for a constant diffusion coefficient D_a, the solution of (2) is given by

$$\sigma(x,t) = \frac{|Z^*|e\rho jL}{\Omega}\Big(\frac{1}{2} - \frac{x}{L} - S(x,t)\Big), \tag{4}$$

where

$$S(x,t) = 4\sum_{n=0}^{\infty}\frac{1}{\lambda_n^2}\exp\Big(-\lambda_n^2\frac{\kappa t}{L^2}\Big)\cos\Big(\lambda_n\frac{x}{L}\Big) \tag{5}$$

with $\lambda_n = (2n+1)\pi$ and $\kappa = D_a B\Omega/kT$.

The function $S(x,t)$ has two important properties. First, for a large t it converges to zero, which enables to obtain the equilibrium stress distribution from (4)

$$\sigma(x,t) = \frac{|Z^*|e\rho j}{\Omega}\Big(\frac{1}{2} - \frac{x}{L}\Big) \tag{6}$$

and secondly, for sufficiently large L and $x = 0$, it behaves like a simple function of time

$$S(0,t) \approx \frac{1}{2} - \frac{2}{L}\sqrt{\frac{\kappa t}{\pi}}. \tag{7}$$

By combining (4) and (7) we obtain an expression for the stress development at the end ($x = 0$) of a one-dimensional interconnect line

$$\sigma(x,t) = 2\frac{|Z^*|e\rho j\pi}{\Omega}\sqrt{\frac{\kappa t}{\pi}}. \tag{8}$$

Equation (8) is a convenient reference for an initial guess in designing of a compact model because of two reasons:

- It analytically describes a stress behavior in time. Reaching of certain stress threshold is a usual condition for EM void nucleation [14].
- It implicitly considers large size interconnects.

IV. Modeling of Vacancy Electromigration

Vacancy EM has been well investigated and successfully modeled by different authors starting with the work of Sarychev *et al.* [15]. Today we have comprehensive and sophisticated EM models which include the gradients of the vacancy concentration, mechanical stress, and temperature as driving forces with tensorial diffusivity for modeling the material anisotropy. One such model, systematically presented in [16], is applied here for the development of a compact model of EM failure in solder bumps.

V. Results and Discussion

A. Full Physical Simulations of EM in Solder Bumps

We have applied the full EM physical model [16] for studying of EM in three solder bumps with the same geometric features but different diameters of $2R = 50\mu$m, $2R = 70\mu$m, and $2R = 90\mu$m. The top and the bottom of the spherical bump structure contacts the UBM layer and the Cu layer, respectively, with a circular interface with a radius $r = 3R/4$.

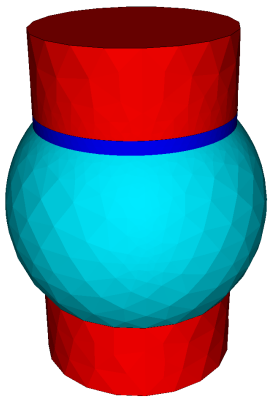

Fig. 2. Solder bump geometry used for the simulation. On the top of the Sn bump, a Ni UBM layer is placed.

In all simulated cases a characteristic stress distribution at the top of the solder bump is obtained as can be seen in Fig. 3. The mechanical stress increases from the periphery towards the center of the bump/UBM interface which leads us to the conclusion that a void most probably nucleates in the center of the interface. From the simulation results we see that for the larger bump (2R=70μm, Fig. 4), a shorter time

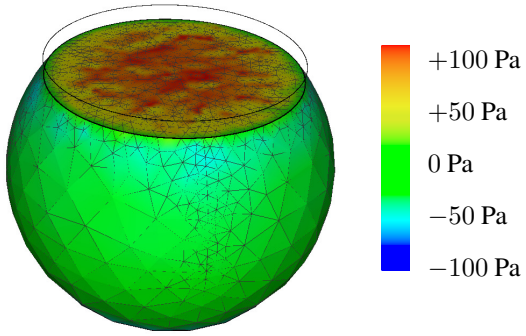

Fig. 3. Stress distribution at the top of solder bump beneath the UBM.

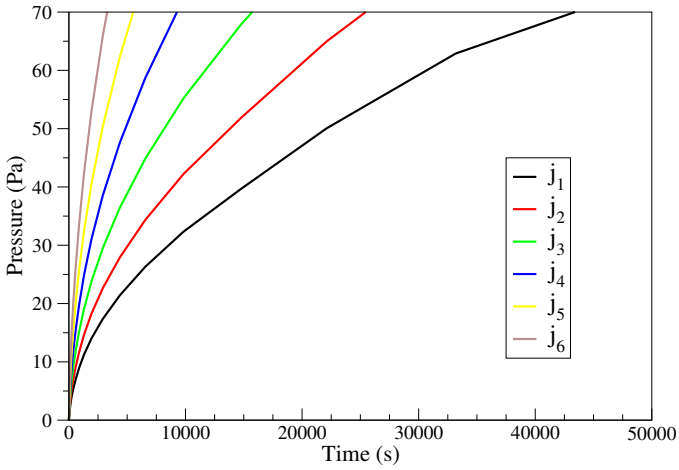

Fig. 4. Stress development in the 70μm bump for 6 different current densities $j_1 < j_2 < j_3 < j_4 < j_5 < j_6$.

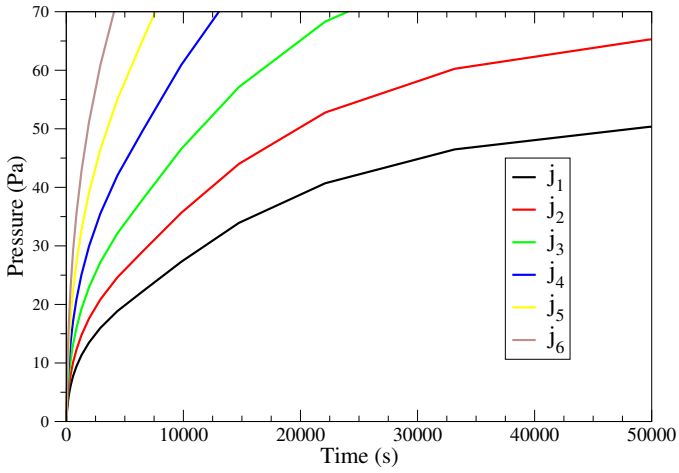

Fig. 5. Stress development in the 50μm bump for 6 different current densities $j_1 < j_2 < j_3 < j_4 < j_5 < j_6$.

is needed to reach the given stress threshold (70 Pa) than for the smaller bump (2R=50μm, Fig. 5). This implies that for the larger bump EM induced material transport is more efficient, since it has more vacancies available in a cross section of the bump. The observed behavior is more pronounced for smaller current densities.

B. Extension of Korhonen Model

For deriving an expression for the mean-time-to-failure t_f it is important to define a failure condition. While the ultimate failure condition of any interconnect is an increase of its resistance, the question is which physical condition must be fulfilled for an initialization of the rapid phase of failure development - void nucleation. According to our previous work [7], [17], in the case of solder bumps, we have to consider two effects:

- Stress voiding [14]
- Kirkendall voiding [18]

It is plausible to assume that mechanical stress will either alone initialize void nucleation or enhance Kirkendall voiding. In this study we confine ourselves to the condition of stress voiding. The stress threshold σ_c in Korhonen's model is attained by a stress build-up along the one-dimensional interconnect. In the case of a three-dimensional geometry we have more vacancies available in the cross section of the bump so, $\sigma \sim jR^2\sqrt{t}$. From (8) and by setting $A = kT\pi\Omega/((e|Z^*|\rho)^2 BD_a)$ we obtain

$$t_f = \Big(\frac{A}{j^2}\Big(\frac{\sigma_c}{\alpha R^2+\beta}\Big)^2 + \frac{B}{j}\Big)\exp\Big(\frac{E_a}{kT}\Big). \qquad (9)$$

The parameters α and β are obtained by fitting to the results of the full physical simulations (cf. Fig. 4 and Fig. 5). While the first term on the right side gives a mean-time-to-failure contribution prior to void nucleation, the second term represents the time of void evolution characterized by the parameter B. In Fig. 6 we show the comparison between the mean-time-

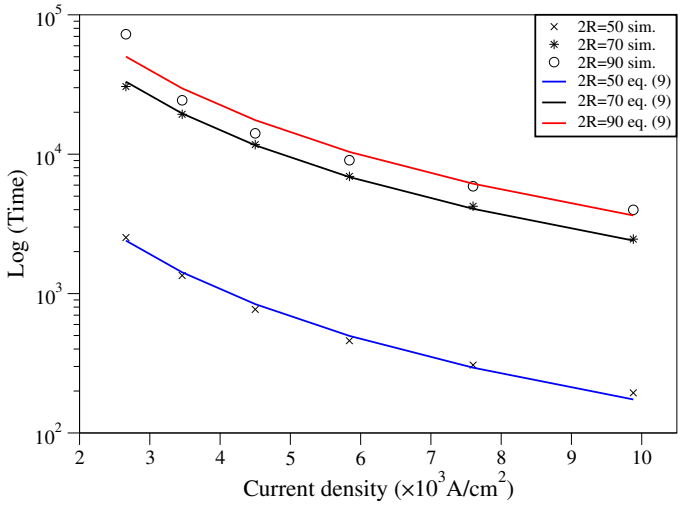

Fig. 6. Time to failure dependence on current density for three different bump sizes.

to-failure obtained by (9) and the full physical model [16] for three different bump radii. For all three different bump sizes a good agreement is obtained. In the studied cases, the void evolution time is assumed much smaller than the void nucleation time (the first summand), e.g. the void development leading to complete failure is very rapid.

C. Void Growth and the Resistance Change

The determination of the parameter B in (9) requires simulations of the evolving void surface, which are performed by the phase field model [19]. In these simulations, current crowding in the vicinity of the void (cf. Fig. 7) influences the development of the void shape which in turn determines the resistance increase of the solder bump (cf. Fig. 8).

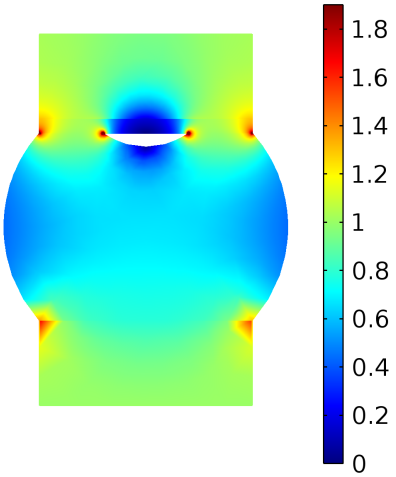

Fig. 7. Current density distribution (10^3A/cm^2) in the presence of the void nucleated at the interface between the bump and the UBM.

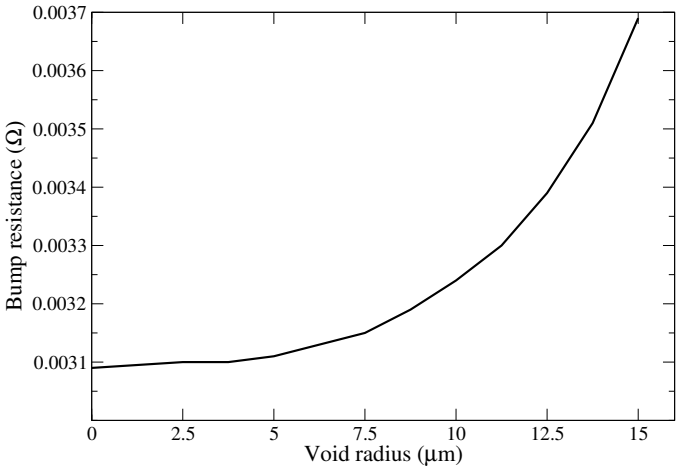

Fig. 8. Increase of bump resistance caused by the growing void.

VI. Conclusion

In this work we have presented an analytical compact expression for the estimation of a mean-time-to-failure of the solder bump. For this purpose we have used a full physical three-dimensional model to simulate EM and mechanical stress driven dynamics of vacancies in Sn solder bumps. When inside the bump a certain stress threshold is reached a void is nucleated and a rapid phase of failure development is initialized. Our compact model for the mean-time-to-failure is designed by an adaptation of Korhonen's model and it is verified and calibrated through comparison with current density/mean-time-to-failure curves obtained by simulation. In addition, the effect of a void growing inside the solder bump on its electrical properties is investigated. The presented methodology is general in nature and can be used for the further refinement of EM compact models.

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