Compact Modeling for the Changing Transistor

(Plenary Paper)

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***Abstract*—Compact model is not only a tool for IC design but also the unique bridge between IC manufacturing and design. It needs not only a mathematical model of a prototype transistor but also accurate models of many real device effects of the modern transistor. Compact model can address not only circuit performance but also reliability. BSIM and BERT are used as examples.**

Keywords—compact model, SPICE, MOSFET, FinFET, reliability

I. INTRODUCTION

Design companies need two things from their foundry partners to design integrated circuits -- design rules and SPICE model (also known as "compact model"). Design rules are created by each fab. Today, the SPICE model, which is a set of long equations that reproduces the exact transistor characteristics for SPICE simulation, is likely a free industry standard model.

The compact model is effectively a "contract" between the wafer fab and the IC design designer. "First wafer success" has become the norm in the past dozen years in spite of rising technology and circuit complexity. That is partly due to the improved accuracy of the compact model. If the model does not describe the transistor characteristics accurately, design effort cannot guarantee success. The model equations contain adjustable parameters. Engineers, with the help of automated parameter optimization tools, choose the parameter values so that the BSIM model accurately reproduces the current, capacitance, and noise over many orders of magnitude covering all working terminal voltages, gate lengths and widths, and temperatures. This process is known as model parameter extraction.

With the CMOS technology scaled aggressively and short channel effects becoming dominant and critical to circuit design, the need for sophisticated and accurate MOSFET models keeps growing. A model must be very accurate to avoid expensive design re-spin, very fast to support simulation of large circuits, and robust for convergence in a wide range of complex circuits (Fig. 1).

The compact model may be used with SPICE to simulate and design circuits directly. Or it may be used with "fast SPICE", which achieves order of magnitude speed up over SPICE with some loss of accuracy and may use the compact model to construct a table look-up model.

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II. BSIM -FIRST INDUSTRY STANDARD MODEL

BSIM stands for Berkeley Short-channel IGFET Model. IGFET (insulated-gate field effect transistor) is an old name for MOSFET. BSIM is the first industry standard model and continues to be the most popular compact model today. BSIM's genesis may be traced to BSIM1 published in 1984 [1], which was followed by BSIM2 in 1988[2].

At the same time we had a much larger and very productive research effort in MOSFET physics and technology. Our research into the many devices physics effects and behaviors of aggressively scaled MOSFETs gradually built a collection of models for V_t dependence of bias and gate length, mobility degradation, velocity saturation effect, output conductance, unified flicker noise theory, etc. Eventually, these models became the building blocks of later BSIM models. The research on the hot carrier reliability led to the first reliability compact model BERT (see section on compact reliability model below).

BSIM3 incorporated some of the new original device physics models. That approach was a marked departure from all previous compact models including BSIM1, 2. Those models used simplistic device physics and relied heavily on inventing equations to “curve fit” the nuances in the transistor data.

BSIM3 was such an improvement over the previous models that the Compact Model Council, an industry standard organization formed in 1995 selected BSIM3v3 as the world's first industry standard model. Soon after, it replaced many dozens of SPICE models in use in 1995. BSIM has been provided by UC Berkeley to users worldwide royalty free following the tradition of the Berkeley SPICE.

III. SIMPLE AND REAL DEVICE MODELS

All compact MOSFET models start with a "simple model" that represents a prototype long channel transistor. The accuracy is achieved by adding numerous "real device models" as shown in Fig. 2. BSIM excels because of its accurate real-device models. For example the output resistance used to be

modeled with Early voltage as a constant. BSIM3[3] introduced three separate mechanisms — channel length modulation, drain-induced barrier lowering and hot carrier induced body bias effect. Each of these three mechanisms is modeled with a nonlinear multi-variable function of channel length oxide thickness, Vt, Vds, Vgs, and Vbs. Accurate output resistance model is very important for analog circuit design and the BSIM output conductance model was an instant success and continues to be used today.

Another example is the gate-induced-drain-leakage or GIDL. We discovered this new leakage current and explained it as the band-to-band tunneling current induced by the gate-to-drain voltage[4]. Once the mechanism was clearly understood, a simple analytical model was introduced and it proved to be very accurate.

Yet another example is the flicker noise or 1/f noise. The unified flicker noise model incorporates both the fluctuation in the number of inversion layer carriers (number fluctuation) and the fluctuation in the Coulombic scattering mobility (mobility fluctuation). We showed that they are correlated because both are caused by the fluctuation in the number of trapped charge in the SiO2 near the silicon/SiO2 interface [5]. We validated the model in detail using the random telegraphic noise measurements that can only be observed in transistors with such small length and width that transistors may contain only one or two oxide trap. These physic studies led to an accurate BSIM Unified Flicker Noise Model.

Even more complex real device models include the self-heating model, and floating body model first introduced by BSIM-SOI and the non-quasi-static model.

The real device models account for 80-90% of model code, simulation time and global accuracy of real transistor modeling.

IV. THE CHANGING TRANSISTORS

Through device physics research, I recognized that the subthreshold current does not have to flow along the silicon-dielectric interface. The subthreshold current density may peak many nm below the interface and leakage paths far from the gate are responsible for short gate transistor leakage. To address this root cause of the leakage power problem, I proposed two device structures in 1996 in response to a DARPA request for proposal entitled "Sub-25nm Switches". They are FinFET[6] and Ultra-Thin Body (UTB) SOI[7]. Both of them eliminate leakage paths that are far from the gate.

Making the thickness of the transistor body, whether a fin, a film, or a wire (see Fig. 3), small in comparison with the gate length suppresses the subthreshold current and can support MOSFET scaling to the end of lithography. Channel doping is not needed for suppressing the short channel effects. Thus random dopant fluctuation, a major contributor to device variation, is eliminated.

FinFET's body is a thin fin. The fin may take a nanowire shape and puts the body under more effective control of the gate [8]. UTB FET's body is a thin film (on dielectric) that is only several nm thin.

Most compact model research today concentrate on solving Poisson equation to derive "simple models" for transistor with new device shape, e.g. FinFET, but long channel length. However, the real need is accurate "real device models" of the new transistors. Examples are the leakage current model for high-k metal gate stack, quantization effect in small structure, tunneling in small transistors, transistors of complex real shapes, not simple and ideal shapes.

Fig. 4. shows some examples of the global accuracy of FinFET modeling achieved by good Real Device models. Accuracy at this level is required to support advanced analog and RF circuit design. Fig. 5 shows another challenge of FinFET modeling. How can real FinFETs from various manufacturers having quite different and irregular fin shapes be modeled with one FinFET standard model? The answer can be found in another paper at this conference [10].

V. COMPACT RELIABILITY MODEL

Our hot carrier injection reliability research led to the first compact reliability simulator. BERT [11] eventually also contained reliability models for oxide wearout, AC electromigration and BJT degradation. Today all major EDA companies offer products based on the BERT framework for hot carrier instability and NBTI, PBTI instability. Reliability compact models also rely on physics based analytical equations and parameters extracted from DC stress test to predict circuit behavior---in this case, reliability (Fig.6). Fig. 7 shows an example of predicting the speed degradation of a micro processor during a 1000 hr life test.

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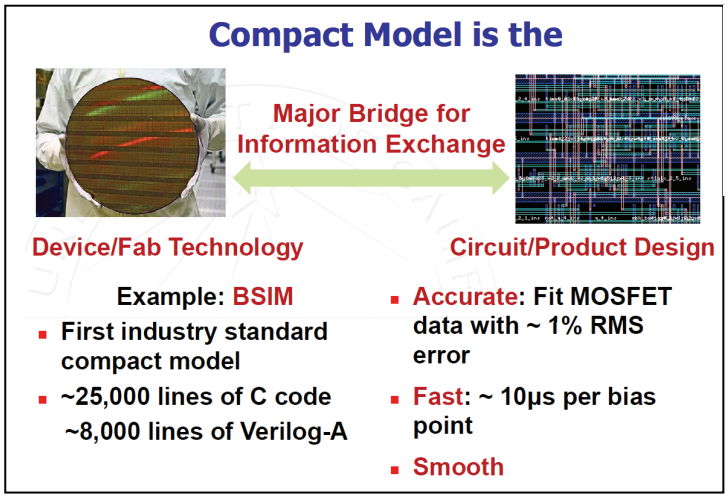


Fig.1. Complex device and manufacturing technologies determine the electrical behaviors of a transistor. Compact model captures this information and makes it available for IC circuit and product design.

Fig. 2. A Compact model is a Simple (long channel) Model and numerous Real Device Models. The latter is 90% of the model and responsible for the global accuracy.

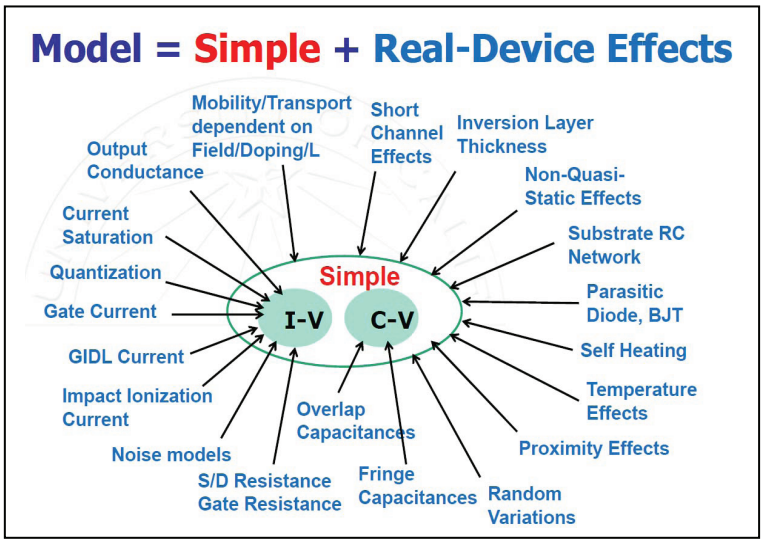
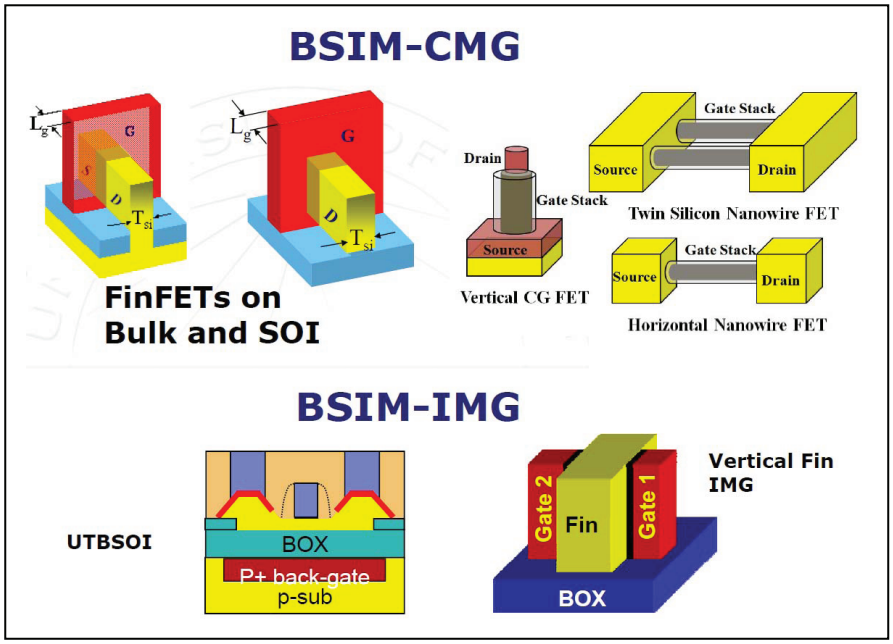


Fig. 3. Common multi-gate (CMG) model allows a single gate voltage, while independent multi-gate (IMG) model supports two independent voltages.



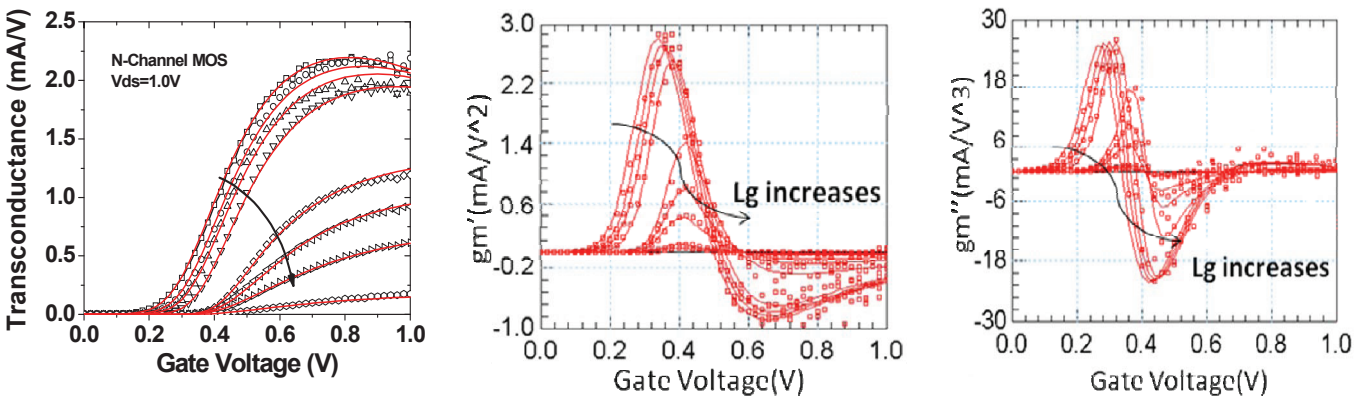


Fig.4. BSIM-CMG accurate captures not only Id and its derivative, gm (left), but also the derivative of gm, gm' (middle), as well as gm'' (right) of FinFETs with channel lengths ranging from 30nm to 10um. Such global accuracy can only be achieved with accurate Real device Models. [9] Curves: BSIM-CMG, Symbols: Measured FinFET data.

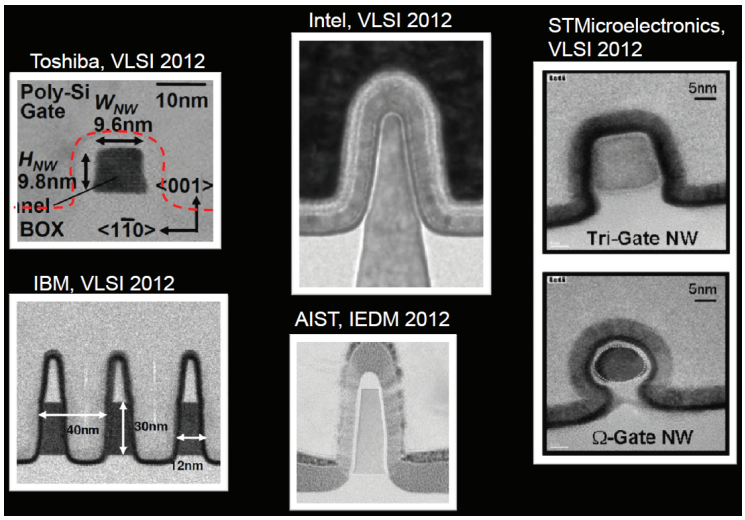


Fig. 5. The fin shape of real FinFET vary from one manufacturer to another and have rounded corners and manufacturing variations. A unified model can model all these. [10]

$$Degradation = f(Age)$$

$$Under\ DC\ Test:\ \ Age = \frac{I_{ds}}{kW}\left[\frac{I_{sub}}{I_{ds}}\right]^{m} t$$

$$interface\ quality \qquad = \varphi_{it}/\varphi_{ii} \sim 2.9$$

$$In\ Circuit:\ \ Age = \int \frac{I_{ds}}{kW}\left[\frac{I_{sub}}{I_{ds}}\right]^{m} dt$$

Fig. 6. BERT, the first reliability simulator introduced physics based accurate yet simple hot carrier aging model. The model has only two parameters that can be extracted easily from DC stress test. Circuit aging can be predicted using this model, SPICE, and BSIM [11].

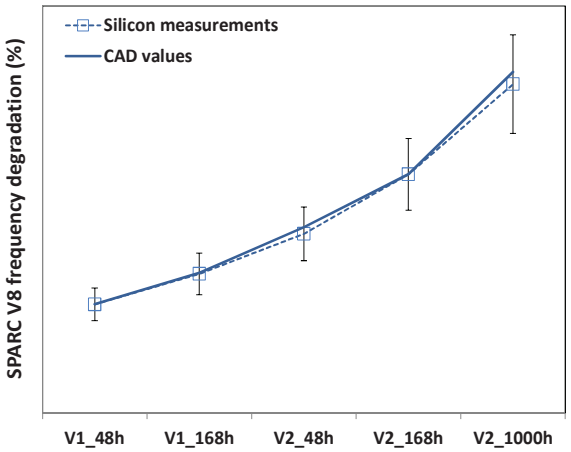


Fig. 7. Compact reliability model accurately predicted the speed degradation of a 32bits SPARC V8 LEON3 microprocessor during a 1000hr life test [12].