PDK development for 10nm III-V/Ge IFQW CMOS technology including statistical variability

Si-Yu Liao, Ewan A. Towie, Daniel Balaz, and Craig Riddet
[1]Device Modelling Group, School of Engineering
University of Glasgow
Glasgow, Scotland, United Kingdom
Siyu.liao@ymail.com

Binjie Cheng[1,2], and Asen Asenov[1,2]
[2]Gold Standard Simulations Ltd. and
University of Glasgow
Glasgow, Scotland, United Kingdom
asen.asenov@glasgow.ac.uk

***Abstract*— From 3D Monte Carlo and drift diffusion TCAD simulations to compact models, we develop an early PDK of 10nm CMOS node technology employing co-integration of 15nm physical channel length III-V and Ge transistors. By taking into account the statistical variability, reliable predictions of the impact of variability on circuit performance and yield can be delivered to achieve variation aware design.**

Keywords—III-V, Ge, CMOS, Statistical Variability, Compact Model, SRAM, Variation-Aware Circuit Design.

I. INTRODUCTION

The 2012 edition of the International Technology Roadmap for Semiconductors (ITRS) has included III-V/Ge based CMOS technology into the "Process, Integration and Devices" and "Front End Process" areas, marking it for possible utilization at and beyond the 10nm technology generation [1]. To derive the best benefits from the enhanced transport properties of the above materials, the Implant-Free Quantum-Well (IFQW) transistor architecture has been proposed, offering simultaneously high channel mobility and drive current along with excellent electrostatic integrity [2], [3]. In this work, a preliminary process design kit (PDK) for the III-V/Ge CMOS 10nm technology has been developed, with the special emphasis on the capture of the statistical variability (SV) for variability aware designs, as the SV has been known as a major issue for advanced CMOS circuits [4]. The full PDK development flow is illustrated in Fig.1.

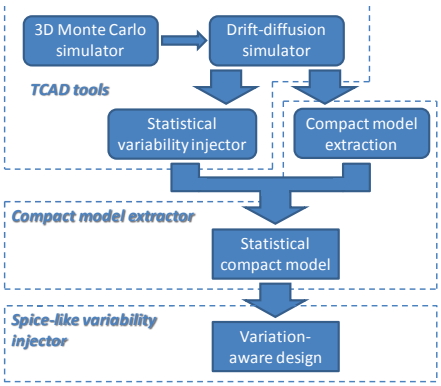

Fig. 1. Diagram of the 10nm III-V/Ge IFQW MOSFET PDK development flow including statistical variability.

A previous IFQW MOSFET structure was designed for the 20 nm CMOS technology and reported by Benbakhti *et al.* [5], [6]. In this work we have designed transistors for the 10 nm CMOS technology generation transistors following the ITRS guidelines [1] and employing $In_{0.53}Ga_{0.47}As$ and Ge as channel materials for the n- and p-channel transistors respectively, with a common high-κ Al_2O_3 gate oxide and a metal gate as shown in Fig. 2. The IFQW transistor utilizes a 3.75nm thick $In_{0.53}Ga_{0.47}As$ QW channel grown on an $In_{0.52}Al_{0.48}As$ substrate and epitaxial in-situ doped raised source and drain. The source and drain regions are doped to $N_D=9.1\times10^{19}cm^{-3}$, the channel doping is $N_A=1.82\times10^{17}cm^{-3}$ and the substrate doping is $N_A=3.65\times10^{18}cm^{-3}$. The gate oxide is Al_2O_3 with an EOT=0.51nm (t_{ox}=1.125nm), and the lateral spacers are Si_3N_4 with a spacer width to be optimized by TCAD simulations. A sub-diffusion of doping into the channel layer has been introduced to enhance the drain current.

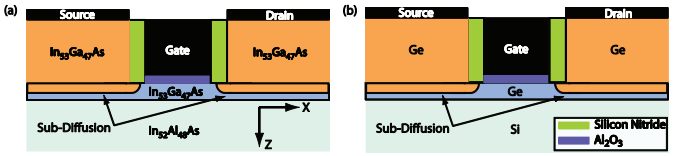

Fig. 2. Schematic of the IFQW MOSFET structure with sub-diffusion, (a) the III-V nFET, (b) the Ge pFET.

II. 3D TCAD TOOL DEVELOPMENT

A. 3D Monte Carlo simulators

This device architecture design has been optimized based on the simulation of the Monte Carlo (MC) module of the GSS TCAD simulator GARAND [7]. The simulator captures the non-equilibrium quasi-ballistic transport effects, includes Fermi-Dirac statistics (FD) as well as quantum corrections using the density gradient approach, and allows for accurate estimation of the on-current at high drain bias [8], [9]. The width of the Si_3N_4 lateral spacers has been determined by the MC module to be optimal at a width of 2nm which yields a good balance between the high drive current and technological feasibility [8], [9]. Fig. 3 shows the transfer characteristics obtained by the MC simulator for the optimized device structure, with supply voltage at 1.0V.

To conduct the SV investigations of this architecture, multiple ensembles of at least 1000 devices are required

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meaning that computational efficiency is of considerable importance. Therefore, the mobility models in the drift diffusion (DD) module of GARAND have been tuned to match the device behavior predicted by the MC simulations and this has been employed to undertake the SV study, thus reducing the computational burden while accurately representing the charge transport in the device.

B. Drift-diffusion simulator calibration

The three major components of the mobility models that have been calibrated to MC results are: the doping concentration dependent mobility, the lateral electrical field dependence along the channel, and the perpendicular field dependence which is related to the gate bias. An automatic calibration strategy is used to fit selected parameters in the mobility models to produce a good agreement with the MC results. Here we have calibrated our simulator over a wide bias range. Fig. 3 shows the mobility calibration of the DD simulations against the MC data for the nominal n-type and p-type devices. An excellent agreement is observed for the high gate bias as well as the subthreshold behavior.

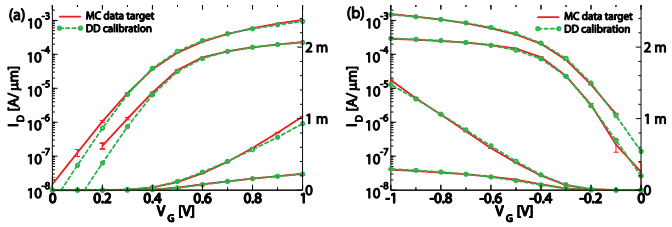

Fig. 3. 3D MC and DD TCAD simulation results of (a) the III-V nFET, (b) the Ge pFET.

Having calibrated the DD simulator, the nominal devices metal gate work function is adjusted to achieve the design target of the V_{TH} = 0.2V under the constant current criterion of I_{DS} = 100nA. The nominal devices performances at room temperature are: I_{ON} = 1137μA/μm and 1401μA/μm; subthreshold swing (SS) = 91.5mV/decade and 93.9 mV/decade; and the drain induced barrier lowering (DIBL) = 106.4mV/V and 75.5mV/V for the n and pFET, respectively.

The temperature dependence of the InGaAs and Ge mobilities has been captured through matching to experimental data in the DD simulator of both Caughey-Thomas and Lombardi mobility models [12], [13], [14], allowing the TCAD tools to be applied for the operation temperature range from 270K (-3ºC) up to 390K (117ºC)

III. Compact Model Parameter Extraction

The compact model is an important part of the PDK in extracted based on target characteristics generated using the calibrated TCAD tools. To properly capture the circuit and device behavior of IFQW MOSFET, the industry standard compact model BSIM4 is selected for the compact model parameter extraction.

The nominal compact model extraction is carried out with the GSS extractor, Mystic [17]. The key BSIM parameters are extracted in an extraction strategy based on 5 stages. The parameters include: *vth0, voff , nfactor, minv, k1, k2, ua, u0, uc, rdsw, vsat, pdiblc2, a0, ags, pvag, delta, cdsc, eta0, etab, prwb.* The aim is an accurate representation of the key transistor's figures of merit including the threshold voltage, off current, SS and DIBL as well as the drive current. In terms of the I_D-V_G and I_D-V_D characteristics, the errors in the extracted nominal compact model at room temperature are 0.82% and 1.51% for the nIFQW and pIFQW respectively for V_{DD} up to 1V as shown in Fig 4.

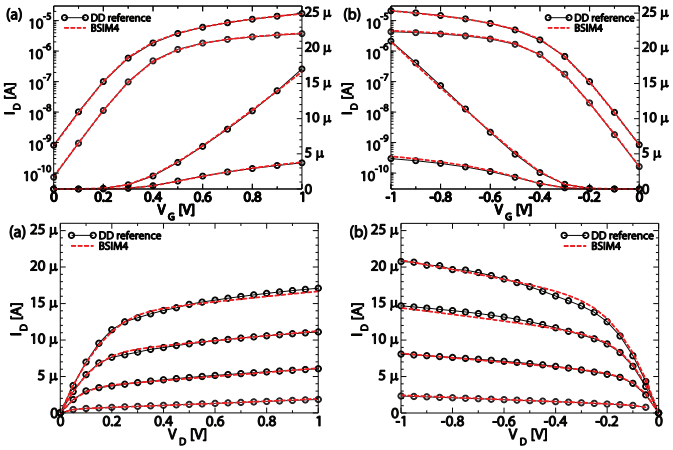

Fig. 4. BSIM 4 compact model extraction: transfer characteristics of (a) the III-V nFET, (b) the Ge pFET, $|V_D|$=0.05V and 1V. I_D-V_D of (a) the III-V nFET, (b) the Ge pFET, V_G from 0.4V to 1V.

The nominal compact model extraction is extended to cover the device operation temperature ranging from 270K to 390K. Then a 5-stage inverter ring oscillator circuit using these model cards is simulated to study the impact of the operating temperature on the inverter's delay. The propagation time of a single inverter increases from 16.9ps to 18.5ps as the device operating temperature increases from 270k to 390K.

IV. Statsitiscal Variability Investigation

The impact of SV has been previously highlighted for ultimately scaled silicon MOSFETs including their impact on circuit performance [4]. It is vital to capture the effect of SV in our PDK to facilitate variation-aware circuit design.

Several important SV sources are implemented in the DD 'atomistic' module of GARAND including random discrete dopant (RDD), line edge roughness (LER), and metal gate granularity (MGG). Here we assume a gate last procedure in the fabrication technology, which minimizes MGG, and therefore only RDD and LER are considered in the SV evaluation. LER is modeled here using 3σ=2nm and Λ=30nm. Ensembles of 1000 transistors for both n- and p-type IFQW transistors are simulated in order to examine each SV source. Fig. 5 presents the impact of the SV sources on the threshold voltage and the drive current, showing that RDD dominates the variation of device performance in the 10nm III-V/Ge IFQW MOSFET technology - similar observations have been reported for Si CMOS SV studies [18], [19]. The SV simulation results are then used to create the associated statistical compact models.

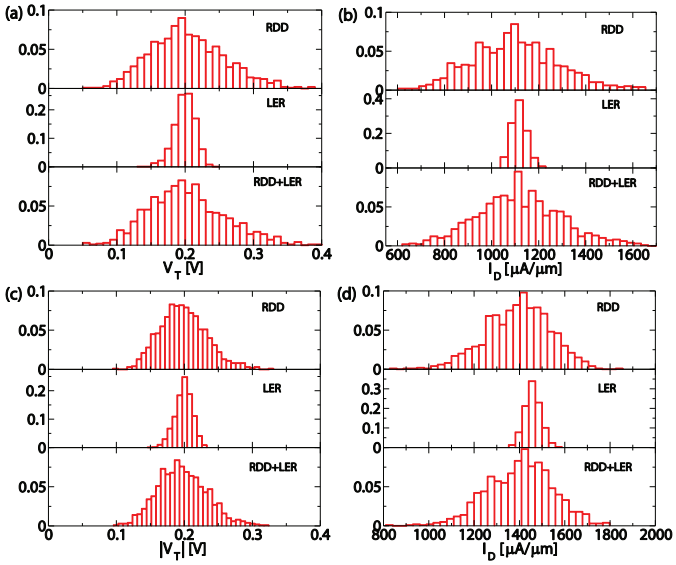

Fig. 5. Statistical variation histogram of threshold voltage and drive current at V_D=1V for (a) and (b) the III-V nFET, (c) and (d) the Ge pFET.

V. Statistical Compact Model

The statistical compact model captures the impact of the SV on device performance simulated by TCAD tools using statistical model parameter cards. To create the statistical compact model, the extracted compact model parameters of the nominal devices are used as the initial values. Then a similar statistical compact model extraction strategy reported by Cheng *et al.* is utilized [15]. Focusing on the device I_D-V_G transfer characteristics, 8 parameters related to the variability sources RDD and LER are selected to be extracted: *Vth0*, *U0*, *Minv, Nfactor*, *Rdsw*, *Vsat*, *eta0*, and *Voff*.

The accuracy in representing individual device characteristics and figures of merit under the influence of statistical variation depends on the number of statistical parameters used during the statistical compact model extraction. Statistical parameters are selected, in an order following their statistical significance, to form the parameter sets of different sizes (1 to 8 parameters). Due to the increasing importance of standby power dissipation in low power IC design, we treat I_{OFF} and I_{ON} equally during statistical extraction and the RMS errors used in both the sub-threshold and on-current regimes are calculated on a linear scale. Figs. 6 (a) and (b) show the distributions of RMS errors calculated for the statistical extraction from the simulation of 1000 statistically different nIFQW and pIFQW MOSFET devices. The distributions demonstrate how the number of parameters that are re-extracted affects the accuracy of the statistical compact model cards when compared to the original simulation data from which they are extracted.

To summarize the distributions of the statistical compact modeling accuracy, the reduction of mean and standard deviation of RMS error against the increase of size of parameter set is illustrated in Fig. 6 (c) and (d). Assuming a Gaussian distribution, the mean of the RMS errors μ is reduced from 14.5% with a 1-parameter set, to 3.7% for an 8-parameter set, and the standard deviation σ is reduced from 6.8% with a 1-parameter set, to 1.7% for an 8-parameter set, for III-V nIFQW devices while for Ge pIFQW devices, μ is reduced from 10.5% to 2.7%, and σ is reduced from 5.1% to 1.2%.

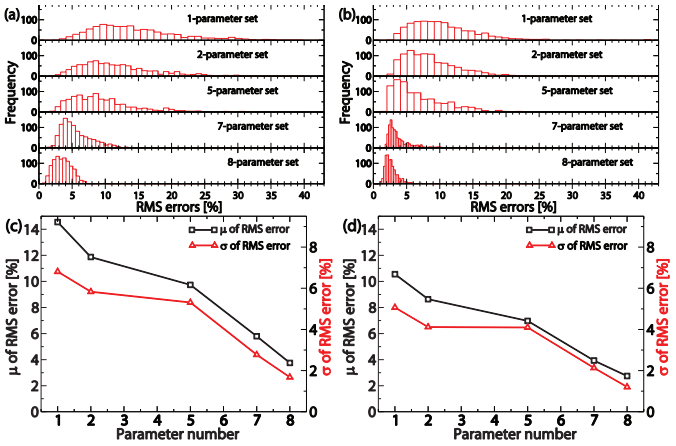

Fig. 6. Distribution of RMS errors between the extracted statistical compact models and the original DD TCAD data for the 1000 devices simulated for the 15nm IFQW MOSFET devices, (a) the III-V nFET, (b) the Ge pFET. Mean and standard deviation in the RMS error of the extracted statistical compact models versus the size of the statistical parameter set, (c) the III-V nFET, (d) the Ge pFET.

VI. Variation-Aware SRAM Design

The extracted compact model cards and statistical compact models are built as a statistical device library and implemented in the GSS RandomSpice simulator for the preliminary variation-aware basic circuit evaluation [16]. To minimize the impact of the SV on the SRAM cell performance, an optimized minimal device dimension 6T-SRAM design is evaluated with the transistor gate width defined as multiples of 15nm. The ratio between the gate width W and the gate length L is different for each of the groups of transistors: i) for pull up (PU) pIFQW transistors, W/L = 1, gate width = 15nm; ii) for pass (PA) nIFQW devices, W/L = 3, gate width = 45nm; iii) for pull down (PD) nIFQW devices, W/L = 4, gate width = 60nm. This cell dimension configuration is noted as 1-3-4. RandomSpice can randomly generate device models from the statistical library for a large number of circuits in the Monte Carlo circuit simulation. For instance, in a 1-2-3 6T-SRAM cell, 12 different minimum size transistors need to be generated in one circuit.

Performing the circuit Monte Carlo simulation with the extracted statistical compact model library, 1000 stable SRAM cells with 1-3-4 configuration is observed for both read and write operations as shown in Fig. 7 (a), and (b). Fig. 7 (c) reveals that the statistical static noise margin (SNM) varies from 0.12V to 0.3V with an average of 0.226V and standard deviation of 25mV. The write noise margin (WNM) mainly varies from 0.3V to 0.6V with average of 0.453V and standard deviation of 51mV.

Using the optimized minimal-sized SRAM cell design, an estimation of cell fail rate for one million SRAM cells taking into account the SV are made based on the 1000 simulated cells for both SNM and WNM as shown in Fig. 8. The generalized lambda distribution plots allow the estimation of

the rate with a known data retention voltage. With our estimated function, a SNM of 0.1V and a WNM of 0.25V of the minimal-sized SRAM cell design delivers a fail rate less than 100 per million.

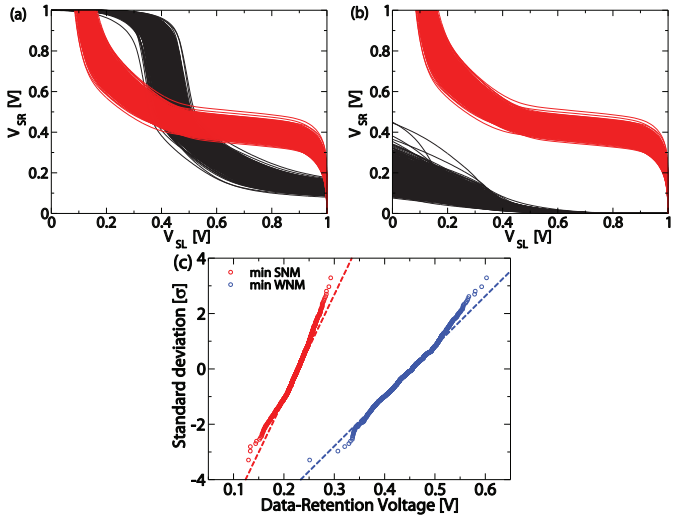

Fig. 7. Statistic output characteristics of 1000 SRAM cells in configuration 1-3-4 ($W_{Pull\ Up}$=15nm, W_{Pass}=45nm, and, $W_{Pull\ Down}$=60nm), (a) for read, (b) for write. (c) Static noise margins and write noise margin of 1000 SRAM cells in configuration 1-3-4.

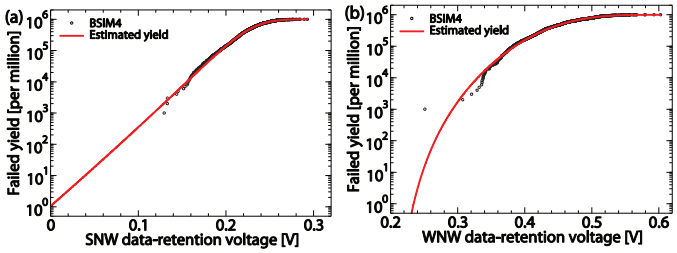

Fig. 8. Statistic output characteristics of 1000 SRAM cells in configuration 1-3-4 ($W_{Pull\ Up}$=15nm, W_{Pass}=45nm, and, $W_{Pull\ Down}$=60nm), (a) for read, (b) for write. (c) Static noise margins and write noise margin of 1000 SRAM cells in configuration 1-3-4.

VII. Conclusion

We have developed a TCAD based PDK for a 10nm generation III-V/Ge MOSFET CMOS technology that accurately captures the statistical variability to facilitate the variation-aware design. The PDK is based on 3D MC simulations and calibrated DD simulators, which maintain computational efficiency without a trade-off on accuracy and are used to assess the impact of SV in these architectures. Based on the TCAD results, a statistical BSIM4 compact model has been built for this technology. An optimized minimal sized SRAM cell has been designed and evaluated using the extracted statistical compact model to estimate the cell fail rate.

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