# A TCAD Study of Substrate Dopant for Extremely Thin SOI MOSFETs with Ultra-Thin Buried Oxide

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*Abstract*—**In this paper, the effects of dopant distribution in substrate/ back-gate, back bias and metal gate work-function on performance and Vt roll-off of Extremely-Thin Silicon-On-Insulator (ETSOI) MOSFETs with Ultra-Thin Buried OXide (UTBOX) (ES-UB- MOSFETs) were simulated and studied. Lateral Non-uniform Dopant Distribution (LNDD) in substrate was used to enhance scaling capability and improve Vt controllability for ES-UB- MOSFETs. Process and device simulations were conducted to demonstrate the importance of substrate dopant engineering and to search the optimization design conditions for ES-UB-MOSFETs. Fixing long channel Vt at ±0.3V for ES-UB-MOSFETs, LNDD enables gate length to be scaled to 20nm for both n- and p-MOS, which is ~ 10% smaller than that of the ES-UB-MOSFETs with lateral uniform doping in substrate. A novel process flow to form LNDD was proposed and simulated.**

***Keywords-Fully depleted SOI (FDSOI), extremely thin SOI (ETSOI), ultra thin BOX (UTBOX), short channel effect, ground plane, lateral non-uniform dopant distributions, MOSFET, back bias, work-function***

## I. INTRODUCTION

The Extremely Thin SOI with Ultra-thin BOX MOSFETs (ES-UB- MOSFETs) is a viable option for continued CMOS scaling owing to its superior short-channel control, inherent low device variability due to undoped channel, good process compatibility with mainstream planer CMOS and controllability of back gate[1-3]. There is a need for systematical investigation of effects of dopant distributions in substrate/back-gate, work-function and back bias (Vbb) on ES-UB-MOSFETs' performance and Vt roll-off. In order to obtain proper saturation threshold voltage (Vt-sat) for short channel ES-UB- MOSFETs, Vt-sat is too high for long channel devices[3]. In this case, it is difficult to reduce power consumption and keep high performance by scaling down power supply (Vdd). On the other hand, as shown in Fig.1, if the Vt-sat of long channel devices is reduced by adjusting back bias, short channel Vt becomes too low to keep the advantage of ES-UB-MOSFETs' scaling capability. Therefore, it is desirable to improve its Vt roll-off curve for keeping its excellent scaling capability and achieving desirable long channel Vt with the same back bias. We propose to use LNDD in substrate, like halo profile used in channel, to tune Vt roll-off curves of ES-UB-MOSFETs.

This work was supported in part by the Opening Project of Key Laboratory of Microelectronics Devices & Integrated Technology, Institute of Microelectronics of Chinese Academy of Sciences, National Basic Research Program of China (Grant No. 2011CBA00605), China National S&T Major Project 02 and CAS funding for China Recruitment Program of Global Experts.

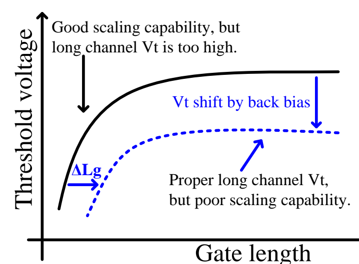


Figure 1. The challenges for gate length scaling with reducing Vt by adjusting back bias.

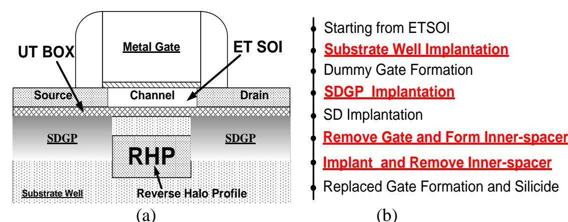


Figure 2. (a) Schematic of an ES-UB- MOSFET with reverse-halo profile (RHP). There is no RHP for conventional ES-UB-MOSFET. (b) A simplified process flow to form RHP with gate- last HKMG process.

## II. SIMULATION METHODS

Sentaurus [4] was used in our TCAD simulations. Process simulator is Sprocess with version Advanced-Calibration 2009.06. Device simulator is SDevice with calibrating carefully to the experimental results in [5]. The quantum-mechanical model Modified Local-Density Approximation (MLDA) is used to calculate the confined carrier distributions that occur near Si–$SiO_2$ interfaces. Mobility models including doping dependence, high-field saturation (velocity saturation), and transverse field dependence were specified for this simulation. Shockley–Read–Hall recombination with doping-dependent lifetime and band-to-band Auger define the generation and recombination model.


ISBN 978-0-615-71756-2

## III. Simulated Device Structure and Process Flow

The simulated ES-UB- MOSFET structure and corresponding dopant profile are shown in Fig.2, where SDGP is source/drain ground plane and reverse-halo profile (RHP) is counter doping profile self- aligned to the gate with inner spacer. The process flow of ES-UB- MOSFET, as shown in Fig.2 (b), is depicted in detail in our previous work [3]. The base-line ES-UB-MOSFET's geometrical parameters used in our simulation are listed in Table I.

TABLE I. DEVICE PARAMETERS USED IN SIMULATION

| Parameters | Value (nm) |
|---|---|
| BOX thickness | 5 |
| SOI thickness | 10 |
| Spacer thickness | 9 |
| Inner- Spacer thickness | 10 |
| Gate Height | 80 |
| Equivalent Oxide Thickness | 1.12 |

## IV. Characteristics of Ideal Devices

### A. Geometry and doping concentration

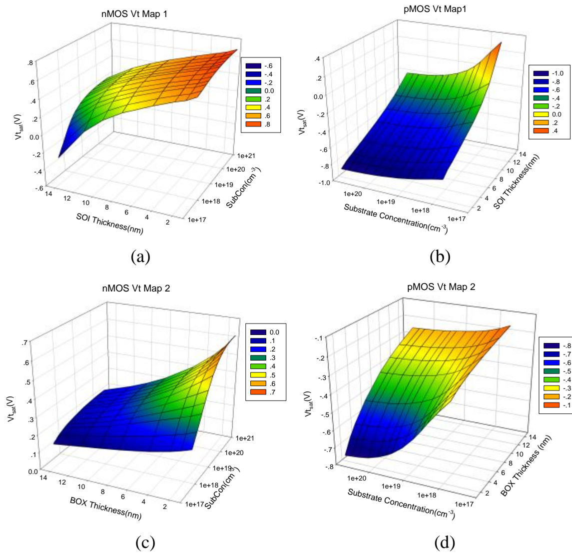


Figure 3. Vt-Map in various SOI thickness and substrate concentration (a) and various BOX thickness and substrate concentration (b).WF=4.6eV

To optimize ES-UB-MOSFET's geometrical and doping parameters, an ideal-doped profile (box-like, and uniform substrate doping) ES-UB-MOSFET was simulated. The effects of the substrate concentration, SOI thickness and BOX thickness on Vt-sat are shown in Fig.3. |Vt-sat| can be reduced by decreasing the substrate doping concentration and/or by increasing SOI thickness. Thinner BOX, thicker SOI and higher substrate halo-typed doping concentration can accelerate the change of Vt. Decreasing the BOX thickness and increasing the substrate concentration enhance the charge density in the substrate near the bottom surface of BOX coupling with channel carriers, which will increase the |Vt-sat|. Vt is sensitive with the total dopant dose under the channel in the substrate [3]. The reduced SOI thickness results the |Vt| increase for NMOS and PMOS devices. This is due to the quantum confinement of inversion charge [6].

### B. Back bias and metal-gate work-function

Fixing long channel threshold voltage at ±0.3V, both the band-edge work-function and high forward |Vbb| and enhance

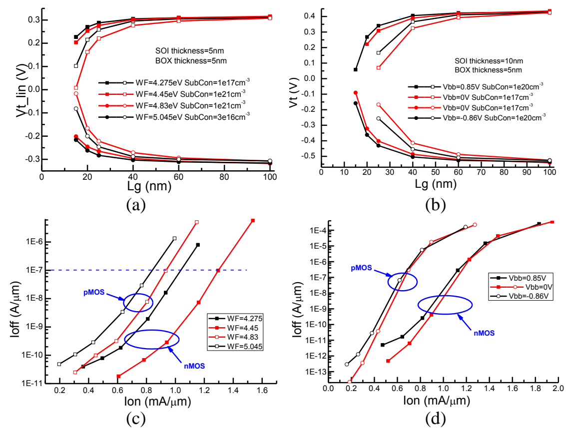


Figure 4. Vt Roll-off curves with controlling work-function and substrate concentration (a) or back bias and substrate concentration (b). Ion-Ioff curves with controlling work-function (c) and back bias (d).

the scaling of the Vt roll-off by co-adjusting the substrate concentration, but the band-edge work-function's Ion vs. Ioff performance degrades obviously, while high forward |Vbb|'s enhanced, as shown in Fig.4.

Fixing the substrate concentration at 2E18cm$^{-3}$ and the long channel threshold voltage at ±0.3V, by adjusting the work-function and back bias, the Ion vs. Ioff performance of mid-gap work-function is enhanced with mainly the same scaling capability, as shown in Fig.5 (a)/ (b). The effective current (Ieff [7]) vs. Ioff performance is balanced out by the $I_{low}$ (Isd when Vg = Vdd/2 and Vd = Vdd) vs. Ioff performance and $I_{high}$ (Isd when Vg=Vdd and Vd=Vdd/2) vs. Ioff performance, as shown

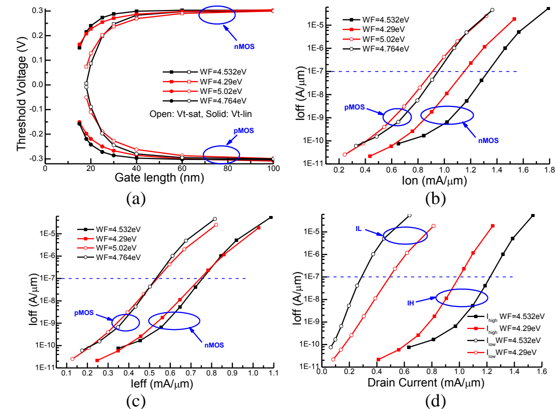


Figure 5. Vt Roll-off curves (a) and Ion vs. Ioff Curves (b) Ieff vs. Ioff Curves (c) $I_{high}/I_{low}$ vs. Ioff Curves (d) by controlling work-function and back bias with same substrate concentration.

in Fig.5 (c)/ (d).

The threshold voltage is affected by the metal-gate work-function directly. The band-edge work-function metal gate's Ion vs. Ioff performance is degraded but the Ieff vs. Ioff performance is enhanced. This enhancement mainly comes from $I_{low}$ since work-function enhancement is easier to be obtained with shorter gate length and/or lower Vgs. At high Ion and/or Ieff, ES-UB-MOSFETs with mid-gap work-function shows excellent Ioff control for the total turned off of the channel. The channel of ES-UB-MOSFETs with band-edge work-function is lightly turned on, which provides a SD leakage channel. At low Ion and/or Ieff, the channel is

controlled by the gate, and the influence of work-function in long channel is not as obvious as short channel devices.

While the back bias and the substrate doping can help controlling the channel bottom surface, and the performance enhancement mainly comes from $I_{high}$ since back bias enhancement is easier to be obtained when Isd/Ioff slope is sharper or Vsd is lower. At low Ion and/or Ieff, ES-UB-MOSFETs w/o RHP and Vbb = 0V shows excellent Ioff control for the total turned off of the channel. The bottom surfaces of the channel in the other two cases are lightly turned on, which provides a SD leakage channel. At high Ion and/or Ieff, the channel is controlled by the gate, and the influence of the back gate and RHP is not as obvious as low gate bias. In the simulation of ideal-doped profile ES-UB-MOSFET, there are humps in the Vt vs. Vbb curves with low substrate concentration, as shown in Fig.6, due to depletion of the substrate [8-9].

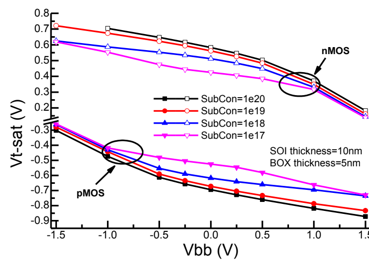


Figure 6. Vt-sat vs. Vbb curve under different substrate concentration.

### C. *Substrate doping engineering*

The lateral dopant distribution in the substrate was studied in this paper, and Reverse Halo Profile (RHP) is used to form Lateral Non-uniform Dopant Distribution (LNDD), as shown in Fig.2 (a). The dopants under the channel will affect the threshold voltage. It turns out that Vt-sat increases with increasing of the total halo-typed dopant dose in the substrate and saturates at total dose = 1.5E20cm$^{-2}$. Moreover, Vt-sat decreases with the increase of the total reverse-halo-typed dopant dose in the substrate and saturates at total dose = 4E19cm$^{-2}$ when the RHP is partially depleted [3]. This can be used to design the Vt Roll-off and enhance the scaling capability with co-using inner-spacer.

As shown in section B, the band-edge work-function and/or forward back bias can enhance the scaling capability, so Band-edge work-function (4.4eV/4.8eV for n-/p-FET respectively) is used in this section. Fixing long channel Vt by back bias and/or RHP, RHP can enhance the scaling capability by 4~5nm (shown in Fig.7 (a)) without losing Ion vs. Ioff performance (shown in Fig.7 (b)). When the gate length scales to 20nm, the

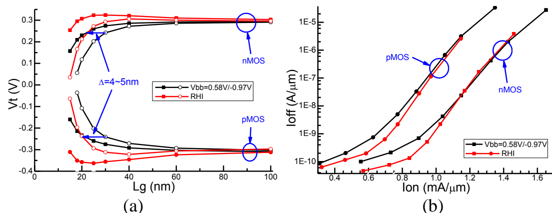


Figure 7. Vt Roll-off curves (a) and Ion vs. Ioff curves (b) for ES-UB-MOSFETs, 1) w/ RHP with Vbb = 0V and 2) w/o RHP with Vbb = 0.58V for nMOS and Vbb = -0.97 for pMOS

ES-UB-MOSFET shows good Id vs. Vg controllability.

## V. PROCESS AND DEVICE SIMULATION RESULTS AND DISCUSSIONS

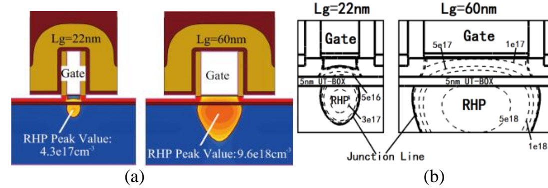


Figure 11. (a) 2D doping distributions in ES-UB- MOSFETs w/ RHP. They clearly show that the RHP concentration is higher in long channel device than that in short channel. (b) Zoomed-in 2D doping contour plot in the channel of ES-UB- MOSFETs w/ RHP. The dopant concentration generated by RHP implant is less than 1e17 near inversion layer.

After calibrating the simulation method to [4] and optimizing the values of the overlap capacitors (Cov) for ES-UB-MOSFETs to 0.25-0.3fF/μm by maximizing on state current (Ion) with minimum Cov, 20nm devices is optimized and simulated from the TCAD simulator Sprocess and Sdevice. 2D doping profiles in the substrate and channel of ES-UB-MOSFETs w/ RHP are shown in Fig.8. The inner spacer help to block short channel to receive RHP, and RHP lowers Vt for long channel devices more than that for short channel, which can help to tune Vt roll-off curve. The Id vs. Vg curves for 20nm ES-UB-MOSFET with RHP are shown in Fig.9, which shows excellent SCE control.

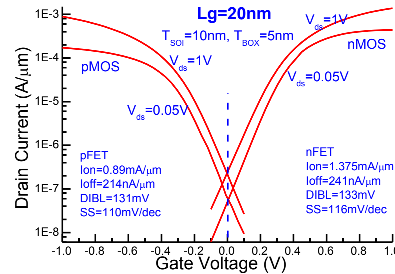


Figure 9. $I_D$ vs. $V_G$ curves for ES-UB MOSFETs w/ RHP at Lg = 20nm. Excellent SCE control was obtained.

Vt roll-off between ES-UB-MOSFETs w/ and w/o RHP is compared in Fig.10. Fixing long channel Vt-sat at 0.3V, RHP enables gate length to be scaled to 20nm, which is ~10% smaller than that of ES-UB-MOSFETs with back bias and uniform doped substrate. Fig 11 shows the values of Ion@Ioff = 10$^{-7}$A/μm and the values of Ieff@Ioff = 10$^{-7}$A/μm are comparable for the ES-UB-MOSFETs: 1) w/ RHP, Vbb = -0.85V, work-function (WF) = 4.4eV for nMOS, 2) w/ RHP, Vbb = 1.04V, WF = 4.9eV for pMOS, 3) w/o RHP and Vbb = -0.4V for nMOS, 4) w/o RHP and Vbb = 0.3V for pMOS.

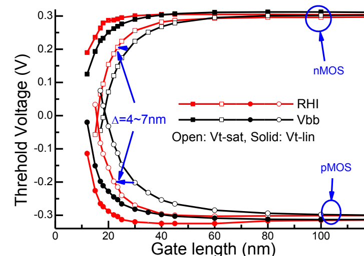


Figure 10. Vt Roll-off curves for ES-UB-MOSFETs in four cases: 1) w/ RHP, Vbb = -0.85V, work-function (WF) = 4.4eV for nMOS, 2) w/ RHP, Vbb = 1.04V, WF = 4.9eV for pMOS, 3) w/o RHP and Vbb = -0.4V for nMOS, 4) w/o RHP and Vbb = 0.3V for pMOS.

The changing of total capacitance (Cg-sd + Csub-sd) induced by the changing of Vbb [3] is negligible in this

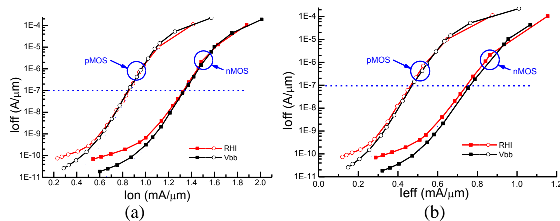


Figure 11. The comparison of Ion and/or Ieff vs. Ioff curves of the ES-UB-MOSFETs in four cases same as Fig.10.

simulation. Due to the channel bottom surface turned on [3], the total capacitance (Cg-sd + Csub-sd) increases ~0.01fF/μm (about 3%) from Vbb = -0.85V to Vbb = -0.4V for Lg = 20nm.

## VI. CONCLUSION

In this paper, the effect of work-function, back bias and substrate concentration was studied in details. The band-edge work-function enhances the $I_{low}$ vs. Ioff performance while high forward |Vbb| and halo-typed substrate concentration can enhance the $I_{high}$ vs. Ioff performance. A Lateral Non-uniform Dopant Distribution (LNDD) in substrate for ET-SOI MOSFETs with UT- BOX (ES-UB-MOSFETs) is used and investigated. Available process compatible with the conventional MOSFETs process is simulated. Comparison shows that fixing long channel Vt at ±0.3V, LNDD enables the gate length scaling to 20nm which is about 10% smaller than that in ES-UB- MOSFETs with lateral uniform doping in substrate and forward back bias. The change of total capacitance (Cg-sd + Csub-sd) induced by the change of Back bias reported in our previous work can be neglected in this work.

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