TCAD Electrical Parameters Extraction on Through Silicon Via (TSV) Structures in a 0.35µm Analog Mixed-Signal CMOS

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Abstract—**This paper presents the electrical behavior of Through Silicon Via (TSV) in an 0.35 analog mixed-signal CMOS technology. Key DC parameters as TSV Resistance and Capacitance are extracted. Small signal analysis and S-parameter extraction are performed on the structure, showing the signal modification because of the structure parasitic.**

Keywords: Through Silicon Via (TSV); 2D/3D TCAD; Small Signal Analysis ; S-parameter; Signal Loss

I. Introduction

3D integration of integrated circuits including High voltage, CMOS, photodiode and MEMS devices [1] is a key challenge for the future evolution of integrated semiconductor systems. A Through Silicon Via (TSV) is one key element connecting stacked circuits (Fig. 1).

One key challenge for the TCAD simulation is to be able to model the multiple process steps required to generate devices and TSVs [2] and to model signal propagation between different 3D circuit levels passing through the TSV. This work describes the electrical behavior of a 250µm deep and 100µm diameter TSV which is modeled by TCAD simulation in a 3D integrated 0.35µm analog mixed-signal CMOS technology.

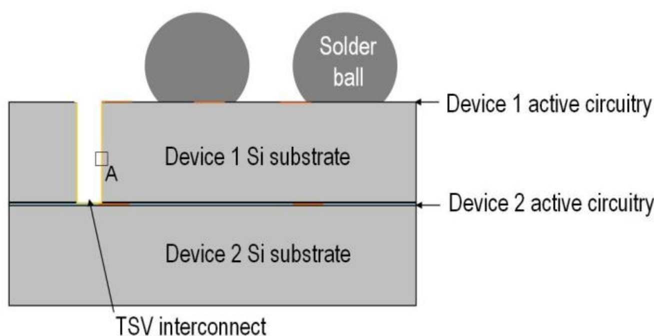

Figure 1. Cross-section diagram of wafer bonded components, with TSV.

II. TSV Structure Generation

Considering the large size of the TSV device studied, electrical characteristics of the TSV have been simulated by leveraging the structure symmetry using cylindrical coordinates.

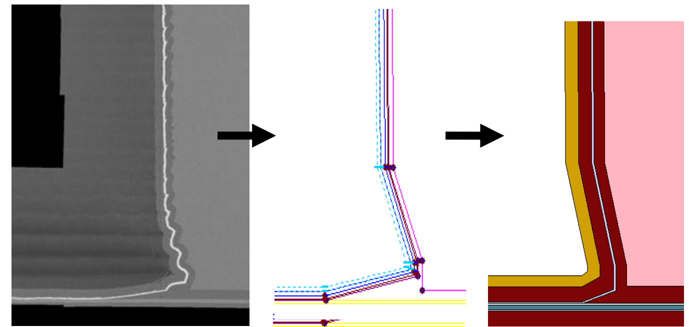

Figure 2. Bottom TSV TEM cross-section (left), layer polygon extraction (middle) and final 2D structure(right).

Polygonal 2D shape layers extracted from full 2D process simulation and information from Transmission Electron Microscopy (TEM) cross-sections of the TSV [3] have been used, as shown in Fig. 2. Physical TSV layer thicknesses have been extracted from TEM and 2D TCAD simulation, and the associated doping profiles from TCAD simulations. This method ensures a very flexible simulation environment (Fig. 3) by doing parameterization of the layers, and keeping the physical relationship between the doping distributions and the layer material properties. It is enabling the investigation of particular TSV side shape modifications like thicknesses variation, over-etch impact or scalloping effects without long and difficult calibration steps which are required in a pure 2D/3D process TCAD simulation.

The final structure combined with cylindrical coordinates gives reasonable simulation runtimes for DC electrical simulations, small signal and S-parameter analysis.

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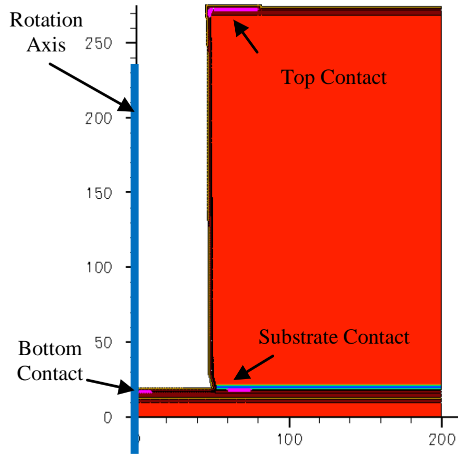

Figure 3. Final TSV structure including all layers needed, contacts placement, doping concentration in substrate; ready for electrical simulation in cylindrical coordinates.

III. ELECTRICAL SIMULATION

A. *TSV resistance*

Two contacts are placed on the top and bottom of the TSV metallization. The main contribution to the TSV resistance is expected to be the resistivity of the Tungsten layer used in the TSV. The Tungsten resistivity had been adjusted to the value of 7.5×10^{-6} Ohm.cm which is significantly different than the default value used in commercial software [4] which has been used throughout this work (2.6×10^{-6} Ohm.cm). However, the value is well in line with the value of 5.6×10^{-6} Ohm.cm given by [5]. With this modification, a TSV resistance of 350mOhm matching well to measurements [6] has been achieved. A Tungsten layer thickness of 200nm in the TSV has been studied. A thickness variation of 15% of the Tungsten thickness (325mOhm – 385mOhm) explains the main part of the process variability observed in Fig. 4. This variation is well in line with the expected variability of the process.

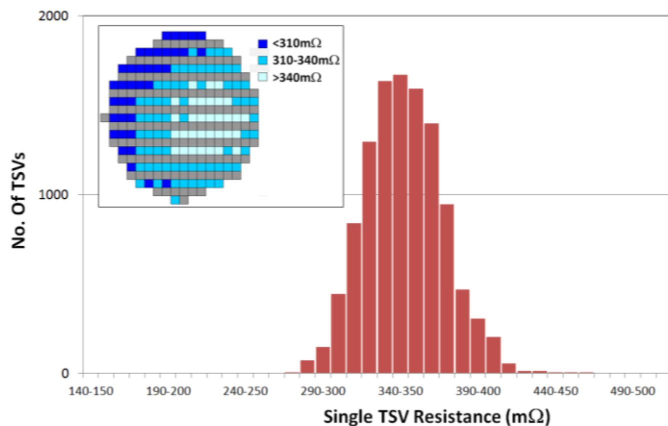

Figure 4. Single TSV resistance distribution (11,000 TSVs), measured by using a dedicated 3D Kelvin structure, compared to TCAD simulation showing the impact of Tungsten variation. Inset: Example TSV resistance wafer map (130 TSV measurements on one wafer).

B. *TSV Capacitance*

A substrate contact has been added to the structure on the bottom of the structure close to the TSV sidewall. A small signal stimulus is applied on this contact and the capacitance at different frequencies from fractions of Hz up to 10GHz has been extracted (see Fig. 5 and 6). For low frequency, the capacitance extraction yields 6.5pF for the structure analyzed and 3pF for frequencies in the range 100MHz up to 1GHz.

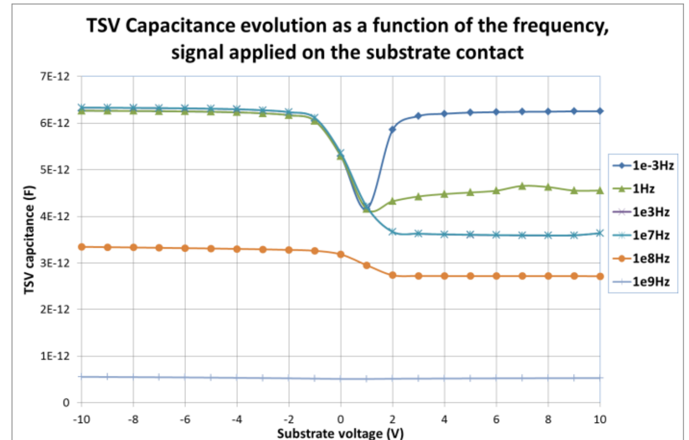

Figure 5. Capacitance evolution at several frequencies, typical capacitance at low frequency: 6.3pF.

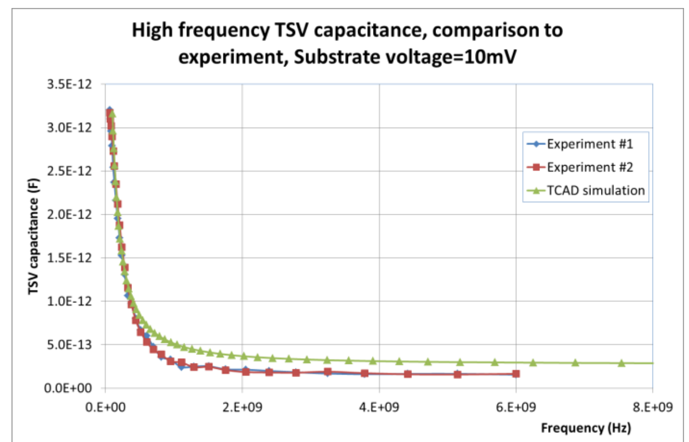

Figure 6. High frequency capacitance comparison to experiment. The capacitance used for modeling is 3pF.

C. *TSV small signal analysis and S parameter extraction*

An equivalent sub-circuit of the TSV can be described by an inductance (L_{TSV}) and a resistance (R_{TSV}) in series between the top and the bottom of the TSV and a capacitance C_{TSV} coupling the TSV to the silicon substrate (Fig. 7). The previous simulations and a SPICE optimization of the sub-circuit give the following values: L_{TSV}=12pH, R_{TSV}=0.35Ohm, C_{TSV}=3.4pF in the GHz frequency range.

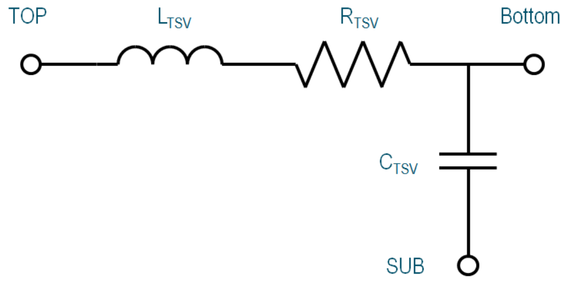

Figure 7. TSV sub-circuit description

1) Single TSV small signal analysis

The structure can be considered as a two port network between the top and the bottom of the structure allowing small signal analysis and S parameters extraction. The signal loss in [dB] curve (Fig. 8) is expressed through the S parameter matrix by:

$$\text{Signal Loss} = 20.\log_{10} |S21| \quad (1)$$

Fig. 8 presents the evolution of the signal loss for the TSV studied, and its comparison to experiment. The region transition of the TSV between the capacitive region at low frequencies, below 1GHz, and the resistive region at higher frequencies is observable on simulation and measurement at a signal loss of -0.9dB.

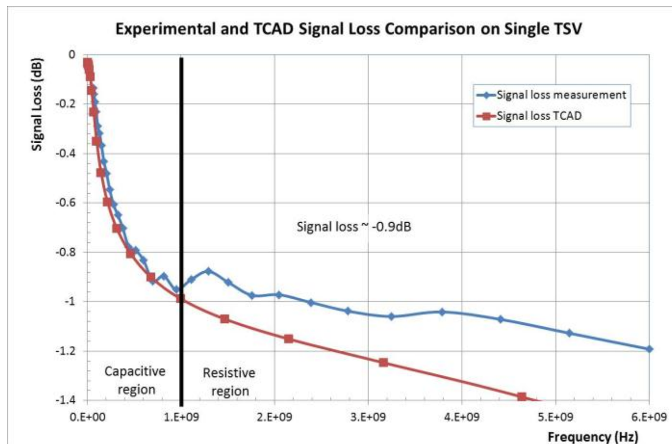

Figure 8. Comparison of the signal loss curve from expermental measurements and TCAD simulation.

The Locus curve presenting the evolution of the imaginary part of the S21 parameter versus the real part of the S21 parameter is shown in Fig. 9. This curve presents also the region transition observed in the previous picture in the GHz range with a good agreement of the TCAD small signal analysis with the experimental data for a large range of frequencies.

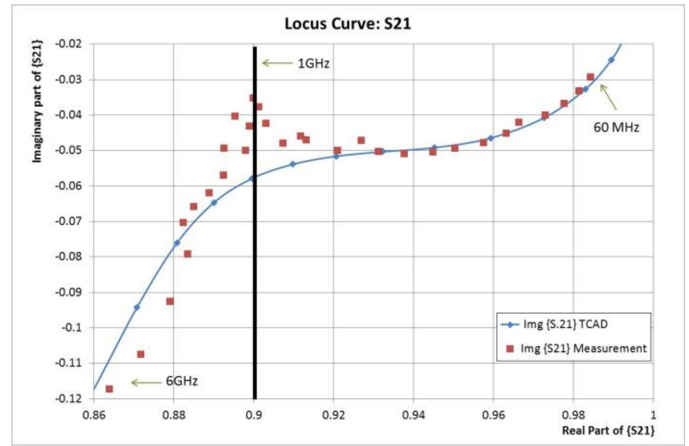

Figure 9. Locus curve of a single TSV, presenting region transition at the GHz range

2) Two TSV in series

In this section, the impact of the distance separating two TSV in series connected by their bottom contact with a metal line with a resistance of 4Ohm/square on the propagated signal is analyzed. The distance is varying from 25µm up to 275µm.

Considering the size of the domain consisting of two TSVs and the Silicon material in between including the metal line joining the TSVs, the whole structure had been cut in three different parts (see Fig. 10): one for each TSV and one for the metal line connecting the bottom of the TSVs. The parts are connected within a contact netlist, and the small signal analysis is performed in mixed-mode simulation.

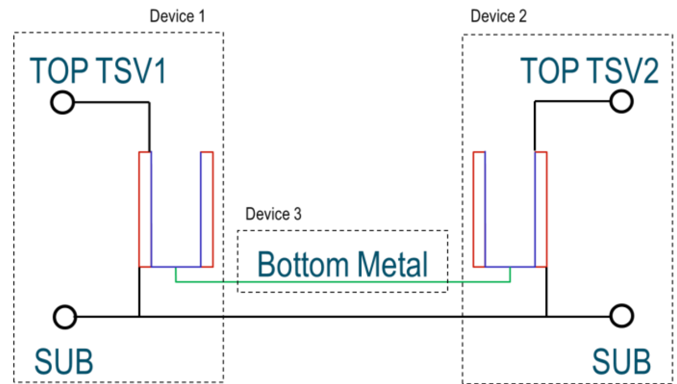

Figure 10. Two TSV in series schematic used for TCAD small signal analysis, where the structure has been separated in 3 different devices and connected through a contact netlist in mixed-mode simulation.

Fig. 11 presents the evolution of the signal loss occurring on a signal applied on one TSV and propagated to a second TSV through a metal connection on the bottom of the TSV. TCAD simulation shows a good agreement on the distances larger than 100 µm on the capacitive region (below 1GHz).

From the signal loss observed at 1GHz, we can model the signal loss value as a function of the TSV distance (Fig. 12). This model can be used in signal circuit analysis when multiple TSV are used for the propagation of a signal.

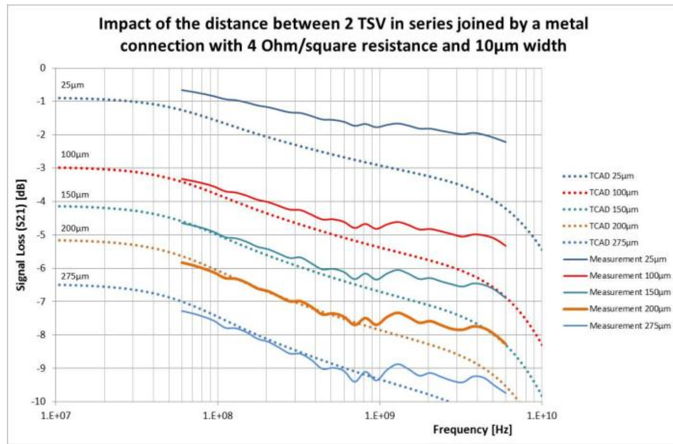

Figure 11. Impact of the distance separating 2 TSV in series by a metal connection of 4Ohm/Square on the Signal loss

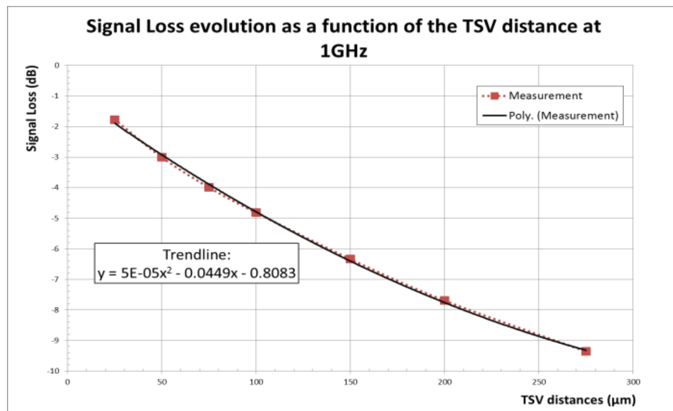

Figure 12. Signal loss modeling

Fig. 13 presents the impact of the width of the bottom line metal connection between the TSVs. TCAD simulation shows a good agreement with the experimental data excepted for the smallest metal connection. The trend observed and confirmed by experiments is to increase the metal connection width in order to minimize the Signal Loss.

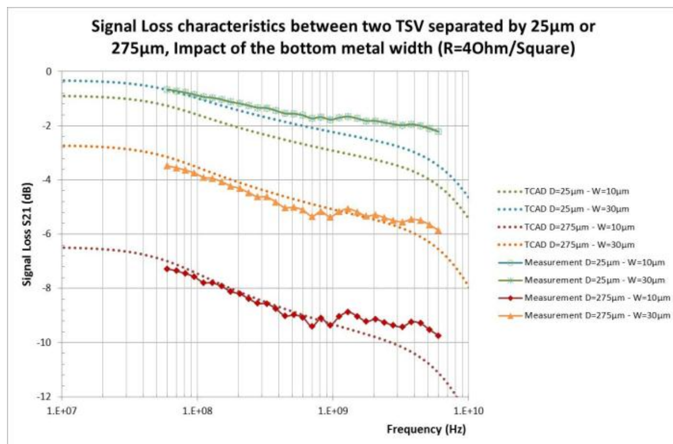

Figure 13. Bottom metal line width of 2 TSV impact on the Signal Loss

IV. CONCLUSION

This paper has demonstrated the capability of the TCAD simulation to represent the electrical behaviour of TSVs.

The method of TSV structure generation based on physical shape and on 2D process TCAD simulation permits a fast generation of flexible structures by parameterization of the associated layers including doping placement in Silicon.

The structure generated is then able to reproduce the key electrical characteristics like TSV Resistance (0.35Ohm) and TSV Capacitance (3.4pF).

The high frequency behaviour using small signal analysis and s-parameters of a two port network has also been carried out, showing the impact of the TSV structure on a signal applied to it with a signal loss of -0.9dB. In the case of two TSVs connected in series, the analysis highlights the impact of the bottom contact line layout by increasing the width of this line for reducing signal loss.

Finally, the physical and electrical behaviour known from TCAD electrical simulations permits the optimization of the TSV structure in stacked circuits of 3D integrated 0.35µm analog mixed-signal technology.

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