An Accurate Surface-Potential Based Large-Signal Model for HEMTs

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Abstract—An accurate surface-potential based large-signal model for compound semiconductor HEMTs is presented. A novel effective gate voltage model is introduced into the derivation of the model core. The method enables a directly application of the standard results from traditional surface-potential theory. As the symmetric linearization technique that used in surface-potential based MOSFET models is also inherited, the Gummel symmetry of an InGaAs/GaAs pHEMT is accurately characterized with the new model. The high-order derivatives of I-V/Q-V remain continuous, making the model suitable for RF large-signal applications. The method and modeling techniques have been verified through comparison with measured DC IV, CV and single-tone input power sweep at 29GHz for a $2\times10\mu\text{m}\times0.1\mu\text{m}$ InGaAs/GaAs power pHEMT, fabricated at a commercial foundry.

Keywords- compound semiconductor HEMTs; surface-potential based; large-signal model

I. Introduction

Compound semiconductor high electron mobility transistors (HEMTs), such as GaAs pHEMTs [1] and GaN HEMTs [2], are widely used in solid-state power amplifiers in a broad range of applications over a large spectrum from UHF to millimeter-wave frequencies. The integration of devices into a circuit environment for power amplifier design and simulation requires compact large-signal modeling of the device operating under various biasing conditions. As a principle for compact devices modeling, the model equations used for circuit simulation are, at best, directly based on or indirectly deduced from the important physics of devices. The principle has been well done in MOSFETs compact models [3]. The CMOS community reached the consensus that a surface-potential based model has superior properties, in particular for nonlinear simulation applications [3]-[4]. Unfortunately, most of the compact models that have been presented in literatures [5]-[10] or implemented in commercial simulators (such as the EEHEMT model implemented in Agilent Advanced Design Systems (ADS)) are still empirical. By using the well known surface-potential (SP) theory and equation resembled the one used in MOSFET models, a scanty sole physical based compact model which suitable for GaN HEMTs large-signal modeling has been presented in [4]. In order to consider the difference of operation region of HEMTs from MOSFETs, [4] chosen not to

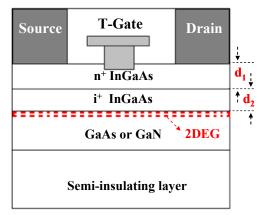


Figure 1. Schematic cross-section of GaAs HEMTs.

use the symmetric linearization technique in arriving at compact model core, thus few of the standard results from the surface-potential theory can be used. As a result, the model is not a Gummel symmetry test passed model.

The purpose of this work is to introduce an alternative method for the SP based large-signal model core derivation for HEMTs which permit to use the standard results from the SP theory directly. The model and modeling techniques have been verified by an accurate predicting of DC I-V, Gummel symmetry test, C-V and large-signal characterizations of a $2\times150\mu\text{m}\times0.1\mu\text{m}$ InGaAs/GaAs pHEMT, fabricated at a commercial foundry.

II. MODEL DESCRIPTION

A schematic cross section of typical compound semiconductor HEMTs is shown in Figure 1. Assumed that: 1) InGaAs layer is fully-depleted; 2) the substrate is treated as insulating; and 3) the channel 2DEG is considered as a charge sheet, we apply the gradual channel approximation (GCA) to obtain the following surface-potential equation (SPE) derived in this work can finally be arranged as follows:

$$(x_{n}-x)^{2} = G^{2} \{e^{-x} + x - 1 + \Delta_{n} [e^{x} - x - 1 - \chi(x)]\}$$
 (1)

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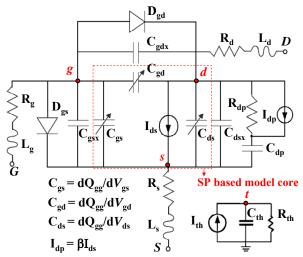


Figure 2. Topology of the proposed large-signal model. L_g , L_d , L_s , R_g , R_d and R_s are the parasitic inductors and resistors of gate (G), drain (D) and source (S), respectively. D_{gd} and D_{gs} are the gate-source and gate-drain diodes, respectively. C_{gax} , C_{gdx} and C_{dsx} represent the external bias-independent parasitic capacitors. C_{gs} , C_{gd} , C_{ds} and I_{ds} are the intrinsic components. A simple AC current I_{dp} , combined with R_{dp} and C_{dp} , is introduced to characterize the trans-conductance frequency dispersion effect of the device. B is model parameter. The self-heating effect is considered in the additional sub-circuit model given at the bottom right in the figure.

where $x = \psi_s/V_T$, ψ_s is the surface potential, $V_T = k_BT/q$. $V_{\rm fb}$ is the flat band voltage, $\chi(x) = -\Delta_{\rm nx}e^x + \Delta_{\rm nx} - x$, $\Delta_{\rm nx} = (e^4 - e^B)$, $A = (E_{\rm C} - E_{\rm F})/qV_{\rm T} + \ln(N_{\rm V}/N_{\rm C}) + (E_{\rm V} - E_{\rm F})/qV_{\rm T}$, $B = (E_{\rm C} - E_{\rm F})/qV_{\rm T} + \ln(N_{\rm A}/N_{\rm C})$, $E_{\rm F}$ is the Fermi level, $E_{\rm C} = kT\ln(N_{\rm A}/N_{\rm C})$, $E_{\rm V} = kT\ln(N_{\rm V}/N_{\rm D})$, $N_{\rm V}$ and $N_{\rm C}$ are impurity concentrations. $N_{\rm A} = N_{\rm V} - N_{\rm C}$. $\Delta_{\rm n} = e^{C_{\rm C}D}$, where $C = (E_{\rm C} - E_{\rm F})/qV_{\rm T} - \ln(N_{\rm C}/N_{\rm A})$ and $D = V_{\rm n}/V_{\rm T}$, $V_{\rm n}$ is the voltage applied to the channel. G is defined as $G = (2q\varepsilon_1N_{\rm A}/V_{\rm T})^{1/2}/C_0$, where C_0 is calculated as $C_0 = \varepsilon_{\rm x}/(d_1 + d_2)$, $N_{\rm D}$ and $\varepsilon_{\rm x}$ are the electron concentration and relative permittivity of the GaAs layer, respectively.

As the derived SPE resembles the one used in conventional MOSFET models [3], the analysis solutions for surface potential can also be borrowed and directly used here. However, as what has mentioned in [4], the symmetric linearization [11] that is employed for MOSFETs, which is crucial in arriving at compact expressions for the current and charges, will cause problems in capturing the characterization of compound semiconductor HEMTs operating in accumulation region. The HEMTs operate in accumulation at the surface rather than in inversion as in the MOSFETs. As a result, all of the equations for currents and charges in [4] are derived from scratch using nonlinear, binomial expansions of the electronic charge density. The symmetric linearization technique is finally not used.

Equation (1) resembles the one used in PSP model [2], so to use the standard results from that theory becomes our natural choice. Due to the fact that HEMT operate in accumulation at the surface rather than in inversion as in the MOSFET, the symmetric linearization technique employed for MOSFETs has no influence on HEMTs characterization. The obstacle to the direct application of the standard results from

MOSFET SPE theory to HEMTs resides on this accumulation regime. Our investigation show that, the problems caused by employing the symmetric linearization technique [11] to (1) for the channel current and charges model equations derivation, is mainly centralized in the operating region of $x_g \le 0$, while can be directly used in the operating region of $x_g > 0$. Considering that the integral results of the surface charge is controlled by the gate voltage mathematically, an effective gate bias $V_{\rm gs,eff}$ is introduced ($x_{\rm g} = V_{\rm gs,eff} / V_{\rm T}$), to realize the transition for the integral of the surface charge from the results derived in the depletion regime to accumulation regime smoothly, while keeping the math structure of the PSP model, so that the symmetric linearization is inherited. $V_{\rm gs,eff}$ is defined as

$$V_{gs, eff} = P_1 \ln(1 + e^{V_2/P_2})$$
 (2)

$$V_1 = V_{gs} - V_{fb} - \Delta V_{fb} (1 + B_0 \ln \cosh(B_1 V_{gd} - V_{bx}))$$
 (2.1)

$$V_{2} = \frac{1}{2} \left[V_{1} + \sqrt{(V_{1} - V_{k})^{2} + \Delta V_{g}^{2}} - \sqrt{V_{k}^{2} + \Delta V_{g}^{2}} \right]$$
 (2.2)

where ΔV_{fb} , V_{bx} , B_0 , B_1 , B_x , V_k , ΔV_g , P_1 and P_2 are model parameters. V_{gs} and V_{gd} are the gate-source and gate-drain voltage, respectively. As the channel is buried one in HEMTs, V_{gs_eff} can also be used to characterize the change of the gate voltage to the channel caused by layers on the channel. The effective gate voltage model, which minus the flat band voltage, could be used to adjust the integral results of surface potential for charges calculation at the small gate voltage region smoothly. Thus the standard SPE results derived at the MOSFET operating in inversion region can be expanded into the HEMTs modeling, though which operating in accumulation at the surface.

The derived analytic solutions for (1) is similar to that in conventional MOSFET models, except of the expression of the flat band voltage, which is process parameters sensitized. The final equations for the drain current (I_{ds}) and gate charge (Q_{gg}) are similar to the industry standard PSP model, the symmetric equations given in the industry PSP model core (Verilog-A version) is further modified to fit HEMT modeling. Agilent Advanced Design System (ADS) and IC-CAP are used to simulate and extract the model parameters from measurements, respectively.

The quality and the capability of the dc transistor model are demonstrated by the description of DC I-V and the Gummel symmetry measurements (see Figure 3 and 4). To characterize the RF behavior, S-parameter measurements were performed. In Figure 5, the capacitances for various bias conditions are shown as extracted from measured and simulated S-parameters at $F_{req} = 4.16 GHz$. Figure 6 shows a simulation result of a single-tone input-power sweep for the modeled device at $F_{req} = 29 GHz$. Excellent results with respect to the measured are achieved. The excellent agreements between the measured and simulated results verified and validated the accuracy of the

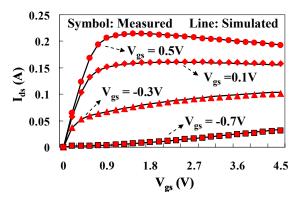


Figure 3. Measured and simulated I_{ds} vs. V_{ds} T=25°C.

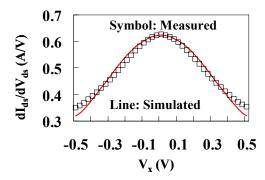


Figure 4. Gummel symmetry test at $V_{gs} = 0V$.

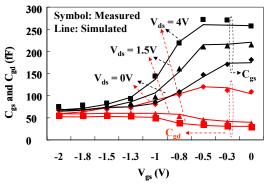


Figure 5. C_{gs} and C_{gd} extracted from measured and simulated S-parameters at $F_{req}=4.16GHz$.

linearization technique and results are remained. Figure 2 gives the topology of the proposed large-signal model.

III. MODEL VERIFICATION

For verification, a depletion-mode (D-mode) InGaAs/GaAs pHEMT with 2 gate fingers, that has a 150µm gate width for each finger, 0.1µm gate length, was fabricated at a commercial foundry. On-wafer measure is executed for parameter extraction. The model topology and the model

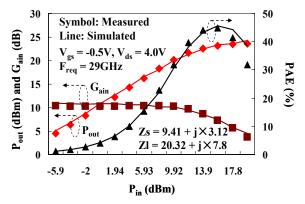


Figure 6. Model simulated and measured fundamental output power (P_{out}) , gain and power added efficiency (PAE).

proposed large-signal model for GaAs HEMTs, which verified that the model also holds for GaN power HEMTs.

IV. CONCLUSION

In this paper, we present a full SP-based HEMT model with high precision in all operation regions and large-signal conditions as well. The quality of the model is demonstrated and verified by direct comparison to DC I-V, C-V and single-tone input-power sweep results of a 2×150µm×0.1µm InGaAs/GaAs power pHEMT. From the best of our knowledge, this model maybe the first reported Gummel symmetric SP based large-signal model for compound semiconductor HEMTs.

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