

The Flexible Compact SOI-MOSFET Model HiSIM-SOI Valid for Any Structural Types

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Abstract—We have developed the HiSIM-SOI model which is a complete surface-potential-based compact model valid for any structural variations of SOI-MOSFETs. This work focuses on how to calculate the three surface-potential values at the FOX/SOI-layer surface, the SOI-layer/BOX surface, and the BOX/substrate surface. The Newton iteration with three variables is investigated. With good initial guesses of the three surface potentials, accurate solutions are obtained with small number of iterations. Dynamically switching depletion modes are achieved by considering all possible charges induced within the device explicitly. Furthermore, SPICE simulation of 100-stage NAND chains demonstrates stable convergence of the surface-potential Newton iteration for any bias conditions.

Keywords—surface potential; SOI; MOSFET; compact model; HiSIM; convergence

I. INTRODUCTION

The SOI-MOSFET technology is getting more attention due to its wide application varieties being achieved by varying the SOI-layer thickness as well as the impurity concentration [1]. The partially depleted SOI-MOSFET structure with a rather thick SOI layer has been applied for high performance circuits. On the contrary, the ultra-thin-layer SOI-MOSFET structure is recently considered to be very useful for suppressing the MOSFET performance variations [2]. We have developed HiSIM-SOI, the first SOI-MOSFET model based on the complete surface-potential description, which is valid for any structural variations [3-7]. The main new development here is focused on how to calculate the surface-potential values, basic values for describing device characteristics. HiSIM-SOI currently captures the dynamic depletion behavior according to the device structure as well as the bias condition. However, further improvement of accurate as well as stable convergence of the surface-potential calculation is inevitable to obtain stable circuit simulation.

II. HOW TO CALCULATE SURFACE POTENTIALS

In modeling, all important features are included in the Poisson equation. As shown in Fig. 1, there are three surface potentials ($\phi_{s,SOI}$, $\phi_{b,SOI}$, $\phi_{s,bulk}$) in the SOI structure, and inducing charges appear in the Poisson equation. From the Poisson equation and the Gauss law, three basic equations are derived as

$$V_{gs} - V_{fb} = \phi_{s,SOI} - \frac{Q_i + Q_{dep} + Q_{b,SOI} + Q_{s,bulk} + Q_n}{C_{FOX}} \quad (1)$$

$$\phi_{s,SOI} = \phi_{b,SOI} - \frac{Q_{s,bulk} + \frac{1}{2}Q_{dep}}{C_{SOI}} \quad (2)$$

$$\phi_{b,SOI} = \phi_{s,bulk} - \frac{Q_{s,bulk}}{C_{BOX}} \quad (3)$$

by considering boundary conditions together with an approximation of a linearly decreasing current distribution into the bulk, where $C_{FOX} = \epsilon_{ox}/T_{FOX}$, $C_{SOI} = \epsilon_s/T_{SOI}$, and $C_{BOX} = \epsilon_{ox}/T_{BOX}$. V_{gs} and V_{fb} are the gate-source bias voltage and the flat-band voltage, respectively.

All charges appearing in the above equations are functions of these three surface-potential values. The main new development is connected with how to solve these equations including three unknown surface-potential values ($\phi_{s,SOI}$, $\phi_{b,SOI}$, $\phi_{s,bulk}$; see Fig. 1). For accurate and flexible circuit simulation model applicable to any structures under any bias conditions, above three equations must be solved iteratively. Here we

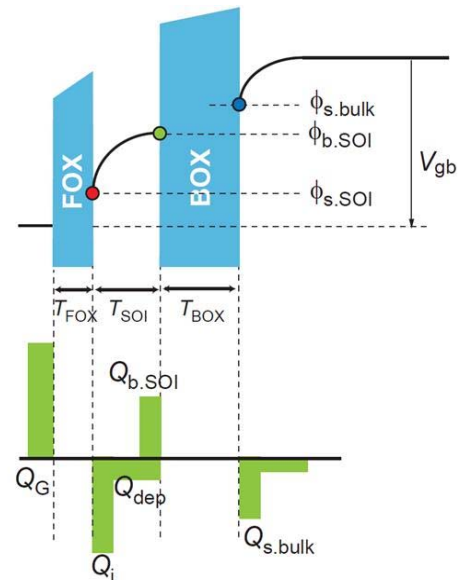


Figure 1. Three surface potentials induced in SOI-MOSFET.

have developed the Newton iteration method for solving three equations simultaneously as

$$\phi_{\text{new}} = \phi + \delta\phi \quad (4)$$

where $\phi = (\phi_{s,\text{SOI}}, \phi_{b,\text{SOI}}, \phi_{s,\text{bulk}})^T$ and $\delta\phi$ is calculated as

$$\delta\phi = -\mathbf{J}^{-1} \cdot \mathbf{f} \quad (5)$$

where $\mathbf{f} = (f_1, f_2, f_3)^T$ which comes from Eqs. (1)-(3) so that each component of \mathbf{f} equals to zero as

$$f_1 = \phi_{s,\text{SOI}} - (V_{\text{gs}} - V_{\text{fb}}) - \frac{Q_i + Q_{\text{dep}} + Q_{b,\text{SOI}} + Q_{s,\text{bulk}} + Q_{\text{h}}}{C_{\text{FOX}}} = 0 \quad (6)$$

$$f_2 = \phi_{b,\text{SOI}} - \phi_{s,\text{SOI}} - \frac{Q_{s,\text{bulk}} + \frac{1}{2}Q_{\text{dep}}}{C_{\text{SOI}}} = 0 \quad (7)$$

$$f_3 = \phi_{s,\text{bulk}} - \phi_{b,\text{SOI}} - \frac{Q_{s,\text{bulk}}}{C_{\text{BOX}}} = 0 \quad (8)$$

\mathbf{J} in Eq. (5) is the Jacobian matrix which consists of partial derivatives of \mathbf{f} with respect to ϕ as written as

$$\mathbf{J} = \begin{pmatrix} \frac{\partial f_1}{\partial \phi_{s,\text{SOI}}} & \frac{\partial f_1}{\partial \phi_{b,\text{SOI}}} & \frac{\partial f_1}{\partial \phi_{s,\text{bulk}}} \\ \frac{\partial f_2}{\partial \phi_{s,\text{SOI}}} & \frac{\partial f_2}{\partial \phi_{b,\text{SOI}}} & \frac{\partial f_2}{\partial \phi_{s,\text{bulk}}} \\ \frac{\partial f_3}{\partial \phi_{s,\text{SOI}}} & \frac{\partial f_3}{\partial \phi_{b,\text{SOI}}} & \frac{\partial f_3}{\partial \phi_{s,\text{bulk}}} \end{pmatrix} \quad (9)$$

In the Newton iteration method, Eq. (4) is repeated until $\delta\phi$ becomes small enough. In HiSIM-SOI, convergence criterion for $\delta\phi$ is set to 5×10^{-13} V to achieve smooth bias dependence of the surface potentials and even their higher-order derivatives. HiSIM-SOI solves the three basic equations twice, for the source and the drain sides separately.

III. INITIAL GUESSES FOR ACCURATE AND STABLE CONVERGENCE

Circuit simulator detects unavoidable extreme bias conditions during iterations, for which normal model equations are hardly applicable. Compact models must provide device performances even for such unrealistic cases. This can be done by deriving analytical equations for such limiting cases. Under normal operation conditions it happens often that three surface-potential values are strongly connected each other. This makes iteration difficult to achieve stable solutions. To avoid the iteration divergence for any cases, good initial guesses for three

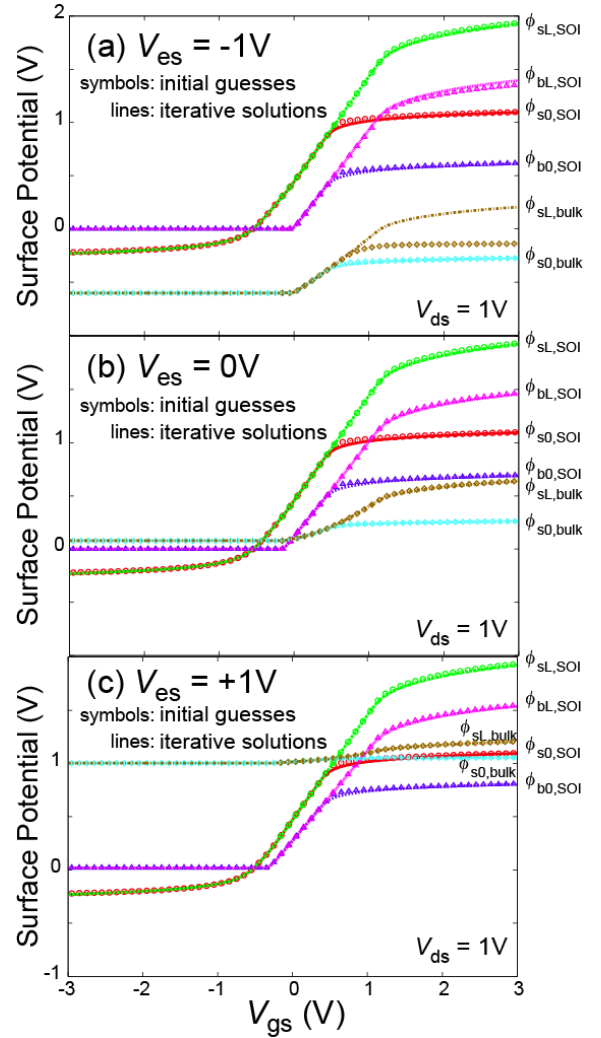


Figure 2. Comparison of the initial-guess values and their iterative solutions of 6 surface potentials for a fully-depleted SOI MOSFET. Substrate bias voltage V_{es} is varied from -1V to 1V.

surface-potential values are inevitable. For this, we have derived analytical equations under several key bias conditions and combined these solutions with smoothing functions. For cases when analytical solutions cannot be derived, local iterations with one valuable are also performed. Since these accurate initial guesses can even reduce the number of iterations for the Newton procedure, the total calculation time can be reduced. The iteration counts in HiSIM-SOI are only about two times larger than those in the bulk-MOSFET model HiSIM2, where only a single surface potential is considered for each source or drain side. It has been demonstrated that the iterative HiSIM2 method is not disadvantageous in comparison to the non-iterative approach. Figure 2 compares the initial guesses and the iterative solutions of 6 surface potentials. HiSIM-SOI can accurately guess the initial values for the Newton iteration. Therefore, HiSIM-SOI can calculate smooth and accurate iterative solutions with small number of iteration count. As shown in Fig. 2, iterative solutions are smoother than the initial values, which has an advantage of good convergence in SPICE simulation.

TABLE I. MODELED PHENOMENA

Physical dependence on device parameters
Short-channel effects
Narrow-channel effects
Impact ionization effect
Poly-depletion effect
Quantum mechanical effect
Pocket implantation effects
Low & high field mobility model
Leakage current models
Noise models for all conduction mechanisms
Floating-body effect
History effect
Body-tie effect
Self-heating effect
DC & AC symmetries
Diode model

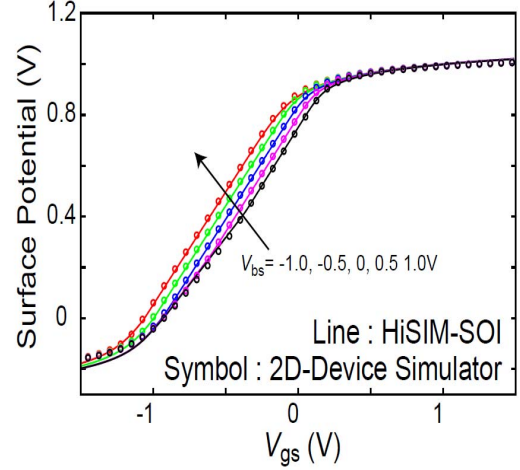
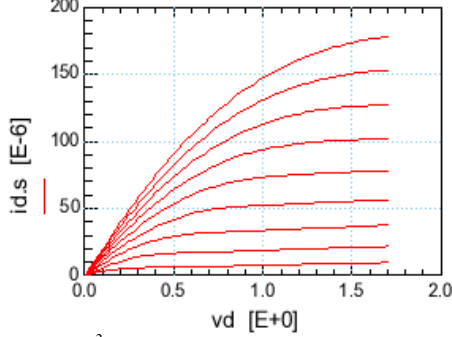
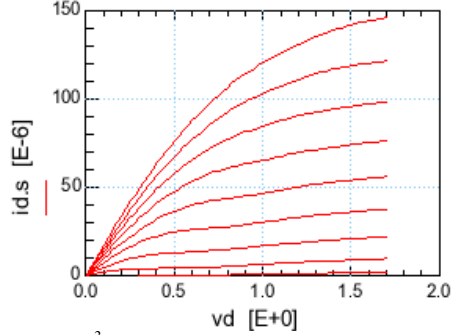


Figure 4. Calculated three surface-potential values on the source side of a fully depleted SOI-MOSFET with HiSIM-SOI in comparison to those with 2D-device simulations.

(a) $N_{SOI}=5e16 \text{ cm}^{-3}$ (fully depleted)



(b) $N_{SOI}=5e17 \text{ cm}^{-3}$ (dynamic depleted)



(c) $N_{SOI}=5e18 \text{ cm}^{-3}$ (partially depleted)

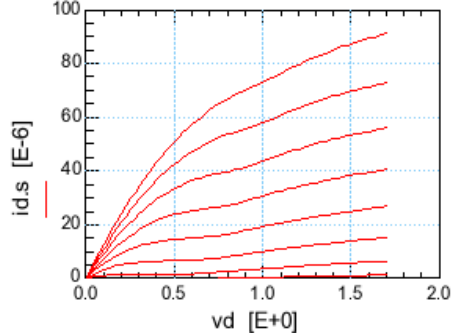


Figure 3. Calculated I_d - V_d characteristics with HiSIM-SOI for three different impurity concentrations of the SOI layer.

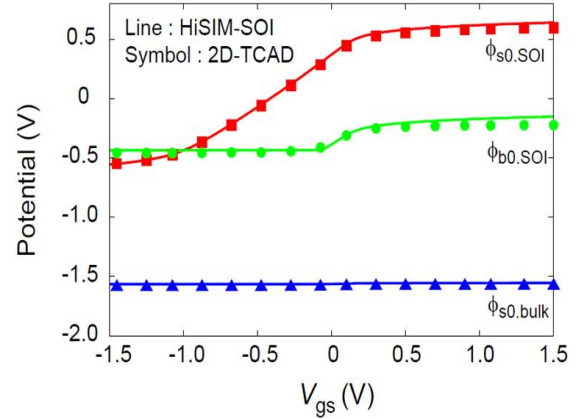


Figure 5. The same comparison of $\phi_{s0,SOI}$ as shown in Fig. 4 for an ultra thin fully depleted SOI-MOSFET.

IV. PERFORMANCE OF THE HiSIM-SOI MODEL

All modeled phenomena are summarized in Table 1. Figure 3 demonstrates the flexibility of HiSIM-SOI with different impurity concentrations. For the $N_{SOI}=5e16\text{cm}^{-3}$ case shown in Fig. 3a, the SOI layer is fully depleted until close to the flat-band condition resulting in reduced kink effects, whereas clear kink effects are observed for the $N_{SOI}=5e18\text{cm}^{-3}$ case shown in Fig. 3c. Figures 4 and 5 compare calculated surface potential values with 2D-device simulation results for different device types. Figure 6 shows comparisons with measurements of I_d - V_{gs} curves and its derivatives to the third order. Figure 7 demonstrates a circuit simulation result of 100-stage NAND-gate chains. With the HiSIM-SOI model, reasonable simulation results can be quickly obtained without any convergence problem.

V. CONCLUSION

In previous works, we have developed HiSIM-SOI based on the surface-potential approach. To complete the flexible SOI-MOSFET model to various SOI-layer thicknesses and BOX-layer thicknesses, three surface potentials must be calculated simultaneously by the Newton iteration method. In this work, we report the details of the surface-potential calculation. Reasonable initial guesses are introduced to get convergence with accurate solutions and small number of iteration count. As a result, HiSIM-SOI can flexibly reproduce measurement results for various kinds of SOI-MOSFETs. Furthermore, good convergence is verified for SPICE simulation of 100-stage NAND chains for example.

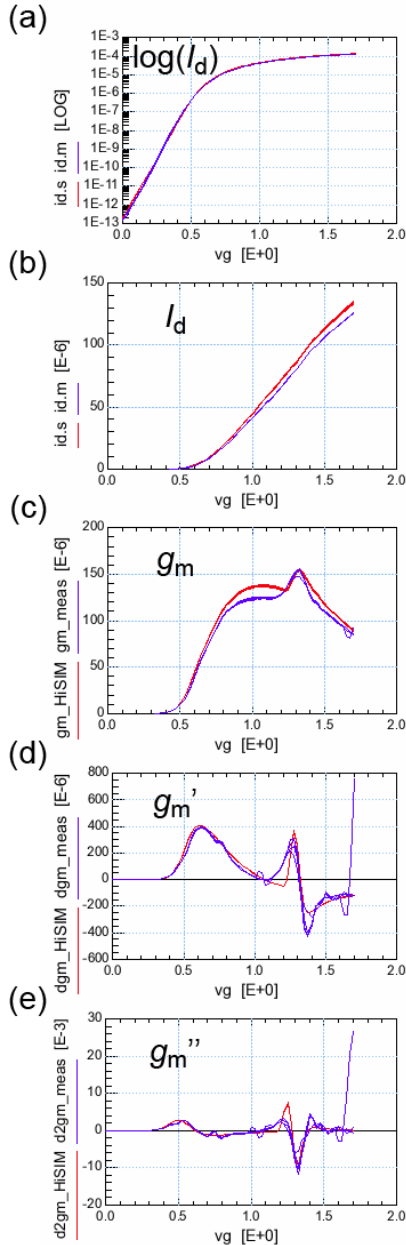


Figure 6. Comparison of HiSIM-SOI simulation results with measurements for partially-depleted floating-body SOI-MOSFET at $V_{ds}=0.05V$.

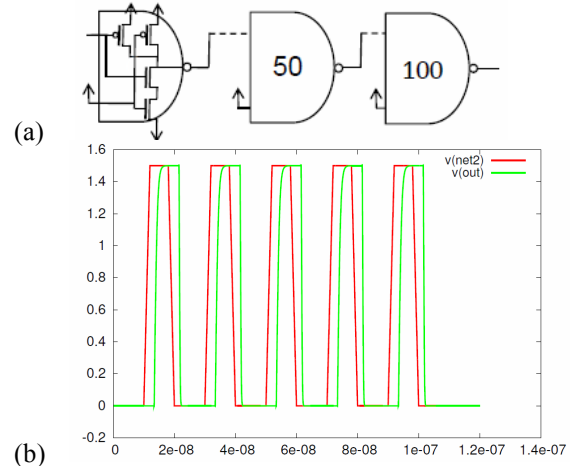


Figure 7. (a) A studied 100-stage NAND-gate chains and (b) its transient SPICE simulation result.

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