P6

A Smart Approach for Process Variation Correlation Modeling

Chung-Kai Lin, Cheng Hsiao, Wei-Min Chan, Min-Chie Jeng
Taiwan Semiconductor Manufacturing Company
168, Park Ave 2, Hsin-Chu Science Park, Hsin-Chu County, Taiwan 308-44, R.O.C
email: cklinb@tsmc.com

***Abstract*—Process variation has become a serious concern in nanometer technologies. Designs with competitive margins rely on well-characterized statistical models, which must predict the magnitude and scalability of variability accurately. In this paper, we propose a novel approach in creating the statistical models, which tracks the global variation correlation among logic and SRAM devices, hence more realistic. The simulation result is verified with TSMC N28 technology silicon. Two types of circuits, SRAM Vccmin calibration and a SRAM tracking circuit with logic, are discussed in this paper. Different simulation setups are applied on these two circuits to understand the impact of device correlation for the SRAM performance and design margin setting.**

Keywords - Process variation; Monte Carlo; Statistical model; Global variation; Local variation; Correlation; SRAM Vccmin, Tracking circuit.

I. INTRODUCTION

In most technologies, SRAM and logic devices usually share many process steps. As a result, they are impacted by the same global variation sources, such as oxide thickness, channel length, and width variations. Traditionally the SRAM and logic variation models are constructed relative independently. The global process variation correlation between SRAM and logic devices cannot be reflected using the worst-case corner simulation. For example, setting both the logic/SRAM model corners to fast assumes the variation correlation equal to 1. On the other hand, setting the logic model corner to fast and the SRAM model corner to slow assumes the variation correlation equal to -1. None of these corner combinations truly reflects the global process variation correlation between SRAM and logic devices. In view of this issue, we developed a new methodology for model providers to build this correlation through Monte Carlo simulation. We first characterize the global variation correlation coefficient by the data collected from two array structure test keys. A correlation matrix is then defined by these coefficients to describe the device correlation for paired devices within the chip. We demonstrate the advantages of this new modeling methodology on two applications with measured silicon data. The first case is SRAM Vccmin calibration. The correlation coefficients within SRAM cell between PG/PU/PD are examined. The result shows a different correlation coefficient setting on SRAM calibration could cause 30~50mV Vccmin shift easily. The second case is SRAM/Logic tracking circuit. In this case, the correlation matrix has been extended to include SRAM and logic devices. Using this new modeling methodology, the impact of correlation matrix designers can achieve more competitive designs with less design margins reserved.

II. MODELING METHODOLOGY

The statistical model for a single device type can be implemented based on measured/extracted SPICE parameters [1] or principle component analysis (PCA) approach [2][3]. The variation sources are usually represented by a set of independent random numbers with Gaussian distributions, which are directly or indirectly linked to the parameters in a compact model so that Monte Carlo simulation can perform. For example, a SPICE parameter (such as L, W, and Vth0, etc.) with variability can be presented by the following equation:

$$SP\_dev_1 = f_1(ran1\_dev_1, ran2\_dev_1, ran3\_dev_1, \cdots) \quad (1)$$

where SP_dev1 is a SPICE parameter for a given device (e.g. dev1) and ran{1,2,3..}_dev1 are independent random numbers representing the random global variation sources for dev1. Fig.1 below shows PCA based Monte Carlo model validation with TSMC N28 technology. Two electrical parameters shown in the plot are the current measured from two bias conditions. Both of the variation magnitude and correlation between these two parameters are well modeled. Since the electrical parameter correlation is defined and self-consistent within compact model, no additional correlation control is needed.

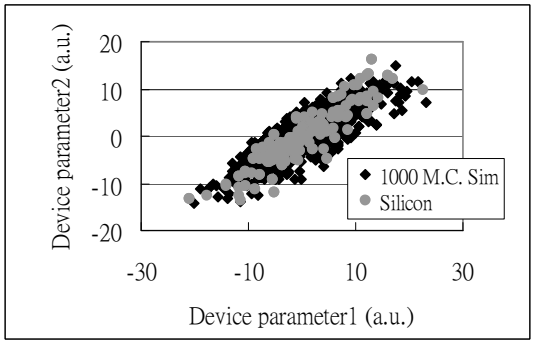

Figure 1. The validation for silicon and 1000 Monte Carlo runs. Two electrical parameters are device current measured at different bias conditions

A. Correlation between two devices

Similarly, the parameter variability of a different device type (dev2) can be expressed as

978-1-61284-418-3/11/$26.00 © 2011 IEEE

$$SP\_dev_2 = f_2(ran1\_dev_2, ran2\_dev_2, ran3\_dev_2, \cdots) \quad (2)$$

Traditional modeling approach either makes dev1 and dev2 uncorrelated or fully correlated, which may not be correct. An example is shown in Fig. 2.

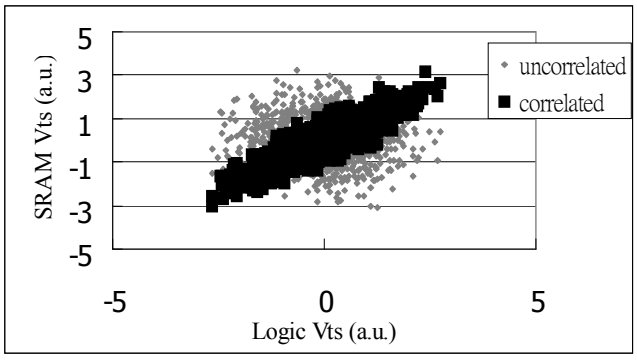

Figure 2. Two Simulation results for Logic and SRAM devices. One is with correlation coefficient R^2=0.9 and the other one is without any correlation.

In this work, we developed the following variability equations:

$$\begin{aligned} SP\_dev_1 &= f_1(ran1\_dev_1', ran2\_dev_1', ran3\_dev_1', \cdots) \\ SP\_dev_2 &= f_2(ran1\_dev_2', ran2\_dev_2', ran3\_dev_2', \cdots) \end{aligned} \quad (3)$$

where

$$\begin{aligned} ran1\_dev_1' &= ran1\_dev_1 \\ ran2\_dev_1' &= ran2\_dev_1 \\ ran1\_dev_2' &= w_1 \times ran1\_dev_1 + \sqrt{1-w_1^2} \times ran1\_dev_2 \\ ran2\_dev_2' &= w_1 \times ran2\_dev_1 + \sqrt{1-w_1^2} \times ran2\_dev_2 \end{aligned} \quad (4)$$

The equations are chosen so that the variability of the devices in Monte Carlo simulation is unchanged. However, the correlation between these two devices can now be controlled by the weighting factor, w_1, and can be characterized by data.

B. Correlation between two groups of devices

The methodology can be extended to the case for more than two devices. Before adding correlation information, the spice parameter variability equations are expressed as:

$$\begin{aligned} SP\_dev_1 &= f_1(ran1\_dev_1, ran2\_dev_1, ran3\_dev_1, \cdots) \\ SP\_dev_2 &= f_2(ran1\_dev_2, ran2\_dev_2, ran3\_dev_2, \cdots) \\ &\cdots \\ SP\_dev_m &= f_m(ran1\_dev_m, ran2\_dev_m, ran3\_dev_m, \cdots) \end{aligned} \quad (5)$$

To model the correlation among these devices, a correlation matrix is developed as shown in Fig. 3. Each element in the matrix represents the correlation coefficient (R) between any pair of devices. The weighting factor, $w_{i,j}$, is characterized from silicon or given specifications. In addition, the random numbers need to be reconstructed listed in Eq. (6) to reflect the correlation information specified in the correlation matrix while with no impact to the original variation magnitude applied in Eq. (5).

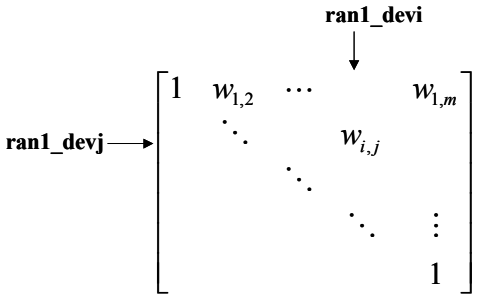

Figure 3. The correlation matrix for multiple devices. The weighting factor, Wij, represents the correlation coefficient between two devices.

$$\begin{aligned} ran1\_dev_1' &= A_1 ran1\_dev_1 + B_1 ran1\_dev_2 + \cdots + M_1 ran1\_dev_m \\ ran1\_dev_2' &= A_2 ran1\_dev_1 + B_2 ran1\_dev_2 + \cdots + M_2 ran1\_dev_m \\ &\vdots \\ ran1\_dev_m' &= A_m ran1\_dev_1 + B_m ran1\_dev_2 + \cdots + M_m ran1\_dev_m \end{aligned} \quad (6)$$

where, the coefficients used in the expression must satisfy the following conditions.

$$\begin{aligned} &A_1^2 + B_1^2 + \cdots + M_1^2 = 1 \\ &A_2^2 + B_2^2 + \cdots + M_2^2 = 1 \\ &\quad \cdots\cdots \\ &A_1 A_2 + B_1 B_2 + \cdots + M_1 M_2 = W_{1,2} \\ &\quad \cdots\cdots \\ &A_{m-1} A_m + B_{m-1} B_m + \cdots + M_{m-1} M_m = W_{m-1,m} \end{aligned} \quad (7)$$

SRAM and Logic devices have their own correlation coefficient matrices, R_SRAM and R_logic. Finally, we integrated them into a unified matrix. In this unified matrix, we can then add the correlation between login and SRAM devices as shown in Fig. 4.

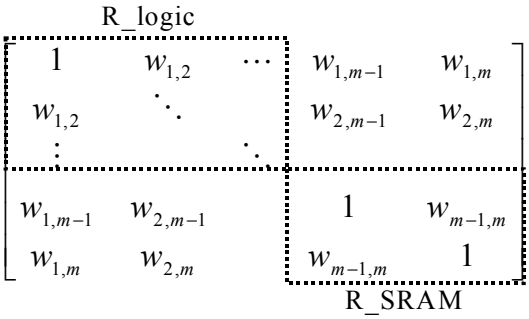

Figure 4. The correlation matrix for multiple SRAM and Logic devices. The weighting factor, Wij, represents the correlation coefficient between two devices.

C. Random number reduction

In practice, the size of the correlation matrix can be quite large as the number of logic and SRAM devices increasing.

This adds difficulty in creating/maintaining the model as well as characterizing cell libraries. To make this approach more feasible, we can reduce the number of random variables by applying another layer of PCA on the correlation matrix shown in Fig. 4 or by other means. With PCA, the random numbers used in Eq. (6) become

$$\begin{aligned} ran1\_dev_1' &= \alpha_1 pc_1 + \beta_1 pc_2 + \cdots + \nu_1 pc_n \\ ran1\_dev_2' &= \alpha_2 pc_1 + \beta_2 pc_2 + \cdots + \nu_2 pc_n \\ &\cdots \\ ran1\_dev_m' &= \alpha_m pc_1 + \beta_m pc_2 + \cdots + \nu_m pc_n \end{aligned} \quad (8)$$

where PC_1~PC_n are independent random numbers and α~ν are their associated coefficients obtained from PCA. The new ran1_dev$_1$' obtained from Eq. (8) can keep the same variation magnitude as that of ran1_dev$_1$~ ran1_dev$_m$ used in Eq. (5). In addition, the number of redefined principle components (n) is usually smaller or equal to the number of original random number (m). If the correlation coefficients in the matrix are not uniform among all the devices and dominated by a few selected devices, the random number reduction rate will be significant. The logic-SRAM joined correlation coefficient matrix described as Fig. 4 usually exhibit a similar pattern, so the random number reduction is an attractive enhancement to reduce the matrix size. Fig. 5 shows the comparison between the case with 20% reduction rate and the original one. It makes almost no impact to simulation results.

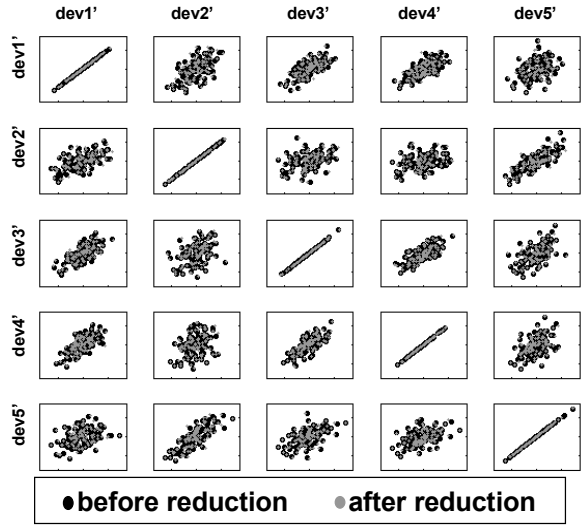

Figure 5. After random number reduction from 5 (black) to 4 (grey), the two set of results are still identical in terms of range and correlation.

III. IMPACT ON CIRCUIT DESIGN

In this section, we will discuss the impact of this new modeling methodology on circuit level. In the first case, the study focuses on a single type of device, a 6T SRAM Vccmin calibration, so the size of correlation matrix is still relatively small. In the second case, the discussion is on SRAM/Logic tracking circuit for the design margin setup. Due to the combination of SRAM and logic devices, the size of correlation matrix is bigger. As a result, the random number reduction is applied.

A. SRAM Vccmin calibration

The Vccmin calibration is a tough challenge for the technology and model engineers [4][5][6]. It involved with lots of modeling and measurement details. In this verification, the impact of correlation among 3 transistors, PG, PU and PD, within a 6T SRAM cell is reviewed. The first step is to construct the correlation coefficient matrix as shown in Fig. 3. Each element of the matrix is extracted from paired array structure. The plot below shows the silicon and model verification on the saturation threshold voltage (Vts) for PG/PD, PG/PU and PU/PD correlation respectively. Both variation magnitude and correlation have been characterized. Some correlation is observed between PG/PD. However, the correlation between PU/PD and PU/PG is relatively low.

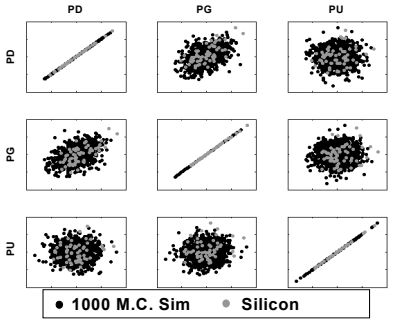

Figure 6. Correlation calibration for PG/PD/PU devices. PG/PD correlation is stronger than PG/PU and PD/PU correlation.

After calibrating the device level model characteristics and their corresponding correlation, the Vccmin distribution can be achieved through Monte Carlo simulation. The silicon and model matching is shown in Fig. 7. The simulation with calibrated correlation model matches the whole Vccmin silicon distribution closely. Another test case with R=1 for PG/PD is also attached in the same plot for comparison. Without a correct correlation model, it is easily found the matching is off, especially for the distribution tail. The gap between two models could be as large as 30~50mV for 95% Vccmin if the correlation is not calibrated properly. The impact could be bigger for the case with a larger global variation.

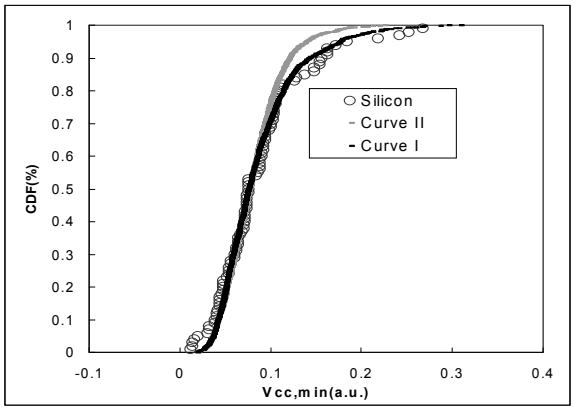

Figure 7. Vccmin simulation. Curve I: model with correct correlation. Curve II: Model with fully correlated PG/PD devices. There is a noticable gap at tail.

B. SRAM tracking circuit with logic

In this example, we review the impact of correlation to the design guard band setting. First of all, we characterized the correlation of global variations between logic and SRAM devices based on the saturation threshold voltage (Vts) from a TSMC N28 technology. The silicon and model simulation comparison is shown in Fig. 8. As shown in the plot, there is certain correlation between SRAM and logic.

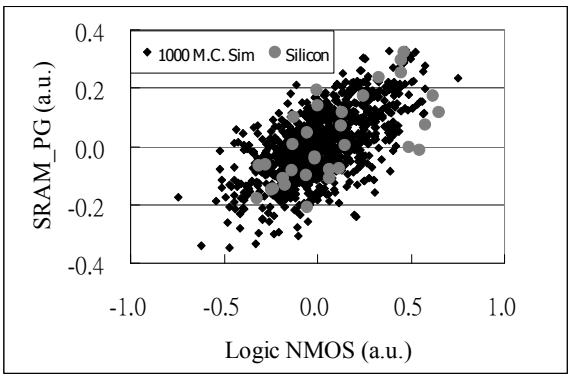

Figure 8. Silicon variation with 1000 M.C. runs for the correlation of logic and SRAM global variation. Both data are taken from array structures to eliminate the local variation.

Secondly, we examine the impact of global variation correlation of logic and SRAM device on a SRAM tracking circuit using the model created above. The SRAM tracking circuit is a logic delay chain for SRAM bit cell read performance monitoring. It is typically designed to provide a feedback control of word-line pulse width to ensure correct read operation. If there were no correlation, designers would need to ensure circuit functionality under the worst-case scenario, i.e. very fast logic devices and very slow SRAM devices. This would result in a very conservative design of the tracking circuit. If the correlation is built into the model, the design margin can be much reduced, as this extreme condition will not occur. The design margin defined here represents the extra word-line pulse width for SRAM to develop bit-line differential signal for sensing out. A larger design margin degrades SRAM performance and consumes more active power due to larger signal swing. Fig. 9 shows the simulation results with four different test cases. Method-1 uses corner simulation and assumes no correlation between logic and SRAM devices. It gives the smallest design margin. Method II applies two independent Monte-Carlo simulations of global variation. Even though we have not included the correlation, the design margin gains 10%. Method III is similar to Method II except that the correlation between logic and SRAM global variations is included. The design margin gains another 10%. Method IV assumes full correlation (R=1) and has the largest design margin, which is of course is too optimistic. This study tells us that the correlation in global variation between logic and SRAM devices must be well characterized and included in the model when doing Monte Carlo simulation in order to minimize the design margins reserved.

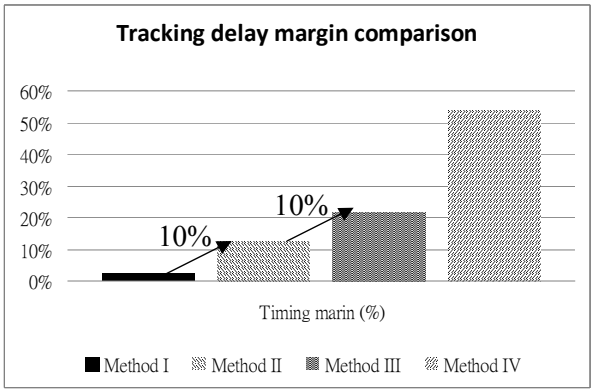

Figure 9. Method I: Corner without correlation; Method II: M.C. without correlation; Method III: M.C. with R^2=0.6; Method IV: M.C. with R=1. The design margin evaluation is the simulation setup dependent.

IV. CONCLUSION

In this paper, we demonstrated a new modeling methodology to reflect the correlation of global variations among different devices. Two examples are discussed, SRAM Vccmin calibration and SRAM/logic tracking circuit margin optimization. Different simulation setups are applied on these two circuits to understand the impact of device correlation. The noticeable difference is observed based on various correlation numbers. To reflect silicon behavior and achieve competitive designs, a well-characterized statistical model with a built-in global variation correlation is essential.

ACKNOWLEDGMENT

The authors want to express their gratitude to the help of H.H. Wang, Y.L. Chen, W.C. Lin and Quincy Li for the Vccmin calibration in this paper.

REFERENCES

[1] Kiyoshi Takeuchi and Masami Hane, "Statistical compact model parameter extraction by direct fitting to variations", IEEE Transactions on Electron Devices, vol. 55, no. 6, pp. 1487-1493, June, 2008.

[2] Kumud Singhal and V. Visvanathan, "Statistical Device Models from Worst Case Files and Electrical Test Data", IEEE Transactions on Semicoductor Manufacturing, vol. 12, no. 4, pp. 470-484, Novmember, 1999

[3] B. Cheng, N. Moezi, D. Dideban, G. Roy, S. Roy and A. Asenov, "Benchmarking the Accuracy of PCA Generated Statistical Compact Model Parameters Against Physical Device Simulation and Directly Extracted Statistical Parameters, International Conference on Simulation of Semiconductor Processes and Devices, 2009.

[4] Seevinck E, List F, Lohstroh J. "Static-noise margin analysis of MOS SRAM cells", IEEE Joural of Solid-State Circuits, Vol. 22, No. 5, October, 1987.

[5] Azeez J. Bhavnagarwala, Xinghai Tang, James D. Meindl, "The impact of Intrisic Device Fluctuations on CMOS SRAM Cell Stability", IEEE Joural of Solid-State Circuits, vol. 36, no. 4, April, 2001.

[6] Wang Y, Bhattacharya U, Hamzaoglu F, et al. "A 4.0 GHz 291 Mb voltage-scalable SRAM design in 32 nm high-κmetal-gate CMOS with integrated power management". IEEE International Solid-State Circuits Conference, 2009.