An Abnormal Floating Gate Interference and a Low Program Performance in 2y nm NAND Flash Devices

Eunmee Kwon, Dongyean Oh, Bonghoon Lee, Jeong-hyong Yi, Sangyong Kim, Gyuseog Cho, Sungkye Park, and Jaehoon Choi

R&D Division, Hynix Semiconductor Inc., San 136-1 Ami, Bubal, Icheon, Gyeonggi, 467-701, Korea, emkwon@hynix.com

Abstract— We have investigated a mechanism for an abnormally large floating gate (FG) interference reported in 2y nm NAND flash device. Based on the experimental and simulation results, we have found that the root cause is attributed to a depletion of polysilicon (poly-Si) layer for the control gate (CG). It was also found that the poly-Si depletion gives deterioration in the program performance. This work suggests that the poly-Si depletion of the CG should be controlled and considered utilizing a full 3-dimensional (3D) TCAD process and device simulations to improve the FG interference and the performance of NAND flash device beyond 2y nm technology.

Keywords-component; Poly depletion; Interference; NAND flash; 3D TCAD simulation

I. INTRODUCTION

It is widely known that the FG interference has increased due to increasing of the parasitic capacitance coupling as the NAND flash cell is scaled down. It gives result a threshold voltage shift (Δ Vth) for a victim cell during cell operation. Recently it has been reported that an extrinsic FG-to-channel coupling called 'direct coupling' makes a stronger effect on the FG interference than an intrinsic FG-to-FG coupling below 50 nm technology [1]. Therefore, it is necessary of 3D structure for simulation work to consider all capacitance couplings in NAND flash cells [2].

In general, a highly doped n-type poly-Si layer is used as the CG electrode for NAND flash cell transistors. However, there will occur of dopant out-diffusion inevitable from the poly-Si layer during the post processes of oxidation and etching [3]. According to device size scaling, the dopant outdiffusion becomes more serious and gives rise to an unwanted depletion layer in poly-Si gate under the read or program/erase operations.

In this paper, we propose a model to explain a bit-line interference phenomenon and a low program performance caused by the poly-Si depletion of the CG for the first time.

II. MODEL DESCRIPTION

The 'bit-line interference' is defined as a \triangle Vth of a victim cell when the state of neighbor cells is changed from erased (lower Vth) to programmed (higher Vth) one. Because a threshold voltage of the victim cell in NAND string should be affected by the FG voltage changes of cells located in nearby bit-line. The amount of voltage change in FG (\triangle Vfg) can be expressed in terms of the BL-to-BL coupling capacitance and the total capacitance for a cell as follows:

$$\triangle V_{fg}^{Victim} = \frac{2 \cdot C_{BL}}{C_{Total}} \cdot \triangle V_{fg}^{BL} + \alpha \cdot C_{FGCH} \cdot \triangle V_{fg}^{BL}$$
(1)

, where

Cbl :	BL to BL coupling capacitance,
Cfgch :	FG to channel coupling capacitance,
CTotal :	Total capacitance,
α	Direct coupling factor.

We have constructed a 3D NAND flash cell structure, as depicted in Fig. 1(a), using a full 3D process simulator. Also described in Fig. 1(b), we have considered two kinds of capacitance coupling of FG-to-FG and FG-to-channel in this study. As the cell size becomes about 20-nm, the distance between an edge of the channel and floating gate of a neighboring cell transistor is so close that the floating gate voltage of the neighboring cell directly influences on the channel of victim cell and changes the electric field distribution at the channel edge. As a result, the cell Vth of victim cell changes due to the direct field effect [1].

III. SIMULATION RESULTS AND DISCUSSION

A measured and simulated FG interference along bit-line direction (BL interference) with variables of technology node is shown in Fig. 2. The obtained simulation results are based on

the intrinsic and extrinsic capacitance coupling depicted in Fig 1(b). As shown in Fig. 2, there begins a discrepancy between simulation and measurement below 20-nm technology node. The BL interference as a function of victim cell's Vth are plotted in Fig. 3. The simulation results are consistent with the measured ones when the victim cell is an erase state, while the measured BL interference shows an opposite tendency when the victim cell is a program state. The actual BL interference increases drastically in proportion to the Vth of victim cell in programmed state.

In order to find out such an abnormal interference phenomenon dependent on victim cell's state, we have noticed the poly-Si depletion and taken the dopant concentration of poly-Si as simulation variables into consideration. Fig. 4(a) shows a 3D simulation structure consists of one victim cell (front center cell in this work) with five neighboring cells around it. We have compared the potential distribution and poly-Si depletion according to the state of the neighboring cell in adjacent bit-line (backside center cell in Fig. 4(a)) as erased (negative Vth) and programmed (positive Vth) one, respectively. Also a poly depletion of CG in 2D along the bitline direction according to different states of neighbor FG is shown in Fig. 4(b). As can be seen in Fig. 4(a) and 4(b), it is obvious that there occurs nearly full poly depletion in the inner poly-Si layer when the neighbor FG is of a program state, while very little depletion when the neighbor FG is of an erase state. We have deduced that the different poly depletion according to neighboring cell state may cause the victim cell's Vth shift because of gate coupling reduction due to the depletion capacitance. The observed abnormal BL interference dependant on victim cell's state under a low poly-Si concentration can be explained as follows:

(1) When the victim cell is of a program state, there occurs different poly depletion at the inner poly region of CG according to the state of neighbor FG and happens Vth shift increasing due to the bit-line interference. Fig. 5 shows the potential distribution of poly-Si at the read bias of 3V. Compared to Fig. 4(a) and (b) case of read bias of 1 V, the poly depletion occurs even though the neighbor FG is of an erase state. On the other hand, when the victim cell is programmed and its Vth is high enough, then the poly depletion does not depend on the neighbor FG potential. Therefore, the Vth due to the bit-line interference may be reduced.

(2) When the victim cell is of an erase state, the poly depletion happens even in FG as shown in Fig. 6. The poly depletion of FG happens at the interface of inter-poly-dielectric (IPD) when the neighbor FG is an erase state, while it becomes more expanding when the neighbor FG is a program state. So the victim cell Vth increases in the positive direction.

Next, we have examined poly-Si concentration effect on BL interference. As can be seen in Fig. 7, the Δ Vth of victim cell has increased dramatically in case of low concentration of CG poly-Si and FG poly-Si when the victim cell is of a program state and erase state, respectively.

The poly depletion gives problem such as program speed reduction besides BL interference. Fig. 8(a) represents the simulation results of a potential drop due to the CG poly depletion as a function of program bias. The depletion width at the inner poly-Si region becomes narrow even at high gate bias in case of high poly-Si concentration for CG, while it has large depletion even if low program bias is applied in case of low concentration. The poly depletion causes FN tunneling reduction due to a potential drop and leads to low program Vth. The simulated potential drop at the bottom of CG and the programmed Vth as a function of CG poly-Si concentration are shown in Fig. 8 (b) and Fig. 9, respectively.

According to our expectation, we obtained improved BL interference by implementing high CG poly-Si concentration in our 2y nm NAND flash device, which is shown in Fig. 10.

IV. CONCLUSION

It is found that an abnormally large Vth shift of victim cell (BL interference) appeared in 2y nm NAND flash device is attributed to the poly-Si depletion of the CG. In case of low poly-Si concentration, the poly depletion happens at the inner CG poly-Si region even at a low gate bias. The poly depletion causes an abnormal interference and a FN tunneling reduction due to the potential drop across depletion layer.

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Figure 1(a). 3D simulated 3X3 array of Flash device



Figure 1(b). 3D Bit-line Interference due to FG-to-FG coupling & FG-to-channel coupling



Figure 2. As active CD decreases below 20 nm, BL interference increased drastically.



Neighbor WL Neighbor BL Poly depletion <Neighbor BL Cell=ERS> <Neighbor BL Cell=PGM>

Figure 4(a). Electrical potential and poly depletion (victim cell Vth=1V $% \left(V_{1}^{2}\right) =0$



<Neighbor BL Cell=ERS> <Neighbor BL Cell=PGM>

Figure 5. Electrical potential and poly depletion. (victim cell Vth=3V, CG bias=3V)



Figure 3. Measurement of BL interference as a function of victim cell Vth. BL interference increases abnormally when victim cell Vth is between 1V and 4V in 2y nm Flash device.



<Neighbor BL Cell=ERS> <Neighbor BL Cell=PGM>

Figure 4(b). 2D plot (CG poly depletion is increased when victim cell Vth is 1V, due to the change of neighbor FG potential)



Figure 6. Electrical potential and poly depletion. (victim cell Vth=-3V)



Figure 7. Simulation of BL interference as a function of victim cell Vth.





Figure 8(b). Electrical potential at the bottom of CG poly-Si as a function of program bias



Figure 9. Simulation result of PGM Vth as a function of CG poly concentration



Figure 10. Measurement of BL interference as a function of victim cell Vth.