# Modeling Temperature and Bias Stress Effects on Threshold Voltage of a-Si:H TFTs for Gate Driver Circuit Simulation

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***Abstract*—Hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFT) have been important device in modern display panel production. In this paper, we study amorphous silicon thin-film-transistor (TFT) degradation under temperature and bias stresses. Rensselear polytechnic institute (RPI) model is widely used for circuit simulation of a-Si:H TFTs, but the temperature (T = -20 - +65°C) and bias stress effects are not considered in the RPI model. The parameters of sub-threshold in the RPI model with temperature and bias stress effects are explored and formulated with the measured I-V data. The results can be used together with the existing model, and thus can describe the temperature dependent characteristics of a-Si:H TFTs well. A 14 a-Si:H TFTs integrated gate (ASG) driver circuit is simulated and tested using the modified RPI model card. The simulations predict the temperature effect on the dynamic properties of ASG circuit and power consumption.**

***Keywords: Amorphous silicon TFT, bias stress effect, temperature effect, threshold voltage, Rensselaer Polytechnic Institute (RPI) model, circuit simulation, RPI model, power comsumption, ASG circuit.***

## I. INTRODUCTION

Amorphous silicon thin-film transistors (a-Si:H TFTs) have been widely used in active-matrix backplanes for LCD displays on glass [1-2]. Figure 1 shows the structure and image of transmission and scanning electron microscope (TEM and SEM) of a fabricated TFT sample. Unfortunately, DC and dynamic characteristics of a-Si:H TFTs are sensitive with operational environment [3]; in particular, they suffer form electric-field-induced threshold voltage shift [4-6]. Figure 2 shows DC characteristics of fabricated samples with temperature variation. We find the drain current significantly increases with the increase of temperature. As shown in Fig. 3,

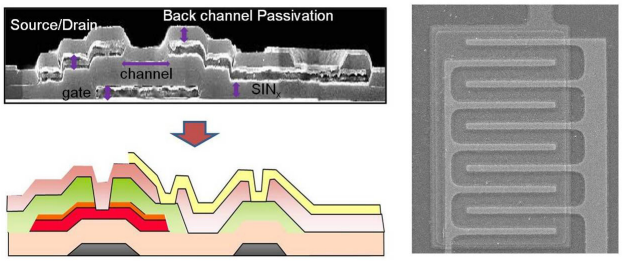


Fig. 1. Cross-sectional and fabricated inverted staggered a-Si:H TFTs and the SEM image.

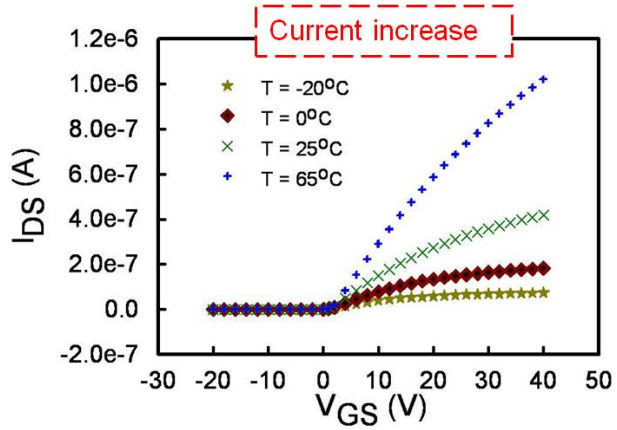


Fig. 2. The $I_{DS}$-$V_{GS}$ characteristics of the fabricated samples with temperature, where gate length / width = 5 μm / 26.5 μm, gate bias $V_{GS}$ = -20 V to 40 V, drain bias ($V_{DS}$) = 0.5 V and temperature (T) = -20°C, 0°C, 25°C and 65°C.

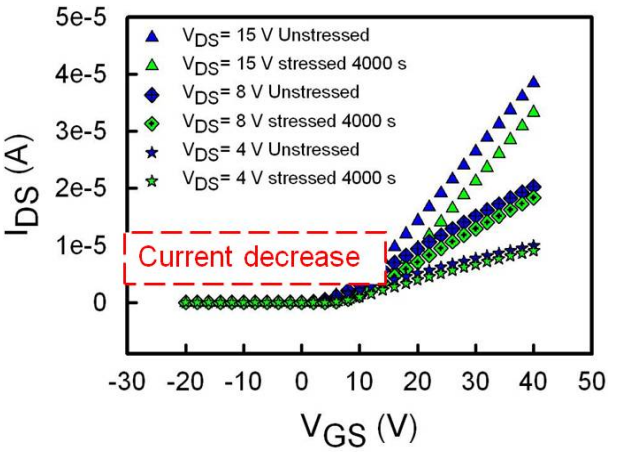


Fig. 3. The $I_{DS}$-$V_{GS}$ characteristics of the fabricated samples with and without stress, where gate length / width = 4 μm / 26.5 μm, gate bias of stress ($V_{GS}$) = 28 V, drain bias ($V_{DS}$) = 0 V and temperature (T) = 65°C.

when TFTs are stressed for a long time, the threshold voltage increases and current decreases. The RPI model with appropriate parameters achieves reliable result for circuit simulation [7-9]. From the results of Figs. 1 and 2, if we would like to obtain thoroughgoing effects with various operational environments, we must consider the temperature and bias stress effects simultaneously. However, the dependence of device's DC characteristics and ASG driver circuit's dynamic properties including power consumption on temperature and bias stress

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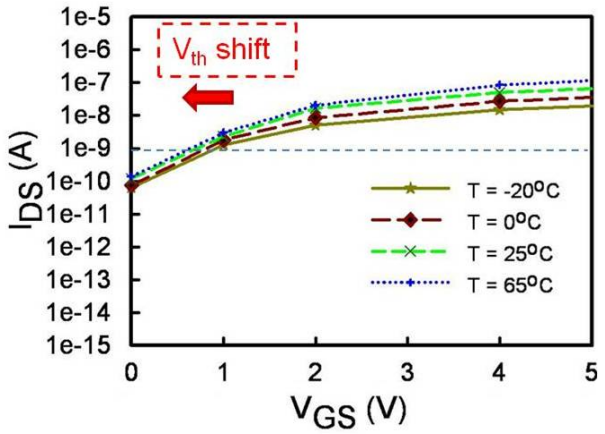


Fig. 4. The $I_{DS}$-$V_{GS}$ characteristics (in log scale) of the fabricated samples with temperature, where gate length / width = 5 μm / 26.5 μm.

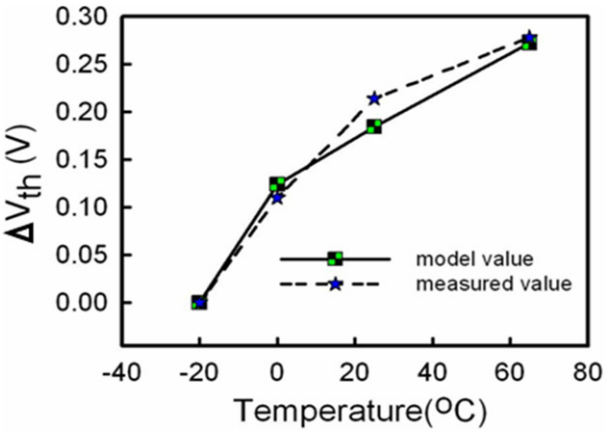


Fig. 5. Measured data and model result of threshold voltage shift of $V_{th}$ ($\Delta V_{th}$ ), where the dash and solid lines are the measured and calibrated data of Eqs. (2).

effect has not been clear yet. In this work, we first model the characteristics of a-Si:H TFT with considering the effect of temperature variation and bias stress, then the ASG driver circuit using the advanced RPI model modified by proposed equations are simulated. The results of this study successfully reveal the temperature and bias effects on ASG driver circuit's dynamic properties. In Sec. II, we describe the bias stress and temperature effect as well as the modeled equations. In Sec. III, we extract the parameters of the modeled equations. In Sec. IV, we state the circuit to be simulated. In Sec. V, we report the results including engineering discussions. Finally, we draw conclusions and suggest future work.

## II. The Temperature and Bias Stress Effects of the Threshold Voltage

First, we use constant current process to define the threshold voltage. The definition of threshold voltage in the process is that the drain current equals to 1 nA as the drain voltage is 0.5 V. As shown in Fig. 4, the threshold voltage increases by the increase of temperature (T = -20°C, 0°C, 25°C and 65°C), thus the threshold voltage is modeled as:

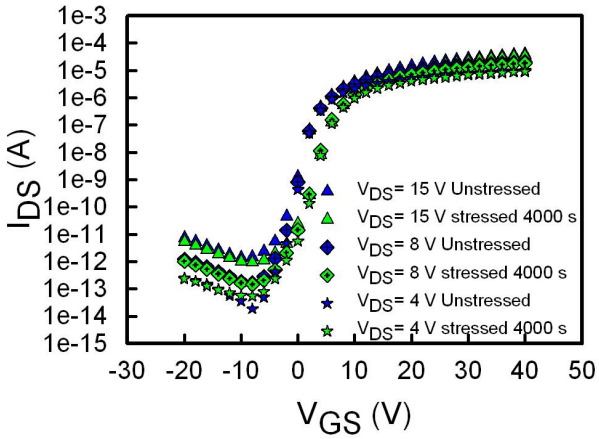


Fig. 6. The $I_{DS}$-$V_{GS}$ characteristics (in log scale) of the fabricated samples with temperature = 65°C, Stress voltage is $V_{GS}$ = 28 V and $V_{DS}$ = 0.4 V; Stress time = 0 and 4000 s, where the gate length / width = 4 μm / 26.5 μm.

$$V_{th}(T) = V_{th}(T_o) + \Delta V_{th}, \tag{1}$$

where $T$ is the operational temperature, $T_o$ is the initial temperature, and $\Delta V_{th}$ is given as

$$\Delta V_{th}(T) = A \cdot (T - T_o)^{\beta} \cdot \exp\left(-\frac{E_A}{kT}\right), \tag{2}$$

where $k$ is the Boltzmann constant, $A$ and $\beta$ are temperature-dependent parameters, $E_A$ is the mean activation energy. In this sample, we use a nonlinear regressing analysis with iteration process to get $A$ = 0.175, $\beta$ = 0.3643, and $E_A$ = 0.0267eV, respectively, as shown in Fig. 5. However, the results of temperature effect can not show a complete characteristics of a:Si TFTs. Fig. 6 shows the TFT sample degradation induced by the bias stress varying from $V_{GS}$ -20 to 40 V with three values of $V_{ds}$ (4, 8 and 15 V). Therefore, if we are interested in obtaining a robust compact model, we must consider the effects of bias stress and temperature simultaneously. As shown in Fig. 7, the threshold voltage increases rapidly at the beginning of stressing and it saturates after 4000 sec. as T = 65°C which is one of 4 sets of the measurement data (they are 25, 45, 65, and 85°C, respectively). The threshold voltage varies with the stress time can be modeled as

$$V_{th}(t) = V_{th}(0) + \Delta V_{th}. \tag{3}$$

According to [10] a semi-empirical description is approximated to the shift of threshold voltage:

$$\Delta V_{th}(t) = A_{ts} \cdot t^{\beta_{ts}} \cdot \exp\left(-\frac{E_{ta}}{kT}\right). \tag{4}$$

Figure 8 shows the $V_{th}$ shift with increasing stress time, where $k$ is the Boltzmann constant, $E_{ta}$ is the mean activation energy, $A_{ts}$ and $\beta_{ts}$ are two constants to be determined. We use a nonlinear regressing analysis with iteration process to get $A_{ts}$ = 23016, $\beta_{ts}$ = 0.4592, and $E_{ta}$ = 0.3771 eV, respectively.

## III. The Temperature and Bias Stressed Parameters

Before circuit simulation, we have to extract all parameters of the modeled stress bias and temperature effects in order to obtain the corresponding model cards first for all regions. In our laboratory, we have developed a parameter extraction software, ECAD (Extract Computer Aided Design) [11-12], based on the RPI model. The RPI model is a kind of compact models for amorphous silicon TFT devices [1]. According to the extraction method, we can extract all the regions and get the values of model parameters that are needed in the circuit simulation. Roughly, we divide the characteristic curves into

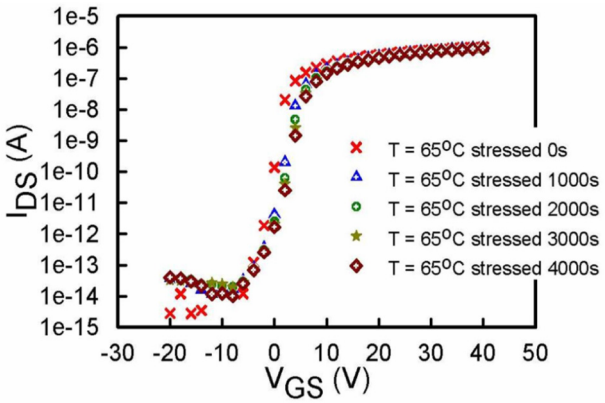


Fig. 7. The $I_{DS}$-$V_{GS}$ characteristics (in log scale) of the fabricated samples with temperature = 65°C, Stress voltage $V_{GS}$ = 28 V, $V_{DS}$ = 0.4 V, Stress time = 0 to 4000 s, where gate length / width = 4 μm / 26.5 μm.

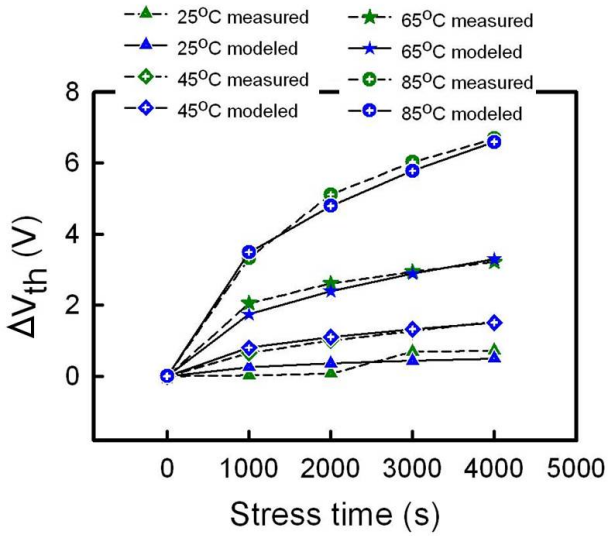


Fig. 8. Measured data and model result of the threshold voltage, where the model result is estimated from Eq. (4).

three parts: the linear region, the saturation region and the leakage region, and then extract the related parameters of these regions with 5% error tolerance, respectively. Figs. 9 and 10 have pointed out all extraction regions and the associated parameters. In summary, we integrate the parameter values and use the RPI extraction procedure to obtain a set of complete model card. Table 1 shows the errors of measured data compared with extracted data in the linear, threshold and saturation regions, as the bias stress time varying from 0 to 4000 sec. and the temperature is equal to 25°C and 85°C, respectively.

Table 1. The errors of the measured result compare with the extracted data with bias stress time under T = 25 and 85°C.

| Error table for measured result compare to extracted data | | | |
|---|---|---|---|
| Region / Stress Time(s) | Leaner (%) | threshold (%) | saturation (%) |
| 0 T = 25°C | 0.38 | 2.13 | 0.98 |
| 1000 T = 25°C | 0.74 | 2.56 | 0.79 |
| 2000 T = 25°C | 0.62 | 2.43 | 0.92 |
| 3000 T = 25°C | 0.63 | 2.66 | 0.56 |
| 4000 T = 25°C | 0.71 | 2.78 | 0.86 |
| 0 T = 85°C | 0.68 | 2.77 | 0.88 |
| 1000 T = 85°C | 0.69 | 2.86 | 0.86 |
| 2000 T = 85°C | 0.86 | 2.23 | 0.79 |
| 3000 T = 85°C | 0.52 | 2.49 | 0.96 |
| 4000 T = 85°C | 0.77 | 2.68 | 0.91 |

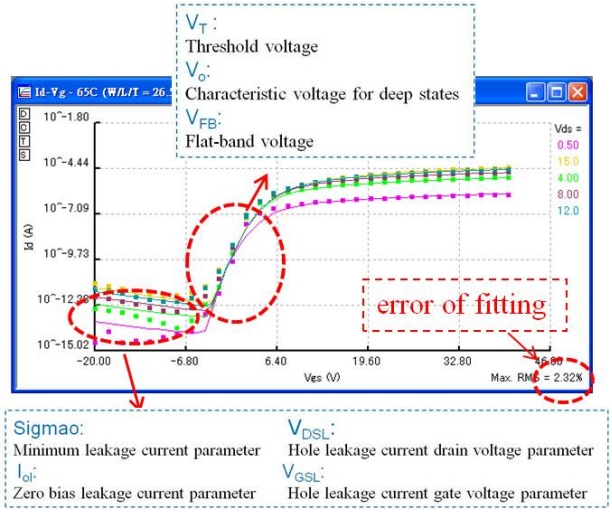


Fig. 9. Extracted region and parameters of I-V curve for a-Si:H TFT using the RPI parameter extraction software ECAD.

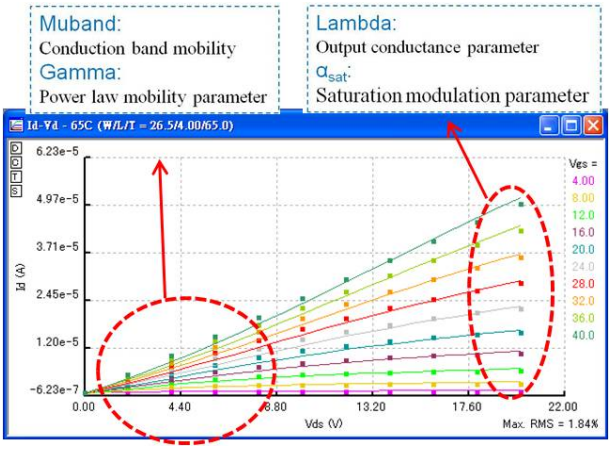


Fig. 10. Extracted region and parameters of I-V curve for a-Si:H TFT in RPI parameter extraction software.

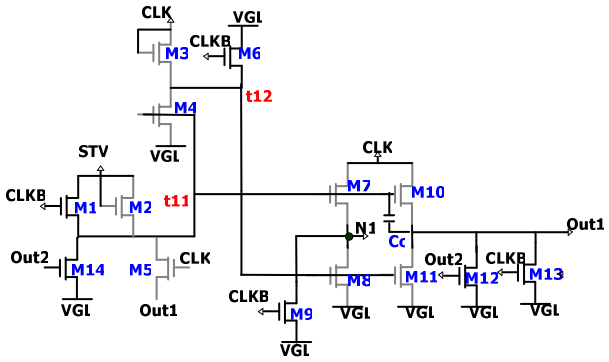


Fig. 11. The tested TFT-LCD driver circuit (denoted as ASG driver circuit) in this work. The a-Si:H TFTs' circuit has fourteen transistors and four capacitance. The bias stress effect of a-Si:H TFTs on ASG circuit is modeled and simulated based upon the calibrated model.

Table 2. The simulated power consumption with respect to different temperatures and under the bias stress time 1000, 2000, 3000, and 4000 sec. of the ASG driver circuit.

| Compared characteristic of power consumption for circuit simulation | | | | |
|---|---|---|---|---|
| T (°C) | Stress time 1000 (s) | Stress time 2000 (s) | Stress time 3000 (s) | Stress time 4000 (s) |
| 25 | 197.65 μW | 196.49 μW | 194.31 μW | 194.09 μW |
| 45 | 199.81 μW | 199.21 μW | 197.12 μW | 195.69 μW |
| 65 | 200.15 μW | 192.82 μW | 189.92 μW | 188.61 μW |
| 85 | 202.14 μW | 195.67 μW | 183.99 μW | 178.78 μW |

## IV. Application to ASG Circuit Simulation

As conventional design, the gate IC's and display panel are fabricated individually and combined each other by bonding process. However, bonding process may result mechanical reliability problem. In on-going design, the a-Si: H TFT gate (ASG) driver circuits integrated on glass have been proposed to handle reliability and give several advantages: mature manufacturing technology, low temperature, low-cost processing, and elimination of the driver ICs.

In this experiment, we apply the proposed equation with the RPI model cards for ASG driver circuit simulation under bias stress and different temperatures. The ASG driver circuit of 14 a-Si:H TFTs, as shown in Fig. 11, is the most critical component in GOP (gate-on-panel) design in display industry [13]. The circuit sends the pulses to drive the pixels on panel, but the quality of it may be seriously affected by the bias stress time and the temperature of operational environment. In fact, the reason is mainly from the threshold voltage shift. The power consumption of the ASG driver circuit is given by

$$P = f \cdot c \cdot v^2, \tag{5}$$

In Eq. (5), $f$ is the frequency of the driving clock signal, $c$ is the capacitance from clock input node, and $v$ is the deviation of high and low voltage level applied on the circuit. Table 2 lists the comparison of power consumption of various bias stress times and temperatures. The negative correlations between stress time and power at each temperature are obvious, but if the stress time is fixed, there are no general trends of power among different temperatures. The reason is that the effects of stress are stronger under high temperature environment.

## V. Conclusions

In this work, we have presented the parameter extraction procedure for modeling bias stress effect on threshold voltage variation of a-Si:H TFTs, based up on RPI model, in TFT-LCD circuit simulation. By considering stress bias, stress time, and operation temperature, the bias stress effect on the threshold voltage has been modeled and calibrated with measured samples. This model can be incorporated into TFT-LCD circuit simulation for reliability issues. We are currently designing and fabricating samples with wide range of device length and width, different temperature and bias stress at the same time for more robust compact modeling.

## Acknowledgment

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