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Reliability of NAND Flash Memories Induced by Anode Hole Generation in Floating-Gate

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Abstract— **We have developed a prediction model of program/erase endurance for NAND flash memory cell. Program/erase simulations of the life-time of the tunnel oxide based on the anode hole injection model are carried out for the NAND flash memory cell structure with various floating gate lengths. The anode hole-generation model is implemented in our device simulation and the simulation in consistent with actual circuit operation has been carried out. It is revealed that the concentration of holes at the edges of the floating gate has an impact on the life time of the tunneling oxide. The present simulation scheme has capable of estimating the dependence of the program/erase cycles to breakdown on the effect of the gate edge current in conjunction with the storage density.**

Keywords-Memory; NAND; simulation; breakdown; AHI

I. Introduction

As flash memory devices have recently reached the deca-nano-meter scale, reliability has become a critical issue. In particular, the tunnel oxide degradation in the deca-nano-meter flash memories is an important problem to be clarified. In a recent study using numerical simulation, NAND cells degrade, such as the threshold voltage shift and data retention characteristics, owing to the tunnel oxide degradation caused by increasing local tunneling current on the floating gate edge during program/erase operation [1]-[2]. Additionally, the NAND cell characteristics are degraded by the holes caused by high-energy electrons injected into the floating gate, since the NAND flash memory uses the Fowler-Nordheim tunneling phenomenon during the program/erase operation [3]. The anode hole generation in the floating gate must cause the degradation, such as traps that induce the threshold voltage shift and, ultimately, the breakdown.

In this study, an approach to predict the program/erase endurance of the NAND flash memory cell is suggested, considering the anode hole-generation model [4]-[7], which is implemented in the device simulation to consider the actual device structure and program/erase operation.

II. Simulation Model

Figure 1 shows a schematic of the anode hole-generation and that schematic of the program/erase operation of the NAND flash memory cell.

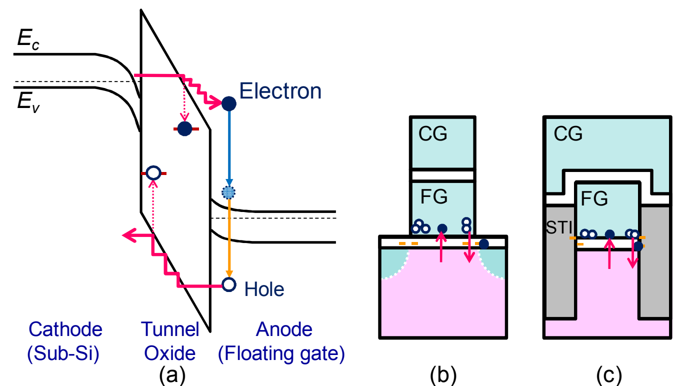

Figure 1. (a) Diagram of anode hole injection in NAND flash memory cell. (b) Cross-sectional view along bit-line direction. (c) Cross-sectional view along word-line direction.

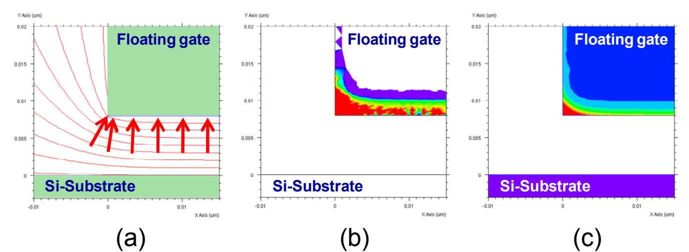

Figure 2. Simulation results in programming condition with L = 30nm NAND flash memory cell. (a) Potential contour plot and illustration of Fowler-Nordheim current flow on floating gate left edge. (b) Quantum efficiency of hole contour plot. (c) Hole concentration contour plot.

A feature of the phenomenon in the flash memory is that the generation takes place in the floating gate, as shown in Fig. 2.

The anode hole injection model is adopted to estimate the time-to-breakdown. In this model, the breakdown mechanism is based on the positive feedback of electrons injected from the cathode, hole generation due to impact ionization and subsequent hole drift to the cathode, and localized field enhancement at the cathode interface due to hole trapping. These injected holes act to increase the current density, through hole-induced trap generation, until the final process leads to breakdown.

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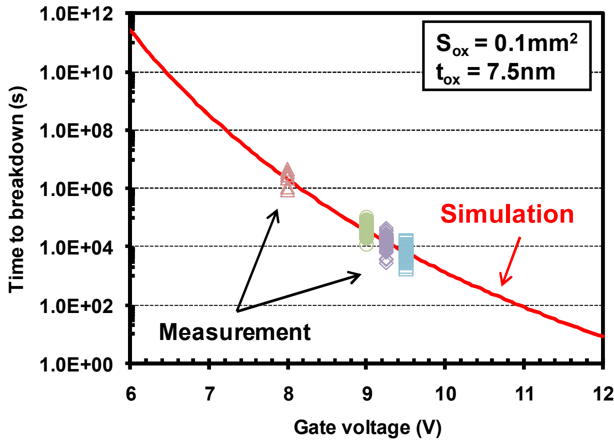


Figure 3. Comparison of time-dependent dielectric breakdown simulations with measurements. Dots indicate measurement results. The solid line indicate simulation results using the anode hole injection model.

The time-to breakdown t_{BD} is given as

$$t_{BD}(t_{ox}, V_{ox}) = Q_{BD}(t_{ox}, V_{ox}) / J_e(t_{ox}, V_{ox}), \qquad (1)$$

where

$$Q_{BD}(t_{ox}, V_{ox}) = Q_p(t_{ox}) / \gamma(E_{gain}(V_{ox})), \qquad (2)$$

$$J_e(t_{ox}, V_{ox}) = \alpha\, E_{ox}^2 \exp(-\beta / E_{ox}). \qquad (3)$$

Here t_{ox} and V_{ox} are the tunnel oxide thickness and applied voltage on the tunnel oxide respectively, Q_{BD} is the charge to breakdown and J_e is the Fowler-Nordheim tunneling current density through the tunnel oxide. Q_p is the hole charge to breakdown. γ and E_{gain} are the impact ionization probability and arrival energy of electrons at the anode, respectively. The simulation results reproduce the results of typical time-dependent dielectric breakdown measurements, as shown in Fig. 3.

III. Simulation Method

In the operation of NAND flash memories, the control gate voltage generates a strong electric field between the floating gate and silicon substrate, by which electrons are injected into or from the floating gate with a tunneling effect. As shown in Fig. 2, the electric field concentrates at the edge of a floating gate and, hence, the tunneling current density is large at the edge compared with at the center of the channel. From this viewpoint, we study the edge current concentration effect quantitatively with a one-dimensional analytical simulation model, which is independent of the structure, and a two-dimensional numerical device simulation model which is dependent on the structure. By comparing the 1D analytical model simulation results with the 2D device simulation results, the effect of the edge is determined.

A. 1D analytical simulation model

To gain insight into the basic NAND cell program/erase operation excluding the structure effect, such as the parasitic capacitance and field concentration, we use the simplified 1D analytical simulation model [9].

Assuming that the floating gate is capacitively coupled to only the control gate and substrate, the floating gate voltage V_{FG} is calculated from a capacitive equivalent circuit of the cell as

$$V_{FG} = V_{CG}\, Cr + Q_{FG} / (C_{IDP} + C_{ox}) \qquad (4)$$

where V_{CG} is the applied control gate voltage, Q_{FG} is the stored charge on the floating gate, $dQ_{FG}/dt = J_e\, S_{ox}$, and C_{IPD} and C_{ox} are the inter-poly-dielectric capacitance and tunnel oxide capacitance between the floating gate and substrate, respectively. S_{ox} is the tunnel oxide area. The coupling ratio Cr is calculated as $Cr = C_{IPD} / (C_{IPD} + C_{ox})$.

Using equations (3) and (4), the floating gate potential and injected electrons are calculated. The hole through the tunnel oxide and the time-dependent dielectric breakdown are calculated using equations (1) and (2). Although, in the bipolar stress such as program/erase operation, the life-time of the oxide is longer than that in the unipolar stress owing to the de-trapping of electron in the tunnel oxide [10], this effect is not taken into account in this calculation.

TABLE I. Values Used for 1D and 2D Simulation Models.

Symbol	*Description*	*Value*	*Unit*
t_{ox}	Tunnel oxide thickness	8.0	nm
t_{IPD}	Inter-Poly-dielectric thickness	12.0	nm
ε_{IPD}	Inter-Poly-dielectric permittivity	7.77e-13	F/cm
L	Floating gate length	10~500	nm
W	Floating gate width	10~500	nm

The number of program/erase pulse to dielectric breakdown is calculated using the accumulated weight of each hole passing through the tunnel oxide.

B. 2D numerical device simulation model

To investigate the effect of tunnel current concentration on the floating gate edge, we performed 2D TCAD device simulations on a typical device structure shown in Fig. 1. The current densities of electrons are calculated using the WKB approximation, and the tunneling currents are fed back to the generation recombination term of the current continuity equation in our 2D device simulator. Program/erase simulations are carried out for the NAND flash memory cell structure with various floating gate lengths.

It is confirmed that the 1D analytical model results are consistent with those of the 2D device simulation in the large-channel device structure.

IV. Simulation Results

The generated hot holes in the floating gate affect the endurance characteristics, that is, the number of program/erase cycles to breakdown for the flash memory. Figure 4 shows the hot holes generation efficiency during program/erase operations and the total hot holes density that through the tunnel oxide, which is a practical indicator of the progress of oxide degradation. The effect of the actual circuit operation, such as the polarity dependence of the degradation, is taken into account, as shown in Fig. 4 (a). Due to the hole generation depends on the injected electrons, many of the hot holes through the tunnel oxide when the program/erase voltage changes abruptly, as shown in Fig. 4 (b). This results indicate that the tunnel oxide degradation is proceed when the program/erase voltage is applied.

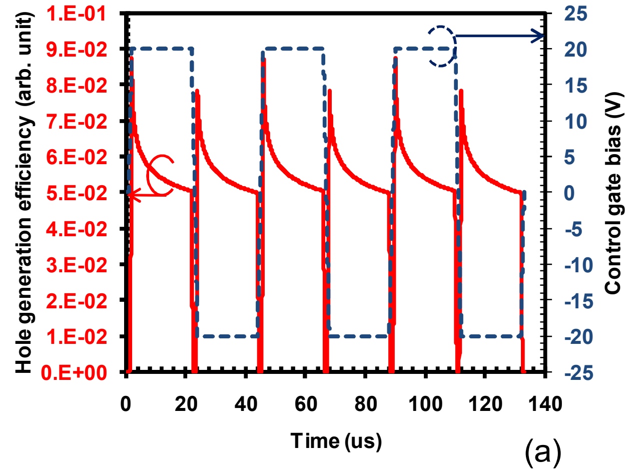
The hot hole generation that degrades the tunnel oxide takes place at the edge of the floating gate in programming condition caused by the tunneling current crowding, as shown in Fig. 2. The tunneling current crowding effect at the gate edge is calculated in the 2D device simulation. Figure 5 shows that the edge current crowding significantly affect the life-time of the tunnel oxide. This indicates that the number of holes through the tunnel oxide depends on the gate length by the effect of the tunneling current crowding. As the floating gate channel length decreases, the hole concentration at the gate edge increase caused by crowding effect. This result suggests that the tunneling current crowding at the gate edge cannot be ignored in a short- channel device.

Figure 6 shows the number of program/erase cycles to breakdown for each generation. This result indicates that the average tunneling current increases owing to the edge effect, such as the edge current crowding. The reliability perspective is important for the storage density and production yield. Moreover, the generated holes degrade the cell reliability caused by the trap site generation in the tunnel oxide.

Although we have considered only the polarity dependence, the tunneling current density at the gate edge increase caused by field concentration in erasing condition [2]. Furthermore, this calculation is performed by the 2D cross-sectional model along bit-line direction, the channel area of the memory cells is separated by shallow trench isolation (STI) as shown Fig. 1 (c). Therefore, as the device size becomes smaller, the effect of electric field crowding at the edge of the cell active area becomes more actualized. Considering these effect, the program/erase endurance would further decrease.

V. Conclusion

We have developed a program/erase endurance prediction model for NAND flash memory cell. We have implemented the anode hole generation model in the program/erase simulation conducted by device simulation with the practical circuit operation. It is revealed that the concentration of hole generation at the edges of the floating gate has an impact on the life-time of the tunneling oxide. The present simulation scheme makes it possible for the design rule dependence of the program/erase cycles to breakdown to be quantitatively estimated with the edge density on the memory chip in conjunction with the storage density.



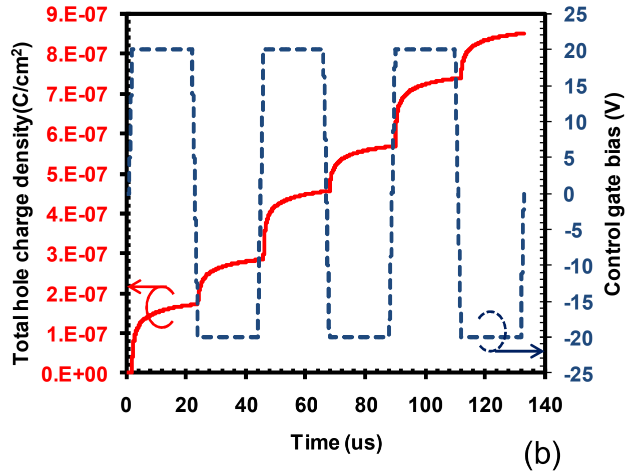


Figure 4. P/E simulation results using anode hole generation model (1D analitycal model) with L = 30nm. (a) Applied P/E pulse and hole generation efficiency. (b) Total hole charge through the tunnel oxide.

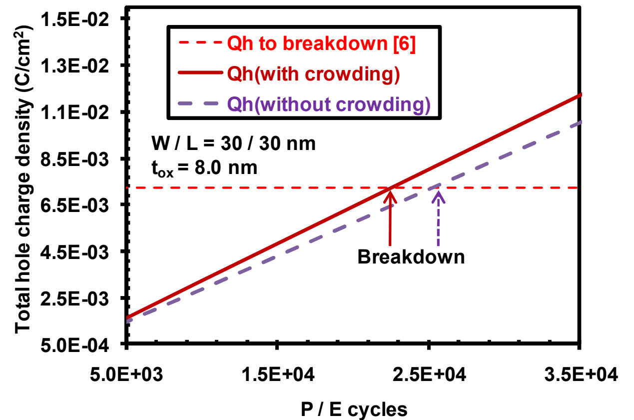


Figure 5. Total hole charge through the tunnel oxide for P/E endurance cycling with or without the tunnel current crowding effect on the gate edge. Qh to breakdown is calculated by the previous report [6].

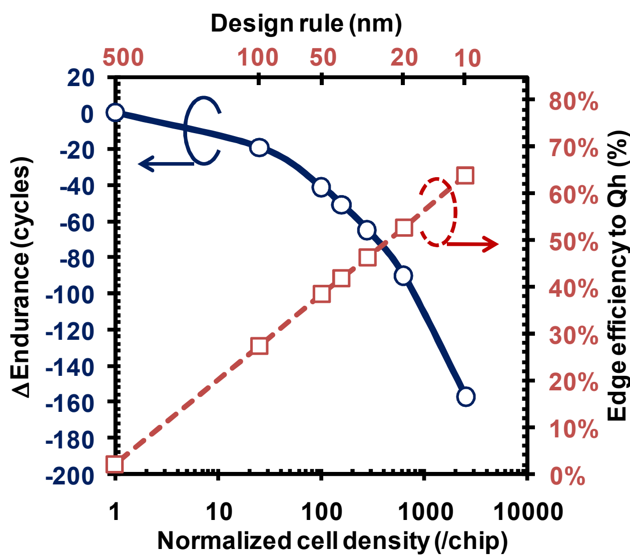


Figure 6. P/E endurance and gate edge efficiency to hole charge trend to design rule.ΔEndurance is the difference between the L = 500nm device and each device with a different sizes.

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