The Non-Equilibrium Green Function approach as a TCAD tool for future CMOS technology

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Abstract—**The potential of the Non-equilibrium Green function formalism as a new TCAD tool is demonstrated with concrete examples. We revise ballistic simulations of variability associated with discrete dopants and SiO_2/Si interface roughness of silicon gate-all-around nanowire transistors. Phonon limited mobility in various nanowire cross-sections are calculated from the current-voltage characteristics, showing an agreement with previous calculations using different models. Using the same electron-phonon parameters, statistical simulations combining discrete dopants and surface roughness are carried out for a nanowire transistor. The use of renormalized physics in the formalism is highlighted. The majority of results use a coupled-mode-space representation in concomitance with a recursive algorithm to deliver fast and accurate results, even with the inclusion of dissipative physics.**

NEGF; Silicon Nanowire transistors; Random discrete dopants; Surface roughness; Phonon scattering

I. INTRODUCTION

As announced by INTEL [1], FinFET devices integrated in CMOS ICs will soon be in production using less power that its planar counterpart while delivering the same, or faster, speed. This opens an era of transition from planar to 3D device architecture in CMOS technology. Future devices will be 3D and will be small, calling for a new more complicate set of designing rules. Accurate device simulation with predictive capability will be needed to guide future designs. Nanometre devices will be plagued by source-to-drain tunnelling, quantum capacitances, etc. The need for an intrinsic quantum device simulation tool is inevitable. Even if classical simulation tools with sophisticated quantum corrections are available, their predictability is limited by a continuous need for calibration. The Non-Equilibrium Green function formalism brings the possibility to incorporate all the quantum-mechanically-induced phenomena in an intrinsic way into TCAD tools, without the need of corrections. The NEGF is still a relatively new technique in device simulation but the efficient incorporation of dissipative physics has opened the possibility to evaluate the device performance in a more accurate way.

Silicon Gate-all-around Nanowire transistors (NWT's) in a wide range of cross-sections have been fabricated. Their outstanding electrostatic integrity has been demonstrated experimentally [2]. However, at small dimensions, the source/channel and drain/channel interfaces could contain less than 10 dopants. The fluctuation in number and configuration of dopants from device to device will affect the effective channel length for transistors under 10 nm, causing fluctuations in the off-current, subthreshold slope and threshold voltage. A larger effect comes from the "roughness" of the Si-SiO_2 interface [3]. The effect of the rough interface on the electron transport is twofold: firstly it induces an extra confinement for small channel cross-sections, and secondly it scatters the carriers, inducing partial reflection, diminishing the probability of transmission from source to drain. Phonon scattering is a source of incoherent scattering and dissipative transport. As the cross-section decreases the effective electron-phonon coupling increases, making the scattering more effective at small nanowire cross-sections. This is based on the fact that the coupling constant is inversely proportional to the cross-sectional area of the nanowire [4]. The rest of the paper is divided as follows; we start with a section in which the NEGF formalism is briefly explained, followed by a section covering the application of NEGF to variability in GAA nanowire transistors.

II. THE NEGF METHODOLOGY AND APPROXIMATIONS

A. NEGF Formalism

The NEGF method [5] was developed in the fifties to solve quantum non-equilibrium problems perturbatively. Today, with the increasing computer power available, this method can be applied to relatively large realistic structures, e.g. 25×25×100 nm. Small structures can even be simulated in a full-band context [6]. Recently [6, 7, 8] phonon scattering has been efficiently incorporated and applied to nanotransistors. The NEGF formalism is essentially embedded in the two following equations [5]

$$(g_0^{-1} - U)g = 1 + \sigma\, g \tag{1}$$

$$(g_0^{-1} - U)g^{<} = \sigma g^{<} + \sigma^{<} g_a \tag{2}$$

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where g_0 is the retarded Green's function for the one-body part of the Hamiltonian with the external field U turned off. σ is the retarded self-energy including the coupling to leads and other interactions (i.e. electron-phonon interactions). The g and g_a are the full retarded and advanced Green's functions, respectively. The first equation is equivalent to Schrödinger equation and the second is a quantum generalization of the semi-classical Boltzmann equation. The physics comes from the approximation made in writing the Hamiltonian g_0^{-1}, the self-energies and the boundary conditions. The Hamiltonian usually contains the renormalized kinetic energy and the Hartree potential. The self-energies have in general real and imaginary parts, the real part represents the renormalization of the electron energy and the imaginary represents the lifetime of the particular electron states, commonly called scattering. There are two types of self energies- the dynamic one σ and the statistical one $\sigma^{<,>}$.

B. The hamiltonian, coupled mode space and the phonon scattering self-energies

The Hamiltonian of NEGF is written in the effective mass approximation and the effective mass is extracted from tight-binding calculations [9] (m_l=1.07, m_t=0.3 in units of electron mass). Non-parabolicity can be introduced by making the effective mass energy dependent. The nanowires in this work are all oriented in the [100] direction. The electron-phonon scattering self-energies ignore the real part [7] and the imaginary is written in the self-consistent Born approximation [7] using local self-energies. The electron-phonon coupling parameters are from ref. [8]. The discrete random dopants are introduced as a charge in a volume 0.2x0.2x0.2 nm^3 [10, 11]. The surface roughness is described by a digitized change in dielectric function through SiO_2/Si interface [12]. The average SiO_2 thickness used in this work is 0.8 nm. The coupled mode space (CMS) method reduces the full 3D problem to the product-space of the longitudinal-space and the modes of the transversal space [13]. The dimension of this space is (n_l × N) where N is the number of modes, which is substantially smaller than the number of discretisation nodes in the transverse cross section (nt^2 × n_l). The effective mass Hamiltonian combined with the CMS method and the recursive algorithm [7] makes the NEGF tool almost as efficient as the semi-classical tools.

III. SIMULATIONS OF GAA SI NANOWIRE TRANSISTORS

In this section we will present various examples of NEGF nanowire transistor simulations, which illustrated different aspect already mention in the introduction. All the simulations presented in this work considered a gate all around silicon nanowire transistor.

A. Tunnelling

We will start with the impact of tunnelling for different channel lengths and nanowire cross sections [14]. The simulated Si NWTs have undoped channels, 0.8 nm SiO_2 oxide and 10 nm Source/Drain regions doped at 10^{20} cm^{-3}. Figs 1 and 2 show the off and on –currents as a function of the channel length for devices with 2.2x2.2 and 4.2x4.2 nm^2 cross-section respectively. The tunnelling current is large at the large cross section mostly as a result of small effective masses (ml= 0.98, mt=0.19) as compared with the confinement masses (ml=1.07, mt=0.3). The on- tunnelling current percentages at high drain are larger when compared with the corresponding low drain results. The subthreshold slope associated with the tunnelling current is larger than the corresponding thermionic one.

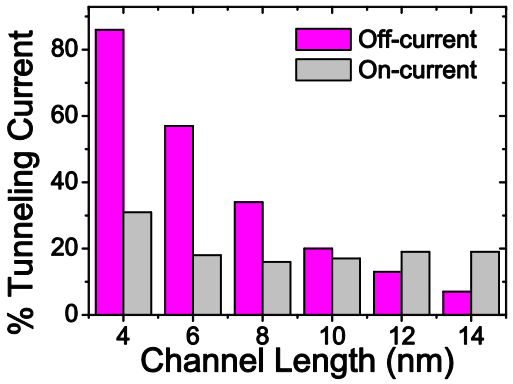

Figure 1. Tunnelling current (as percentage of total current) as a function of the channel length for the device with a cross-section of 2.2x2.2 nm^2. The drain bias is 0.05 V.

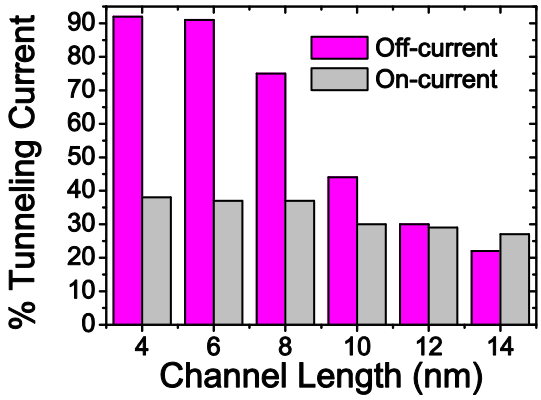

Figure 2. Tunnelling current (as percentage of total current) as a function of the channel length for the device with a cross-section of 4.2x4.2 nm^2. The drain bias is 0.05 V.

B. Random Dopants & Surface Roughness

In this section we study the impact of surface roughness and its combination with random discrete dopants on the current variability in nanometer scale nanowire MOSFETs [12]. The simulated transistors are 26 nm long, consisting of a 6 nm undoped channel and 10 nm S/D regions doped at $10^{20}cm^{-3}$. The cross-section of the device is 2.2×2.2 nm^2. Rough interface is considered in the channel and random discrete dopants are placed in two regions of 4 nm located between continuously doped S/D regions and the channel [12]. The surface-roughness-related resistance, estimated at V_G=0.55 V (Vd=1 mV) from the simulations including only random dopants, is R_{SR} =6.9067×10^3 Ω and the charge integrated

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through the cross-section in the middle of the channel is Q_{ave}=1.30×10^6 cm$^{-1,}$ which results in a surface-roughness-related mobility of 542 cm^2/Vs. The current-voltage characteristics of 30 microscopically different devices combining random surface roughness and random dopant configurations are shown in Fig. 3 for a drain bias of 1mV. When the effect of both sources of variability is considered the maximum spread in threshold voltage is 145 mV compared to the surface roughness case alone (100mV). The on-current fluctuations are also larger compared to the case with only surface roughness, with the lowest-current device producing an on-current, which is approximately 15% of that of the smooth device.

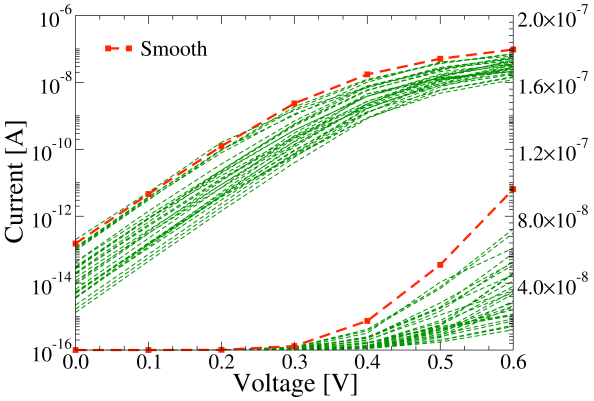

Figure 3. I_D-V_G characteristics of the nanowire transistor with *surface roughness* in the channel and *random dopants* in the source and drain.

The average on-current is reduced by 42% for the surface roughness case and by 63% for the combined case, relative to the smooth case. Considering the discrete dopants alone the on-current was reduced by 48% [11]. The contribution of the combined processes to the on-current is not a simple addition of both effects. The "average" threshold voltage shift is approximately 67 meV and is rather similar in both cases (surface roughness only and combined case), as it is mainly a result of the average over the same surface roughness type.

C. *Channel Length Dependence of Random Dopant variability*

In this section, the variability induced by discrete dopants has been compared for 2.2×2.2 nm^2 and 4.2×4.2 nm^2 cross-section nanowire transistors with two different channel lengths (6nm and 12nm) at low drain bias (1mV) [15]. The results are shown in fig. 4. The random dopant result in threshold voltage, sub-threshold slope and on-current variability. The columns in Figure 11 show the histograms corresponding to $V_T - \langle V_T \rangle$, $S - \langle S \rangle$, $(I_{on} - \langle I_{on} \rangle) / \langle I_{on} \rangle$ respectively, where $\langle V_T \rangle$, $\langle S \rangle$ and $\langle I_{on} \rangle$ are the ensemble averages of V_T, S, I_{on} respectively. The threshold voltage and the sub-threshold slope variability are both reduced with the increase in channel length due to better gate electrostatic control and less tunnelling. Both the threshold voltage and the sub-threshold variability are less in the 2.2×2.2 nm^2 transistor due to improved electrostatic integrity. In contrast, the on-current variability is much higher in the 2.2×2.2 nm^2 transistor compared to its 4.2×4.2 nm^2 counterpart due to the larger number of dopants and more self-averaging in the second case. The on-current variability, which is due to variability in the access resistance, is virtually channel length independent for the two-nanowire cross-sections.

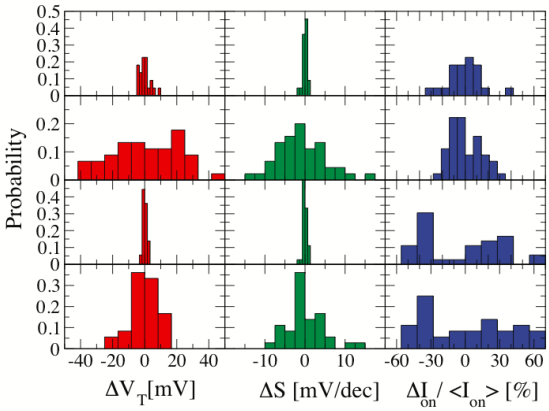

Figure 4. The two-first rows from the bottom to the top represent the 6nm and 12 nm channel length and 2.2x2.2 nm^2 cross-section devices. The two-second rows (from bottom to top) represent the 6nm and 12 nm 4.2x4.2 nm^2 devices.

D. *Phonon Scattering*

In this section the NEGF formalism is used to estimate the phonon limited mobility of a broad number of nanowire cross sections.

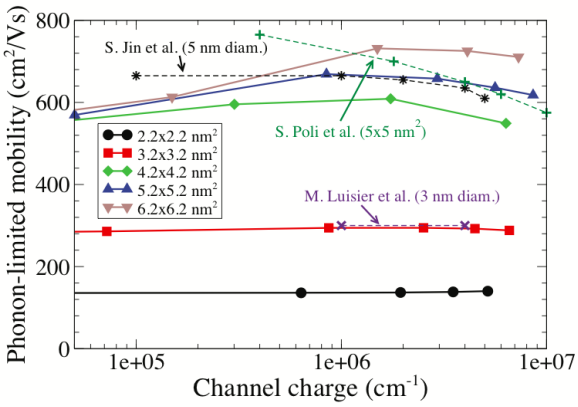

Figure 5. Phonon limited mobility for various nanowire cross-sections. The S. Jin, S. Poli and M. Luisier correspond to the results of refs. [8],[16] and [6] respectively.

This mobility is calculated by estimating the resistance of the channel (R_{ch}) for a given channel charge Q_{ch}. To obtain R_{ch} we estimate the source/drain resistances $R_{s/d}$ by doing a linear regression using the total resistance of the three long channel devices (20, 30 and 40 nm). Then, we can obtain the channel resistance for each transistor as $R_{ch} = R_{total} - R_{s/d}$. The phonon-limited mobility is calculated as $\mu_{pho} = L_{ch}/(R_{ch}Q_{ch})$ where L_{ch} is the effective channel length, which is in general different from

the gate length. Fig. 5 shows the phonon limited mobility as a function of Q_{ch} for various cross-sections. There is very good agreement with other publications [8, 6, 16].

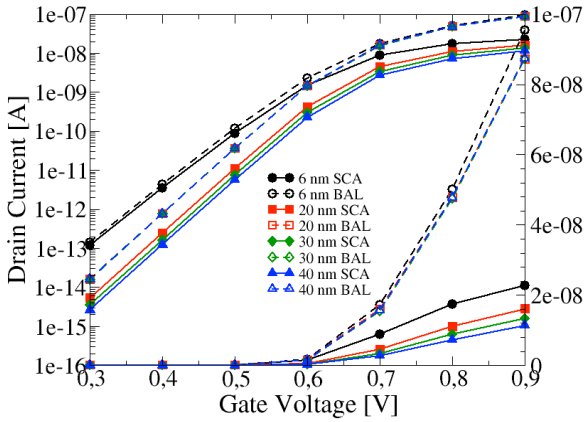

Figure 6. I_D-V_G characteristics of nanowire transistors of 2.2x2.2nm^2 cross-section with differing channel lengths. Dashed lines correspond to ballistic simulations and continuous lines to simulations including phonon scattering. The drain bias is set at 1mV.

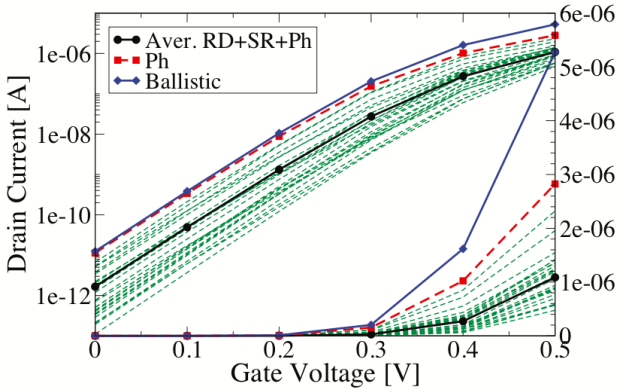

Figure 7. I_D-V_G characteristics of nanowire transistors with discrete random dopants (4nm) in S/D, surface roughness and phonon scattering. The Ballistic I_D-V_G is in Blue, the average I_D-V_G and the I_D-V_G with only phonon scattering are included. The device has 6 nm channel length, 10 nm S/D and 2.2x2.2 nm2 cross-section. The drain bias is V_D=0.6V.

Fig. 6 shows the I_D-V_G characteristics for the different gate length transistors and a 2.2x2.2 nm2 cross-section at 1 mV drain bias in the presence of phonon scattering in the whole device. The effect of scattering is negligible for the 6nm device at low gate bias but becomes significant at high bias. Furthermore, the on-current reduces 77% of its ballistic value due to scattering. From this 20% corresponds to the scattering in the source/drain region.

E. Variability including phonon scattering

In this section we have carried out statistical simulations at high drain bias (V_D=600 mV) for a 2.2x2.2nm2 transistor considering electron-phonon scattering, discrete random dopants and surface roughness [15]. Fig. 7 shows the I_D-V_G characteristic of 25 devices, which differ in the realisation of disorder. The I_D-V_G characteristics of the smooth ballistic device, the device with phonon scattering only and the average I_D-V_G characteristic of the 25 devices with disorder have also been calculated. The average threshold voltage shift is around 60 mV and is the result of the confinement induced by interface roughness. The sub-threshold slope fluctuates in the range 65-70 mV/dec. The change in sub-threshold slope is mainly associated with the discrete dopants. The on-current of the ballistic device is reduced 57% by phonon scattering. This strong reduction is partially due to: (i) scattering in the source/drain extension regions and (ii) the reduction of phonon limited mobility induced by the decrease in the device cross-section. It should be noted that the impact of the phonon scattering is of the same order as the other mechanism.

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