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Large-Signal Full-Band Monte Carlo Device Simulation of Millimeter-Wave Power GaN HEMTs with the Inclusion of Parasitic and Reliability Issues.

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***Abstract*—We report for the first time the simulation of the large-signal dynamic load-line of high-Q matched mm-wave power amplifiers obtained through a Monte Carlo particle-based device simulator. Due to the long transient time of large reactive circuit elements, the time-domain solution of power amplifier high-Q matching networks requires prohibitive simulation time for the already time-consuming Monte Carlo technique. However, by emulating the high-Q matching network and the load impedance through an active load-line, we show that, in combination with our fast Cellular Monte Carlo algorithm, particle-based accurate device simulations of the large signal operations of AlGaN/GaN HEMTS are possible in a time-effective manner. Reliability issues and parasitic elements (such as dislocations and contact resistance) are also taken into account by, respectively, exploiting the accurate carrier dynamics description of the Monte Carlo technique and self-consistently coupling a Finite Difference Time Domain network solver with our device simulator code.**

I. Introduction

The drive towards device scaling with increased output power levels in current millimeter-wave power amplifiers [1] results in a highly non-linear, out-of-equilibrium transport of high-energy carriers inside the devices. Particle-based Monte Carlo (MC) device simulators, in particular the ones based on full band electronic structure and phonon spectra rather than analytical models, allow an accurate description of this complex nanoscale carrier-dynamics.

Small-signal AC analysis fails to predict large-signal device performance, which must be assessed by simulating the device within the full range of actual operating conditions. In such cases, the load-line voltage swing and the matching network must be included. Moreover, the analysis of the dynamic load-line can provide valuable insight regarding the device large-signal operations [2] and the related inner carrier dynamics.

High-Q ($i.e.$ highly selective in frequency) matching networks are required to suppress undesired harmonics in popular RF power amplifier classes such -AB, -B, -F, and hard-driven Class-A. Solving these networks with time domain techniques requires long simulation time due to the long transient times related the network large reactive elements. So, time-consuming MC simulators are somewhat poorly suited for this kind of analysis. However, this issue can be overcome by using an active-load line technique where a sinusoidal voltage generator, tuned at the fundamental frequency, is connected to the device output [3].

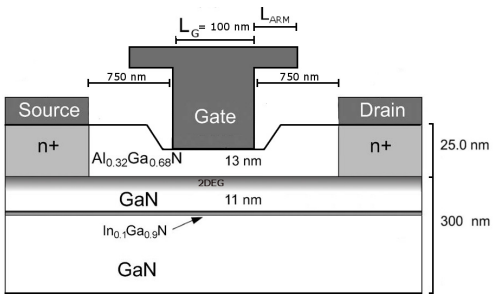

Fig. 1. Simulated $AlGaN/GaN$ HEMT device [4], [5]

In the present work, we simulated and analyzed the dynamic load-line under large-signal operations of the the GaN HEMT reported by Palacios *et al.* [4], previously modeled in a former work of our group [5], as shown in Fig. 1. The details about the used active load-line technique are described in Section II, and the inclusion of parasitic element under large-signal operations is discussed in Section III. Finally, the large-signal characterization, in terms of dynamic load-line and output waveforms of the chosen GaN HEMT is reported in Section IV, and conclusions are drawn in Section V.

II. Time-efficient Simulation of mm-wave Power Amplifiers Load-lines with high-Q Matching Networks

The active load-line technique can emulate the load-line voltage swing at the drain contact at the fundamental harmonic, and presents a short-circuit at the other harmonics, effectively emulating a high-Q matching network tuned at the fundamental frequency. The actual synthesized load

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impedance can be determined in post-processing:

$$Z_L(\omega_1) = |Z_L(\omega_1)|e^{j(\angle Z_L(\omega_1))} = \frac{v_D(\omega_1)}{i_D(\omega_1)} = \frac{|v_D(\omega_1)|}{|i_D(\omega_1)|}e^{j(\angle v_D(\omega_1) - \angle i_D(\omega_1))} \quad (1)$$

where $v_D(\omega_1)$ and $i_D(\omega_1)$ are the complex phasors of the drain current and voltage sinusoids at the fundamental frequency ω_1

Then, the magnitude and phase of the complex load can be adjusted by changing magnitude and phase of the voltage generator:

$$|v'_D|(\omega_1)| = |v_D(\omega_1)| \left(\frac{|Z_{Ltarget}(\omega_1)|}{|Z_L(\omega_1)|} \right) \quad (2)$$

$$\angle v'_D(\omega_1) = \angle v_D(\omega_1) + (\angle Z_{Ltarget}(\omega_1) - \angle Z_L(\omega_1)) \quad (3)$$

where $Z_{Ltarget}(\omega_1)$ is the desired load impedance at the fundamental frequency ω_1.

This active load-line technique, and the fact that our full band Cellular Monte Carlo (CMC) is up to 25 times faster than conventional MC simulators [6], allow us to perform efficient large-signal simulations of state-of-the art GaN HEMTs. The simulations of 160 ps ($i.e.$ four 25 GHz time periods) with 50000 simulated carriers, 2.5 fs Poisson solver time step, and 0.2 fs free-flight time step, required about 20 hours of actual computational time on a 64-bit Intel Xeon 3 GHz using 1.3 Gb of RAM to store the precomputed scattering look-up tables (required by the CMC approach).

III. Inclusion of Parasitic Elements under Large-Signal Operations

The analytical inclusion of parasitic elements based on small-signal analysis post-processing [7] is not feasible in the large-signal regime. Therefore, our full band CMC simulator was self-consistently coupled with a time-domain network solver. This solver uses the CMC device simulator current output at each Poisson solver time-step to solve, by using a Finite Difference Time Domain (FDTD) approach, the differential equations of the network and calculate the resulting network voltages that are then fed as input to the device simulator [8]. The small reactive parasitic elements can be time-efficiently simulated with this approach because their transient time response is much shorter than the one associated with high-Q matching network elements ($i.e.$ large reactive values).

In such way, we can simulate the difference between the voltage applied to the device "extrinsic" contacts and the voltage actually seen by the device at its "intrinsic" contacts. The advantage of this real-time time-domain solution, unlike the small-signal AC analytical approach, is that there are not assumptions regarding small-signal / large-signal regime, the linear / non-linear response of the device, and the number of harmonics involved.

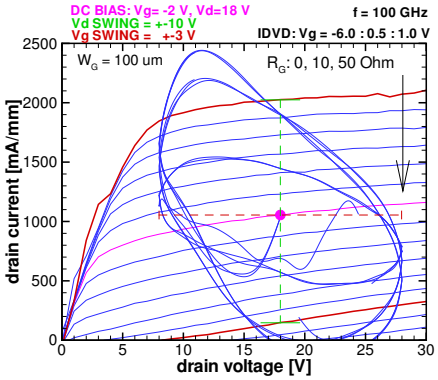

Fig. 2. Effect of the gate parasitic resistance, R_G, on the dynamic load-line at 100 GHz.

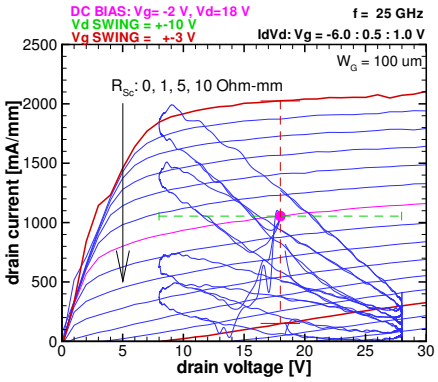

Fig. 3. Effect of the source contact resistance R_{Sc} at 25 GHz.

IV. Large-Signal Simulations of mm-wave GaN HEMT Power Amplifiers

The active load-line technique and the FDTD solver were combined, together with the CMC, in order to include in the device large-signal operations the output high-Q matching network / load impedance seen by the device at its output contacts (by using the active load-line) and relevant parasitic elements (by using the FDTD solver).

The effect of the parasitic gate resistance (R_G) on very high-frequency (100 GHz) large-signal operations, in a device biased in Class-A, is shown in Fig. 2. As we can see, the voltage drop associated to the gate resistance leads to a lower gate voltage swing, seen by the device at its intrinsic gate contact, resulting in a lower output drain current swing. There is no change in the DC quiescent point of the device because the gate displacement current has only an AC component (no gate leakage due to tunneling was simulated). In this case, we chose to preserve a constant drain voltage swing regardless the output drain current. This corresponds to a situation where the different devices see a different load-impedance ($i.e.$ the different slope of the dynamic load-line major axis corresponds to the different real-part of the load impedance seen by the device). On the other hand, this approach allows us to evaluate the operation of different devices within the same range of

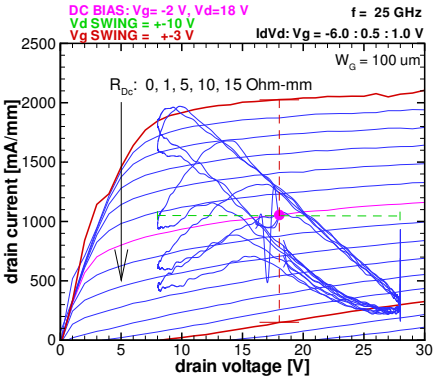

Fig. 4. Effect of the source contact resistance R_{Sc} at 25 GHz.

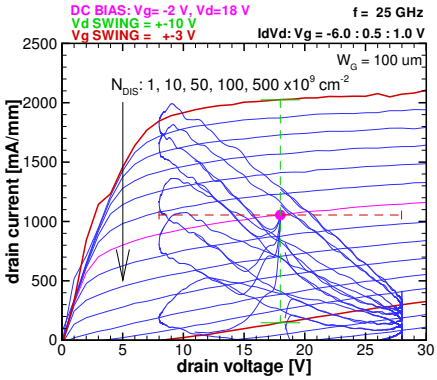

Fig. 6. Effect of threading-dislocation defects at 25 GHz.

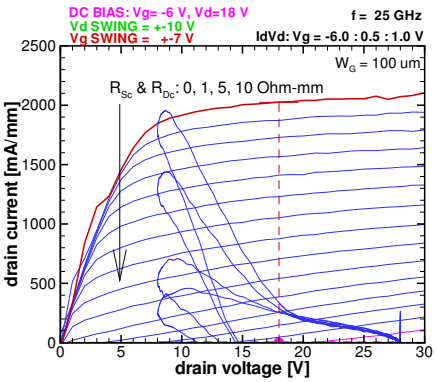

Fig. 5. Effect of source and drain contact resistance with the device biased for Class-B operations at 25 GHz.

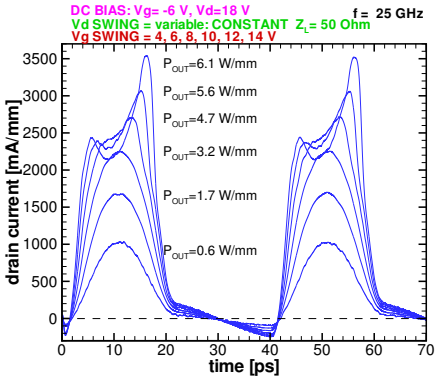

Fig. 7. Output current waveforms for increasing input power with the device biased for Class-B with high-Q output matching network at 25 GHz.

drain voltage swing.

Using a similar approach, the impact of the parasitic source (R_{Sc}) and drain (R_{Dc}) contact resistance, in terms of reduced drain current (due to R_{Sc}) and higher drain saturation voltage (due to R_{Ds}), is reported, respectively, in Fig. 3 and Fig. 4. As we can see, the effect of R_{Sc} is to shift the quiescent point by reducing the intrinsic v_{GS} seen by the device. This also results in a lower output current drain swing ($i.e.$ difference between the maximum and minimum current achieved by the dynamic load-line) due to the reduced device extrinsic transconductance. On the other hand, R_{Dc}, reduces the intrinsic v_D seen by the device causing a shift of the V_{Dsat} toward higher values. This results in the reduced drain voltage swing range where the device dynamic load-line is above the saturation voltage. As we can see, as we increase R_{Dc}, but keeping a constant drain voltage swing, the dynamic load-line is distorted due to the fact that the device is not always operating within the saturation region anymore. This reduces the output power as well as introduces the generation of spurious harmonics due to the large distortion. The combined effect of R_{Sc} and R_{Dc} on the load-line of a high-Q matched class-B amplifier can be seen in Fig. 5.

Reliability issues related to material defects such as dislocations can be included by exploiting the accurate nano-scale carrier dynamics description provide by the full band CMC approach. As we can see in the results shown in Fig. 6, the device behaves similarly to the R_{Sc} and R_{Dc} cases. This because the increased dislocation scattering reduces the carrier velocity in the device access regions, resulting in large source-gate and gate-drain access region series resistance. In this particular case, the effect of the source-gate access resistance is overwhelming with respect to the gate-drain one. The effect of the latter one can be only partially seen by the slight distortion introduced on the lowest dynamic load-line.

The distortion of Class-B output drain current waveforms, due to increasing input power, with constant load impedance of 50 Ω is shown in Fig. 7. In this case, we used a constant load impedance / variable drain voltage swing approach. For each input power level, the CMC simulations were repeated each time adjusting the drain voltage swing, due to the load-line, according to Eq. (2) and (3) until the desired load was achieved. In such way, we were able to perform a power sweep preserving a constant load impedance at the fundamental frequency ($i.e.$ increasing drain voltage swing with increasing drain output current, and constant IV phase relation). The dynamic load-lines of a constant load impedance input power sweep for a Class-A amplifiers are shown in Fig. 8, and the related large-signal typical figures of merit are shown in Fig. 9.

The active load-line can be also used to investigate the behavior of the large-signal output impedance of the device.

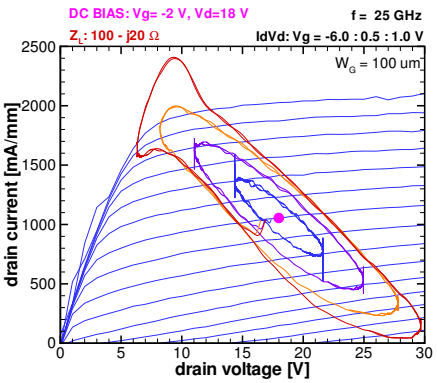

Fig. 8. Dynamic load-lines for increasing input power with the device biased for Class-A with high-Q output matching network at 25 GHz.

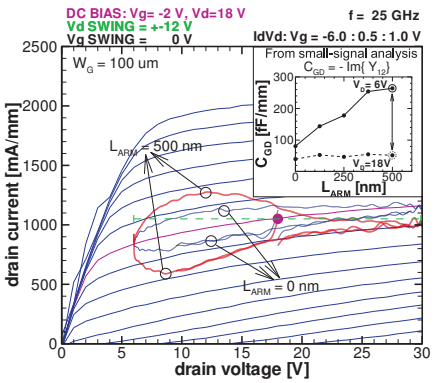

Fig. 10. Impact of the field plate length (L_{ARM}) on large-signal output impedance in a SiN passivated device at 25 GHz.

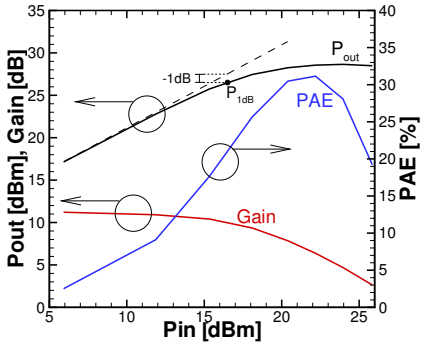

Fig. 9. Output power (P_{out}), Power Added Efficiency (PAE), and gain versus input power (P_{in}) for the power sweep shown in Fig. 8.

This is accomplished by applying a constant bias voltage at the gate without applying any RF input. The impact of the field plate length (L_{ARM}) on the large-signal output impedance (Z_{OUT}), due to the related drain-to-gate capacitance (C_{gd}), is shown in Fig. 10 in the Class-A biasing case. In this picture, the C_{gd} values obtained from small-signal analysis are also reported in the inset. As we can see, the difference between the C_{gd} values at low (6 V) and high (18 V) drain voltage without field plate ($i.e.$ $L_{ARM} = 0$) is small (41 fF/mm). On the other hand, there is a large difference (211 fF/mm) between the low and high voltage values of C_{gd} in the full-length field plate case ($i.e.$ $L_{ARM} = 500$ nm). This because the gate-drain depletion region inside the device is heavily dependent on the field plate length and the drain voltage. This results in a large variation of the output impedance, dominated by C_{gd} rather than C_{ds}, during the drain voltage swing with a full-length field plate as clear in the dynamic output impedance lines reported in the main figure.

V. Conclusion

In this paper, we reported for the first time the large-signal dynamic load-line of high-Q matched mm-wave power amplifiers obtained through a Monte Carlo particle-based device simulator. In particular, the combination of the active-load line technique, the fast CMC algorithm, the accuracy of the full band approach, and the parasitic element inclusion through a self-consistently coupled FDTD/CMC simulator allowed us to provide an accurate time-efficient characterization of high-power, high-frequency GaN HEMTs under large-signal operations. Lastly, we underline that the active load-line technique, combined with the drain voltage swing correction iterative procedure, represents the one-harmonic special case of a more general frequency domain network solver known as Harmonic Balance [9].

Acknowledgments

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