Statistical MOSFET Current Variation Due to Variation in Surface Roughness Scattering

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Abstract—**An efficient and accurate method to include surface roughness scattering from a general, realistic synthesized surface in 3D Monte Carlo simulation is presented with verification. The method is then applied to study drain current variation due to variation in surface roughness scattering in an 18nm bulk Silicon *n*MOSFET, highlighting substantially increased variation at low drain bias compared with electrostatic drift diffusion simulation.**

Keywords-variability; surface roughness; Monte Carlo

I. INTRODUCTION

Carrier propagation within the fluctuating potential landscape introduced by statistical sources of variability in 3D *'ab-initio'* Monte Carlo (MC) device simulation naturally includes the effects of transport variation in the estimation of statistical parameter variation [1]. These transport variations exist due to differences in position dependent carrier scattering between devices, owing to the fluctuating potential. They contribute additionally to the electrostatic modulation of carrier density in determining variability in device characteristics. Such statistical MC simulations, in contrast to efficient drift diffusion (DD) simulations, are motivated by the need for a predictive treatment of carrier transport variation that correlates with the source/channel injection velocity and the drain current in ultra small devices [2]. In this way, previously the impact of transport variation from random discrete dopants on drain current variation has been studied [3].

This work extends the analysis of transport variation by introducing a novel approach to surface roughness scattering, including its first application in assessing the impact of surface roughness scattering from random semiconductor/insulator interfaces on drain current variation. Such variation is expected to contribute to statistical device parameter variation where the channel length is comparable to the correlation length of the surface roughness features. The method is described in section II, including calibration of the surface parameters to replicate experimental universal mobility results. Section III details the simulation of drain current variability in an 18nm *n*MOSFET. Conclusions then follow.

II. SURFACE ROUGHNESS SCATTERING

A. Surface Scattering Model

Surface roughness scattering is here included solely via the deterministic propagation of carriers within the 3D fluctuating quantum potential landscape obtained from the density gradient solution in the presence of a realistic discrete rough semiconductor/insulator interface. No stochastic scattering process in the MC scattering rate table or boundary condition is considered. In this way, the particle dynamics recovers the position dependent scattering directly resultant from the surface features.

The surface is created randomly by Fourier synthesis using an exponential autocorrelation function characterized by the correlation length Λ and RMS amplitude Δ. Synthesis yields a continuous function with zero mean. Taking all positive values as a shift of the semiconductor from the nominal interface into the insulator and all negative values as a shift of the insulator into the semiconductor, application of the random surface pattern results in a digitization of the interface with amplitude dependent upon the mesh spacing at the nominal interface. Thus the digital steps at the interface are controlled through the choice of mesh. The correlation length Λ is a parameter of the synthesis and will be well represented within the simulation domain so long as the mesh spacing in the plane of the interface samples it sufficiently. A cross section of the digitized interface about the nominal interface is illustrated in Fig 1.

The effective quantum potential is obtained from the solution of the coupled Poisson and density gradient equations and its application to self-consistent MC simulation has been demonstrated previously [4,5]. The density gradient solution is characterized by three effective mass parameters b_x, b_y and b_z that respectively relate to the quantum confinement strengths in the x, y and z directions.

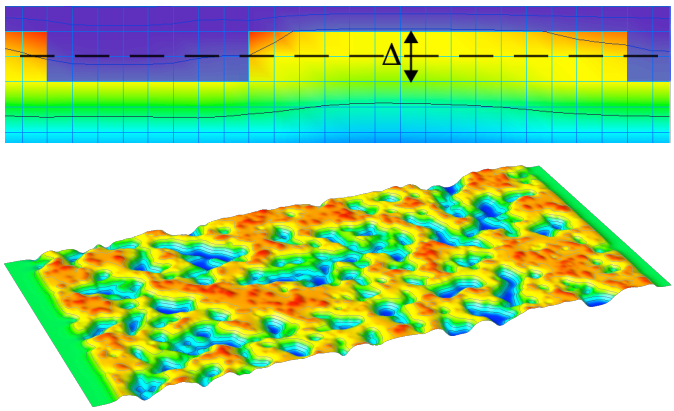

Figure 1. Cross section illustrating the digitised surface variation. The dashed line represents the nominal interface about which the surface varies with a step height Δ. The potential variation associated with a large surface is also shown.

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B. *Calibration*

In order to validate this model, MC simulation of inversion layer transport in a Silicon *n*-MOS capacitor was performed so as to recover the universal vertical field dependence of the surface mobility. A series of Silicon *n*MOS capacitors with substrate doping concentrations of $3.9\text{x}10^{15}$, $2.0\text{x}10^{16}$, $7.2\text{x}10^{16}$, $3.0\text{x}10^{17}$, $7.7\text{x}10^{17}$ and $2.4\text{x}10^{18}$ cm^{-3}, following experimental results by Takagi [6], were simulated over a range of gate biases. All have a surface measuring 50 x 100 nm^2 resolved with uniform 0.25nm mesh spacing in x and y directions. The inversion layer is similarly resolved with 0.25nm mesh spacing in the z direction. The typical surface potential associated with the simulation domain is also shown in Fig. 1. Adjusting the density gradient and surface parameters allows the effects of surface roughness to be adjusted and calibration of carrier mobility to experimental results to be performed. Changes to the surface amplitude Δ and density gradient effective mass parameters b_x and b_y alter the self-consistent surface potential and electron concentration solution. A larger effective mass in the plane of the surface results in a surface potential that shows more abrupt variation and therefore increased surface roughness scattering and reduced mobility. Similarly, increasing the height of the interface step results in greater variation in the surface potential associated with increased/decreased insulator thickness and therefore greater surface roughness scattering and reduced mobility. Calibration to experimental mobility is performed by modifying these parameters alone. b_z is assumed fixed as it is calibrated to give inversion layer carrier distributions in good agreement with Poisson-Schrödinger or non-equilibrium Green's function simulation that hold over a wide range of gate biases [7], while the mobility was found to be insensitive to the correlation length Λ for values close to experimentally observed values. Fixed values of Λ=1.5nm [8] and b_z=0.4 are used throughout.

Quantum corrected DD simulations of the described MOS structure are therefore performed over a range of gate biases and substrate doping, initially with surface amplitude Δ=0.3nm. This amplitude is approximately the inter-atomic layer spacing of the silicon lattice and is the amount by which the rough surface is observed to vary [8]. A range of values from 0.2nm - 0.3nm has however been reported in the past [9,10]. It should be expected that the simplified, discontinuous transition of the material dielectric, representing the interface within the discretised simulation domain, would ignore the chemical width at the interface [11]. It should therefore be no surprise if the mobility calibrated surface amplitude differs from experimental observation, though it should be expected to be close. Values of the density gradient effective mass parameters are initially b_x=b_y=0.6.

Frozen field MC simulation with '*ab initio*' surface roughness scattering is then performed using the DD effective quantum potential solution as previously described [1,3-,5]. The MC simulator employs an ellipsoidal non-parabolic band model with phonon mechanisms calibrated to bulk silicon. A small time-step of 0.01 fs is used throughout and is required in order to accurately propagate carriers within the rapidly varying quantum potential. Carrier mobility is estimated as the ratio of the ensemble average velocity to the applied field and is plotted against the effective field, calculated as the average electron weighted field in the z-direction. Ionized impurity scattering is modelled using the Brooks-Herring formalism, which does not well capture the low minority carrier mobility at low carrier concentrations, and consequent weak screening, present in the depletion regime. In this regime the mobility is limited by the bulk phonon mechanisms. Following discussions in [12], the acoustic deformation potential governing the strength of the bulk acoustic phonon interaction with carriers was increased in order to reduce the phonon limited mobility at weak confining fields. This was calibrated to agree with surface mobility calculations presented in [13].

This process was repeated, adjusting Δ, b_x and b_y, and the final calibration results plotted in Fig 2. The universal nature of the mobility degradation is immediately evident and, further, excellent agreement with experimental surface roughness limited mobility [6] is seen. II scattering is seen to limit mobility at lower effective fields in devices with high substrate doping and again matches well the experimental data. The final calibrated surface and density gradient mass parameters are given tin table 1.

TABLE I. CALIBRATED SURFACE PARAMETERS

Amplitude Δ [nm]	*Correlation length Λ [nm]*	b_x	b_y	b_z
0.5	1.5	0.8	0.8	0.4

III. SURFACE ROUGHNESS VARIATION

Having calibrated the surface scattering model, it was then applied to a well-scaled 18nm *n*MOSFET [14]. An ensemble of 100 devices, each with a random rough interface pattern, was generated and simulated at a high gate bias of V_G=1.00V for both low and high drain biases of V_D=0.05V and V_D=1.00V respectively. The interface was resolved with the same 0.25nm mesh spacing as used during surface scattering calibration. Following quantum corrected DD simulation, self-consistent quantum corrected MC was used to accurately simulate carrier transport. Fig.3 shows the 3D potential profile, highlighting the surface variation, in a typical device from the ensemble after self-consistent quantum corrected MC simulation.

Figures 4 & 5 show the scatter plot of the drain current variation from quantum corrected MC against DD simulation at

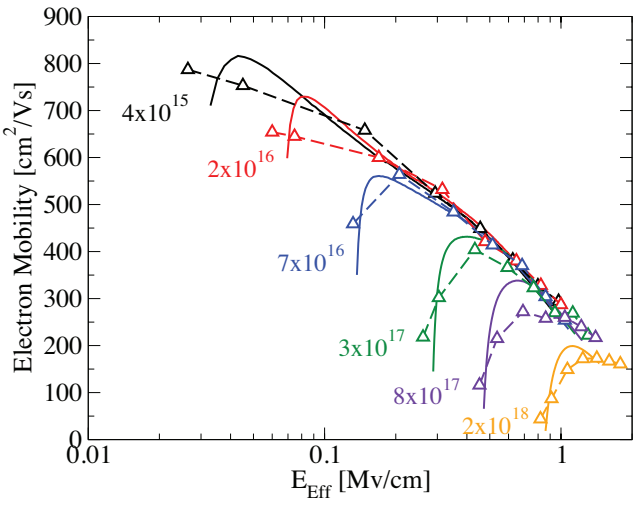

Figure 2. Calibrated surface mobility (symbols) compared with experimental data [6] over a range of substrate doping concentrations

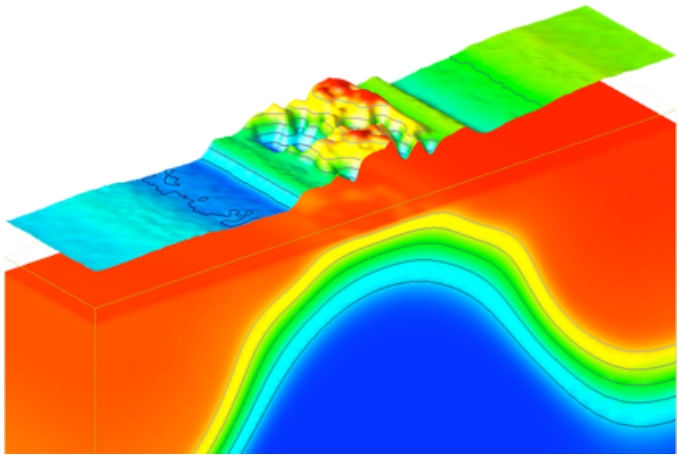

Figure 5. Potential profile of typical 18nm device with rough surface. The potential at the nominal interface is shown as a contoured slice and coloured separately.

low and high drain bias respectively. The dashed line is the curve y=x for reference. The standard deviations of the distributions are given in each case.

At low drain bias it is seen that the MC result show significantly greater variation, a 166% increase, compared with DD. The error in the drain current from MC has, after estimating the correlation length of the current signal, been estimated at around 2%. Considering this, the increased variation and low correlation is due to additional transport variation within the MC. Conversely, the results at high drain bias show strong correlation with the DD results and little difference in the standard deviation. This suggests surface roughness scattering is less important in this regime. These results are consistent with the increased scattering of lower energy carriers within the channel at lower drain biases and with quasi-ballistic transport at high drain biases.

Figures 6 & 7 show the MC simulated electron concentration within the channel at the nominal interface for devices with the lowest and highest drain currents respectively, at both low and high drain bias. The difference in the area of reduced oxide thickness between the two devices, which directly effects the total carrier concentration via the electrostatic increase in carrier concentration, especially at low drain bias, visibly correlates with the drain current – the greater the total area of reduced oxide, the greater the average carrier concentration and hence current. At high drain, current continuity combined with high carrier velocity limits the effect towards the drain. To quantify this, a statistical window spanning the width of the channel and positioned at its start is considered. The length of the window is allowed to increase until it spans the channel from source to drain. At each length, and for all devices in the ensemble, the area of reduced oxide within the window is determined. Fig. 8 shows the correlation of the incremental area with drain current for both DD and MC at both low and high drain bias. DD results are seen to be strongly correlated with the total area of reduced oxide thickness (that is $\Delta L/L_G$=100%) at both low and high drain bias, highlighting the electrostatic mechanism of variation due to the corresponding increase in carrier concentration over the entire device. MC shows similar dependence at high drain bias, as expected due to the strong correlation with DD as seen in

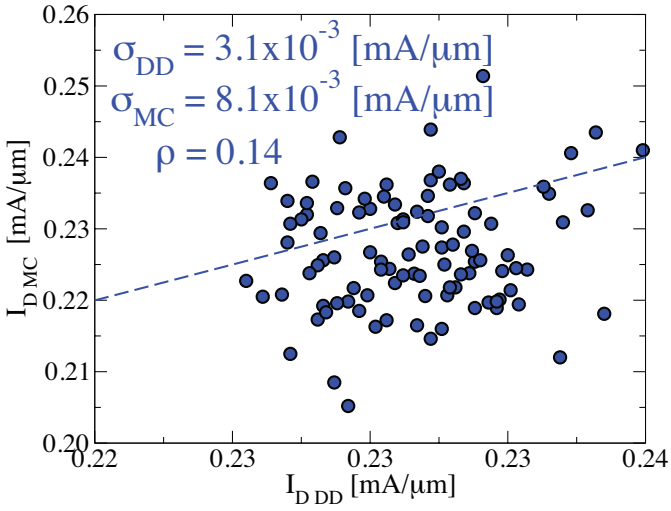

Figure 3. Scatter plot of drain current variation from DD vs. MC at V_D=0.05V. Results are largely uncorrelated owing to additional scattering at low energy.

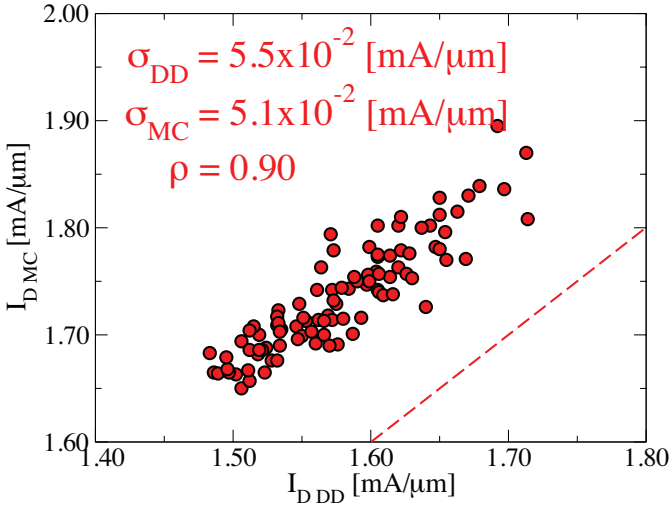

Figure 4. Scatter plot of drain current variation from DD vs. MC at VD=1.00V. Results are strongly correlated as scattering is here mitigated at high energy.

Fig. 5, but shows a rapidly decreasing correlation at low drain bias. This implies variation at the source ($\Delta L/L_G$=0%) plays the dominant role in MC simulations. The correlation due to electrostatic variation at the source is nearly half that of the correlation over the entire channel at high drain bias, suggesting that scattering form the interface pattern variation is responsible for additional current variation. Inset in Fig. 8 is the scatter plot of I_D results for low drain bias against high drain bias for both DD and MC simulation. The correlation seen in DD results emphasizes that the variation in drain current due to the electrostatic impact of the random surface at low drain is a good predictor of the result at high drain. The same is not true of MC results due to the dependence upon drain bias of the transport variation.

IV. Conclusions

We have described an efficient and direct method for the description of surface roughness scattering from realistic

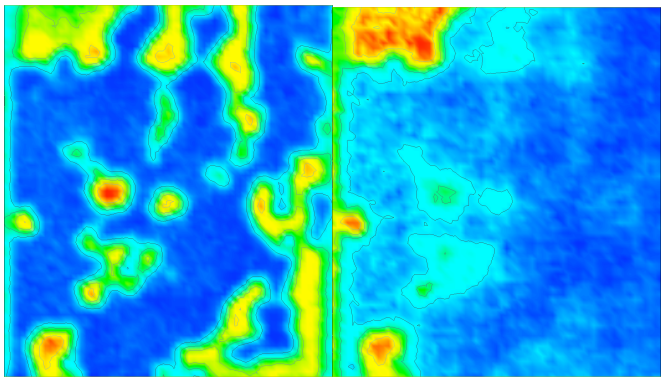

Figure 6. Electron concentration at the nominal interface for (left) Vd=0.05V and (right) Vd=1.00V in device with lowest I_D resulting from the surface pattern.

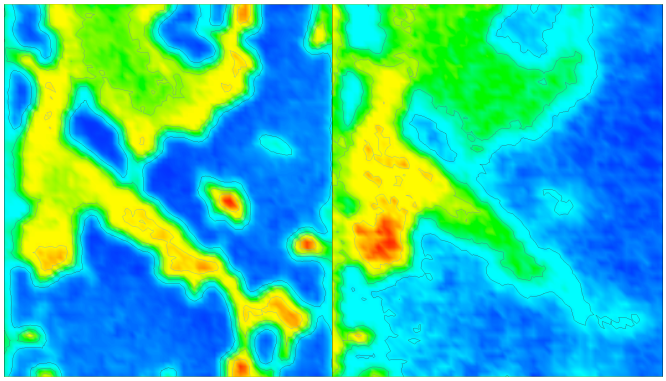

Figure 7. Electron concentration at the nominal interface for (left) Vd=0.05V and (right) Vd=1.00V in device with highest ID resulting from the surface pattern.

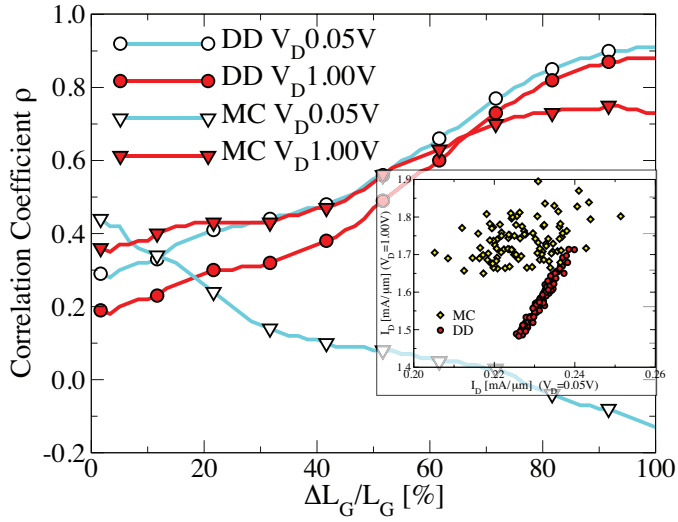

Figure 8. Correlation of I_D with ratio of area of reduced oxide to channel area in an increasing statistical window of length ΔL_G.

interfaces in MC simulation. After calibration of the surface RMS height and density gradient effective masses in the plane of the surface the model was shown to reproduce the universal nature of surface mobility dependence on vertical field in excellent agreement with experimental mobility in the surface roughness limited regime at high effective vertical field. Empirical fitting of the acoustic deformation potential to match the surface phonon limited mobility at low effective field and substrate doping resulted in excellent agreement with experimental results over a wide range of doping and bias conditions. The surface model was then applied to an ensemble of realistic 18nm nMOSFETs with random semiconductor/insulator interface patterns. At low drain bias, the variation due to surface roughness scattering in MC simulation was seen to be in excess of the variation due to the electrostatic modulation of carrier density seen alone in DD simulation, while at high drain bias the surface scattering played little role. Correlation of surface variation with current suggests that scattering from surface variation near the source is the dominant mechanism leading to increased variation at low drain bias, while at high drain bias quasi-ballistic transport limits transport variation.

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