Critical Analysis of 14nm Device Options

P. Oldiges[1], R. Muralidhar[1], P. Kulkarni[2], C-H. Lin[3], K. Xiu[1], D. Guo[4], M. Bajaj[5], N. Sathaye[5]
IBM Corporation, Semiconductor Research and Development Center
[1]Systems and Technology Group, Hopewell Junction, NY, USA; [2,3,4]IBM Research, [2]Albany, NY, USA,
[3]Yorktown Heights, NY, USA, [4]Hopewell Junction, NY, USA; [5]Systems and Technology Group, Bangalore, KA IN.
[1]poldiges@us.ibm.com

***Abstract*—Modeling challenges and solutions for silicon based high performance device options at the 14nm node are presented. A variety of devices are being considered, using a variety of methods to analyze the devices objectively. Partially depleted silicon on insulator (PDSOI) devices are compared against extremely thin (ETSOI) and FinFET devices.**

Keywords-14nm technology; PDSOI; ETSOI; FinFET; TCAD; performance modeling.

I. INTRODUCTION

In order to be able to continue scaling of gate length and pitch at the 14 nm technology node, further device innovation will be required. In addition to the usual knobs that technologists use to extend device scaling and performance, such as reducing gate dielectric thickness and source/drain/extension junction depth, more radical changes are being considered in the device structure. Instead of building conventional planar bulk or partially depleted Silicon on Insulator (PDSOI) devices, fully depleted devices are now serious contenders. Even at the 22 nm node, Intel has announced a production-ready fully depleted non-planar device [1]. In this work, we present some of the key challenges for modeling 14nm devices, and show a variety of methods that we have used to overcome these challenges to understand the issues related to PDSOI, ETSOI, and FinFET designs.

II. DEVICE STRUCTURE SPECIFICS

The three basic device options that we consider are shown in Figure 1 [2]. A common set of process and device physics parameters was used, which were based on calibrations to 32 nm node SOI data. A subset of parameters was adjusted according to the various process assumptions for the devices and relevant hardware data that were available. Unless otherwise stated, all process and device simulations were done using TSuprem4 [3] and Fielday [4,5]. PDSOI and bulk device gate length scalability and electrostatic integrity are a strong function of the body doping. ETSOI and FinFET devices show much improved short channel characteristics due to charge in the channel being geometrically confined in the Si body.

PDSOI: Salient aspects of the incumbent PDSOI 14 nm device include: 1) scaling down of the SOI thickness from 90 nm at the 32 nm node to ~65 nm at the 14 nm node with a S/D cavity etch that leaves about enough Si for epitaxial growth of in-situ doped SiGe or SiC, 2) reduction of spacer thicknesses to attain a gate to silicide distance of about 14 nm, 3) maintaining the same compositions for eSiGe and eSiC as in 22 nm technology and junction depth reduction from the 22 nm node. The gate workfunction (WF) for NFET and PFET were varied to understand the impact of WF on device performance.

ETSOI: Devices with gate lengths ranging from 12 nm through 38 nm with constant contact length, 30 nm raised source-drain and 5 nm SOI body thickness were simulated. The dopant profiles showed reasonably well overlapped devices with ~10^{19} cm^{-3} active concentration at the gate-edge. For nFET devices, a contact resisitivity of 2.7 Ω-μm^2 was extracted from the model-to-hardware fit. However, for 14 nm devices, a contact resisitivity of 1 Ω-μm^2 was assumed for both n-FET and p-FET devices. ETSOI devices show higher Cov over the PDSOI due to the raised SD design; higher C_{of} component.

FinFET: 2D/3D FinFET TCAD decks were utilized for performance prediction at the 14 nm node for both high-performance logic and SRAM. Several key parametric components, such as parasitic contact resistance, parasitic capacitance and extension junction gradient, were evaluated using 3D process/device simulator for scaling from 32 nm to 14 nm node dimension. FinFET has better electrostatic control compared to planar bulk devices. However, due to the inherent 3-dimensional device architecture, additional optimization considering the parasitic resistance and capacitance penalty are required for optimal device performance at the 14 nm node.

III. COMPARISONS

A common set of groundrules and device targets were the basis of a TCAD based comparison study of PDSOI, ETSOI and FinFET. The key target parameters are shown in table I below. In the initial phase of study, no HK related mobility degradation was assumed as the exact nature of its impact is still undergoing characterization. A common specific contact resistivity of 1 Ω-μm^2 was assumed to correctly capture the

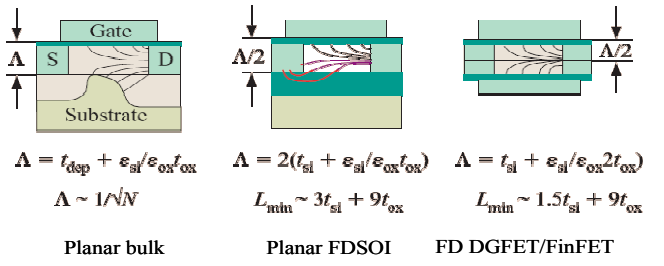

Figure 1. Electrostatic integrity of various device options (from [2]). Planar bulk and PDSOI devices are strongly dependent upon the body doping. Planar FDSOI devices (ETSOI) and double gate (FinFET) devices are more easily scaled

978-1-61284-418-3/11/$26.00 © 2011 IEEE

impact of contact length scaling. In this initial comparison study, the impact of CA resistance due to pitch scaling was neglected. The Mujtaba mobility model [6] was used to capture the effects of surface, Coulomb and phonon scattering. Process and device calibrations were performed against relevant hardware. Conventional stressor elements are used for the PDSOI devices, but no stressors are used for the fully depleted options.

TABLE I. 14NM DEVICE TARGETS

PCP (nm)	Target L (nm)	Tinv (nm) N/P	Ioff (nA/μm) N/P
60-80	18	0.85/1.0	43/51

In addition to the DC device characteristics, inverter delay is calculated to understand how the various device architectures affect. A 7-stage inverter chain with a fan-out of 3, as shown in figure 2, is simulated. The delay of the inverter is determined by averaging the rising and falling edge delays. Effective capacitance (Ceff) is then extracted and compared.

Table II summarizes the key device parameters extracted from the simulations for a power supply voltage of 0.9V. All results are for an 18 nm physical gate length device with an off current set to the prescribed targets from table I.

As expected, the elecrostatics are seen to be much better for the ETSOI and FinFET devices. DIBL and Vtsat are much smaller than for PDSOI, even with a larger Cov. Drive current (Ieff) is also larger for the thin body devices due to lower Vtsat and Vtlin. Additionally, the undoped body yields a potential mobility advantage over PDSOI, since the well and halo implants necessary to control SCE in PDSOI also cause a mobility degrade due to increased coulomb scattering. PDSOI however, has the upper hand in being able to define multiple Vt devices through the simple adjustment of halo/well dose.

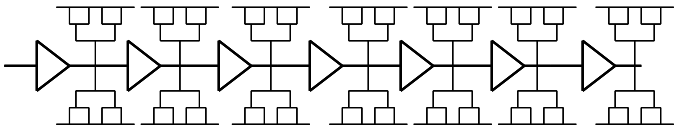

Figure 2. 7-Stage inverter chain used to calculate delay and Ceff of the various device options.

IV. PERFORMANCE ENHANCEMENT

In addition to the conventional knobs that we use to enhance device/circuit performance such as reducing gate dielectric thickness, we also investigated the impact of junction depth and extension/gate overlap on device performance. PDSOI and bulk devices are impacted by a reduction in source/drain or extension junction depth, so we focus our attention on reducing the extension junction depth. Figure 3 shows some results of reducing extension depth on PDSOI short channel effect. Idealized PDSOI structures with analytic doping profiles were created. The depth of the extension was varied, keeping the off current and overlap capacitance fixed. The result is improved DIBL while the subthreshold slope is unaffected.

TABLE II. NFET/PFET DEVICE PARAMETRICS FROM SIMULATIONS

	PDSOI N/P	ETSOI N/P	FinFet N/P
Vtsat (mV)	269/-262	238/-165	210/-134
DIBL (mV)	140/148	81.9/111	57/34
Ieff (μA/μm)	502/398	613/455	716/569
SSsat (mV/dec.)	99.4/139.3	82.3/78.6	74.1/70.3
Ion (μA/μm)	976/848	1120/887	1274/942
Rext (Ω-μm)	277/314	243/236	174/266
Cov (fF/μm)	0.268/0.278	0.32/0.31	
Ceff (fF/μm)	3.43	3.63	3.54

Figure 4 shows the impact of increasing underlap on device characteristics for a PDSOI device. An increase in device underlap increases the effective gate length, so the DIBL and subthreshold slope are seen to improve. The tradeoff of increased effective gate length is that the link-up resistance between the source/drain/extension and channel also increases with underlap. The effective current, Ieff, is a good measure of the switching speed of a device [7]. Figure 4b shows that Ieff reaches a maximum value for an underlap of ~2 nm for the device studied. The drop-off in Ieff at larger underlap is due to an increase in external resistance. ETSOI and FinFET devices also show similar improvements and trends in DIBL and Ieff with increasing underlap.

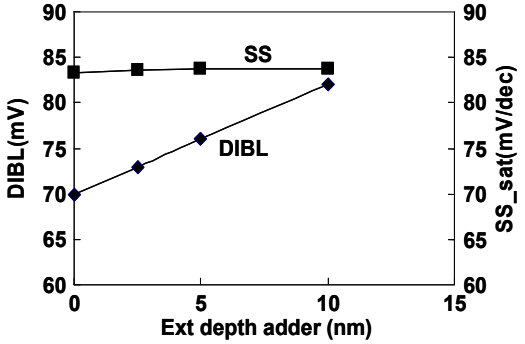

Figure 3. Impact of extension depth on PDSOI/Bulk device short channel effect. DIBL can be improved with shallow extensions.

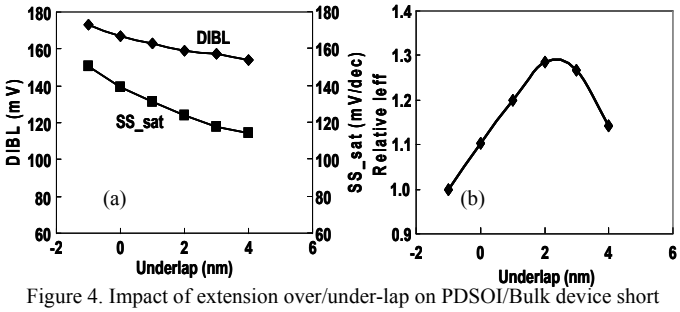

Figure 4. Impact of extension over/under-lap on PDSOI/Bulk device short channel effect and device characteristics. (a) Both DIBL and subthreshold slope are improved with uncreasing underlap. (b) Ieff increases with underlap until the extension resistance negatively impacts the current drive.

V. VARIABILITY

Device variability is an important consideration when developing a technology [8]. Although it is possible to run brute-force simulations to deeply analyze devices, simple "spreadsheet" analyses can provide a quick look into device

variability. In this section, we show the development of simple variability models to estimate the effects of Vt variations due to gate line edge roughness (LER), random dopant fluctuations (RDF) and metal gate WF fluctuation (GWFF) due to grain orientation. For FinFET's we also describe a model for σ_{Vt}variation due to Fin width variation [9].

The RDF model used is a standard published formula (1), such as found in [10], but in this work, we verify that the formula is valid via Monte Carlo modeling of simple prototype 22 nm node gate length devices. 500 randomly doped structures evaluated for W = 250 nm, W = 500 nm, and W = 1000 nm. Poisson statistics were assumed for fluctuations in number of dopants. As shown in Figure 5, equation (1) is an excellent fit to the simulations.

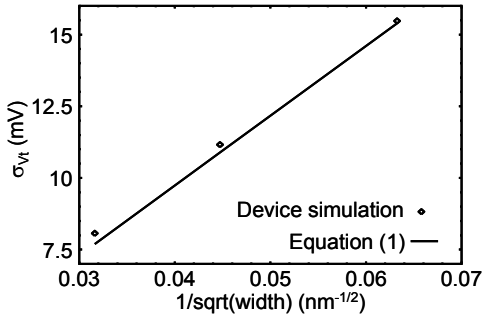

Figure 5. Comparison of equation (1) with device simulations of Vt variation due to random dopant fluctuations.

$$\sigma_{V_t} = \frac{qt_{inv}}{\varepsilon_{ox}} \sqrt{\frac{1}{WL} \int_0^{yo} \left(1 - \frac{y}{yo}\right)^2 N(y) dy} \tag{1}$$

The model that was developed for Vt fluctuations due to LER is based on a previously published concept of adding up 2D device "slices" [11], but the edge roughness itself is modeled using the measured spatial frequency spectrum of patterned gates. This spatial frequency is then fed in to a Monte Carlo code and the Vt of various gate width devices is determined. Knowing the spatial frequency spectrum of the edge roughness, a simple sum of squares formula, as shown in Equation (2) can be used to determine σ_{Lg}. Knowing σ_{Lg}, σ_{Vt} is seen to have a linear relationship with σ_{Lg}, with the proportionality constant being the slope of the Vt rolloff characteristics. Figure 6 shows the results of the simulations and analysis.

$$\sigma_{Lg} = \sqrt{\sum_{i=1}^{N} \left[\frac{A_i * \sin(W * f_i)}{\sqrt{2} * W * f_i} \right]^2} \tag{2}$$

For Vt variations due to GWFF, we define 3D devices with a gate that is divided into regions with different WF. For some given metal "grain" size, Monte Carlo techniques are used to set the WF of the grains according to the expected WF [12]. A large statistically significant number of Id-Vg characteristics were modeled for each of the configurations and Vt was extracted. For various device widths and grain sizes, we have found that the Vt variation can be reasonably well approximated by the equation (3). This formula was asserted

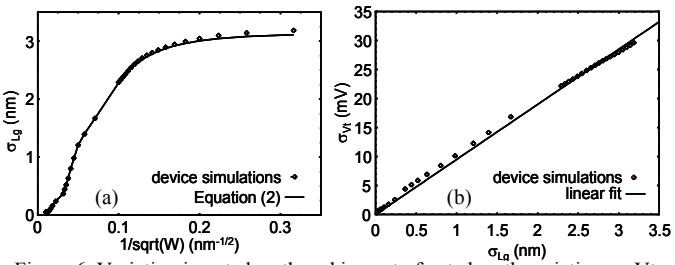

Figure 6. Variation in gate length and impact of gate length variation on Vt variation. (a) For LER that can be described by a dispersion relationship, the gate length variation is seen to be approximately linear for wide devices (W >~100 nm). (b) σ_{Vt} is seen to be proportional to σ_{Lg}, with the proportionality constant being the slope of the Vt rolloff characteristics.

in [13], but this assertion was based on a simple summing up of the WF and grain size of the gate itself. In this work, we define grain size and WF, run the 3D device simulations, and extract the Vt from the Id-Vg characteristics. Because we do the full device simulation, we are able to quantify the differences between this simple σ_{Vt} shown in (3) and the actual σ_{Vt} distribution.

$$\sigma_{Vt} = \frac{\sigma_{WF}}{\sqrt{N_{grain}}} \tag{3}$$

For FinFETs, the Vt variation due to fin thickness variations was recently published [9]. The basic equation describing the Vt variation is shown in equation (4).

$$\sigma_{Vt} = \frac{\sigma_{Vt(Nfin=1)}}{\sqrt{N_{fin}}} \tag{4}$$

Finally, we use these models to compare our device options. Figure 7 shows the individual σ_{Vt} variations as well as the total. The above equations (1)-(3) were used to obtain our estimates. We can see that the random dopant fluctuations will have a quite severe impact on PDSOI and bulk (halo) devices. We also see clearly that the excellent electrostatics of ETSOI and FinFET devices will reduce the impact of LER induced Vt variations.

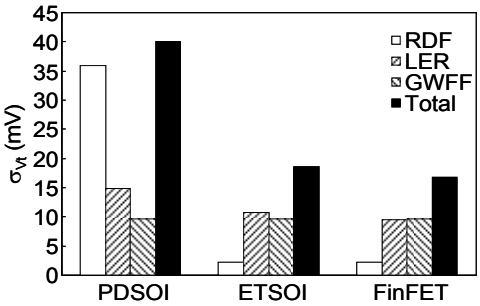

Figure 7. Comparison of Vt variability for various 14nm device options.

VI. Device Physics

It is of utmost importance to have confidence in the device and process models that are implemented in the simulation tools. But we must also take a pragmatic approach to modeling, making sure that any new physics that is

incorporated into the tools will not have a negative impact on simulation turnaround time.

One of the areas that we have focused on is MOS mobility models. A stress enhanced mobility model has been implemented in Fielday, which is based on the work in [14]. Careful validation of this model against hardware was done to give us confidence in our results. While stress is used to improve device performance, the use of high-k gate dielectrics has been seen to cause mobility degrade. Figure 8 shows the impact of SiO_2 interface layer thickness on electron mobility [15]. We have developed and implemented a simple remote phonon scattering model, based on the theory in [16], that allows us to model the impact of high-k thickness and interface layer thickness.

Quantum mechanical effects in devices continue to be important. We use QDAME [17, 18] to validate and tweak

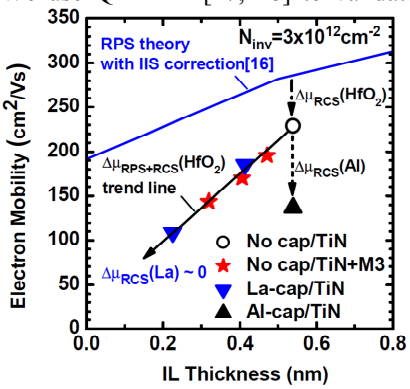

Figure 8. Mobility degradation due to HK gate dielectric (from [15]).

parameters used in our quantum correction models for thin semiconductor layers and confinement in various crystallographic orientations. QDAME is also used to help us gain understanding of intraband tunneling models, and tunneling at metal/semiconductor contacts, as well as metal/metal interfaces.

High field transport is no longer seen only when the MOS device is biased at Vds = Vdd. Doping levels and gradients are so high, that even in linear operation, carriers see high electric fields. Damocles [19] allows us to probe the high field carrier transport regime and validate our simple device models. Typical use of Damocles is to understand the best methods to approximate the effect of velocity overshoot within the confines of the drift-diffusion model. We also utilize Damocles to help us understand transport at heterojunction barriers.

VII. Conclusions

The three leading device architectures for the 14 nm node were analyzed. We showed that evolutionary scaling of bulk/PDSOI is possible down to the 14 nm node. Fully depleted designs, however, show much better short channel effect, and therefore better scalability. An analysis of variability indicates that fully depleted devices are expected to be significantly less sensitive to random doping fluctuations, and overall should show less variability than PDSOI or bulk designs. Finally, we presented several models and methods that we found to have an important impact in validating our confidence in our modeling tools.

Acknowledgment

The authors are grateful for modeling support and feedback from S. Furkay, J. Johnson, and R. Robison. This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

References

[1] D. Scansen, “Intel putting fins on at 22 nm”, EETimes, http://www.eetimes.com/electronics-blogs/dew-point/4215728/Intel-putting-fins-on-at-22-nm , May 4, 2011.

[2] W. Haensch, *et al.*, ”Silicon CMOS devices beyond scaling”, IBM J. Res. Dev., vol. 50, p. 339, 2006.

[3] Synopsys “Taurus-TSUPREM-4” advanced 1D and 2D process simulator,http://www.synopsys.com/Tools/TCAD/ProcessSimulation/Pages/TaurusTSupreme4.aspx .

[4] E. Buturla, *et al.*, ”A new three-dimensional device simulation formulation,” NASECODE VI Proc., pp. 291-296, 1989.

[5] M. Ieong, *et al.*, ”Efficient quantum correction model for multi-dimensional CMOS simulations,” Proc. SISPAD, pp. 129-132, 1998.

[6] S.A. Mujtaba, *et al.*, "An accurate NMOS mobility model for 0.25mm MOSFETs," in Proc. 6th Intl. Conf. Simul. Sem. Dev. Process. (SISDEP), pp. 424-427, 1995.M.H. Na, *et al.*, “The effective drive current in CMOS inverters”, IEDM Tech. Dig., paper 5.4.1, pp. 121-124, Dec. 2002.

[7] M.H. Na, *et al.*, “The effective drive current in CMOS inverters”, IEDM Tech. Dig., paper 5.4.1, pp. 121-124, Dec. 2002.

[8] N. M. Idris, *et al.*, “Comprehensive simulation study of statistical variability in 32nm SOI MOSFET”, 7th Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits (EUROSOI), 17-19 January, Granada, Spain, 2011.

[9] C-H. Lin *et al.*, "Modeling of width-quantization-induced variation in logic FinFETs for 22nm and beyond", VLSI Symp. on Tech. Dig., paper 2A-3, June 2011.

[10] "Fundamentals of Modern VLSI Devices", Yuan Taur and Tak H. Ning, 2nd edition, p. 241.

[11] P. Oldiges, *et al.*, "Modeling line edge roughness effects in sub 100 nanometer gate length devices", proc. SISPAD, pp. 131-134, Sept. 2000.

[12] H. Dadgour, *et al.*, “Modeling and analysis of grain-orientation effects in emerging metal-gate devices and implications for SRAM reliability”, IEDM Tech. Dig., paper 29.6, pp. 705-708, Dec. 2008.

[13] C. Yu, *et al.*, "Statistical simulation of metal-gate work-function fluctuation in emerging High-K/Metal-Gate CMOS devices", Proc. SISPAD, paper 9A-4, Sept. 2010.

[14] K. Xiu, "Simulation of phonon-limited mobility for nano-scale Si-based n-type non-planar device under general orientation and stress condition", Journal of Computational Electronics, Vol. 7, No. 3, 172-175, 2009.

[15] T. Ando, *et al.*, “Understanding mobility mechanisms in extremely scaled HfO2 (EOT 0.42 nm) using remote interfacial layer scavenging technique and Vt-tuning dipoles with gate-first process”, IEDM Tech. Dig., paper 17-1, Dec. 2009.

[16] M.V. Fischetti, *et al.*, “Effective electron mobility in Si inversion layers in MOS systems with a high-κ insulator: The role of remote phonon scattering”, J. Appl. Phys. 90, 4587-4608, 2001.

[17] S.E. Laux, *et al.*, “Ballistic FET modeling using QDAME: Quantum Device Analysis by Modal Evaluation,” IEEE Trans. Nanotech., vol. 1, pp. 255-259, Dec. 2002.

[18] S.E. Laux, *et al.*, “Analysis of quantum ballistic transport in ultra-small silicon devices including space-charge and geometric effects,” J. Appl. Phys., vol. 95, pp. 5545-5582, May 2004.

[19] S. E. Laux, *et al.*, "Monte Carlo simulation of submicron Si n-MOSFETs at 77 and 300 K", IEEE Electron Device Letters, vol. 9, No. 9, pp. 467-469, September, 1988.