TCAD Challenges and some Fraunhofer Solutions

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Abstract— **In order to meet its industrial target to reduce the development time and costs for new semiconductor technologies, devices and circuits, TCAD must meet various challenges which are outlined in the ITRS. After a short outline of these challenges, related results obtained at Fraunhofer for the simulation of lithography and other topography steps, dopant diffusion/activation, device architectures and impact of process variations are summarized.**

Keywords-ITRS; lithography, topography, dopant diffusion and activation; device architectures; process variations and windows

I. INTRODUCTION

TCAD is one of the very few enabling technologies which can contribute to the reduction of times and costs in the development of nanoelectronics technologies and devices. This is among others documented in Table MS3 of the 2009 issue of the International Technology Roadmap for Semiconductors ITRS [1], where the development costs and time reductions were in best practice cases estimated e.g. for 2011 at 35% and 37%, respectively. This estimate was based on a survey with TCAD users in industry, and continues to hold. In order to continue to meet such ambitious targets for the reduction of development time and costs, efficient research work on models and simulation tools is needed which is focused on the industrial requirements for future products. In turn, the Modeling and Simulation chapter of the ITRS has ever been written from the industrial point of view. Unfortunately, in parallel to the increasing costs of manufacturing facilities and experiments the work reported at leading simulation conferences such as SISPAD has during the last couple of years got less in line with these requirements, with an increasing share of academically interesting but industrially less relevant papers, and, in turn, less participation from industry. However, as will be shown in the following many problems need to and can be addressed which are both scientifically interesting and industrially relevant.

II. TCAD CHALLENGES IN THE ITRS

Within the ITRS, Modeling and Simulation is a crosscut chapter, which means that its content is largely derived from the requirements of the other ITRS chapters which deal with the real processes, devices and hardware tools. This view is complemented by experts' knowledge about the state-of-the-art and the technical and scientific possibilities in Modeling and Simulation. A very severe non-scientific problem, however, is the general shortage of resources which frequently prevents research requested by the ITRS to be performed in time. In consequence, results on models and tools are frequently not available on ITRS schedule.

The Modeling and Simulation challenges of the ITRS span a wide range from equipment-related issues to compact modeling. Materials, reliability, variations and algorithms are included almost everywhere. The short-term (until 2017) challenges of the 2010 ITRS include

- Lithography simulation including EUV;
- Front-end process modeling for nanometer structures;
- Integrated modeling of equipment, materials, feature scale processes and influence on device and circuit performance and reliability, including random and systematic variability;
- Nanoscale device simulation capability: Methods, models and algorithms;
- Electro-thermal-mechanical modeling for interconnect and packaging;
- Circuit element and system modeling for high frequency (up to 300 GHz) applications;

whereas the long-term challenges (2018 – 2024) include

- Modeling of chemical, thermomechanical and electrical properties of new materials;
- Nano-scale modeling for Emerging Research Devices and Interconnects including Emerging research Materials;
- Optoelectronics modeling; and
- NGL (next generation lithography) simulation.

These challenges are detailed in Table MS1 of the Modeling and Simulation chapter. More explanations are then given in the text of the Modeling and Simulation chapter. At the time of writing this paper, the 2011 Modeling and Simulation Challenges have not yet been approved for publication. Nevertheless, it can be stated that these challenges are being maintained for 2011, however with important changes in the detailed "summary of issues", due to the shift of the ITRS time scale by two years, now giving projections until 2026. Following a first publication at the ITRS Summer Conference

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in July 2011 in San Francisco, these changes will also be presented in the oral talk at SISPAD.

III. SOME FRAUNHOFER SOLUTIONS

In this section, an overview of some activities and results obtained at Fraunhofer IISB is given.

A. Lithography Simulation

Traditionally, lithography simulation has not been in the focus of SISPAD, largely because a clear separation could be made between patterning issues and devices. However, this does no more hold, because especially this process step now faces severe physical limits which challenge further scaling. Moreover, lithography is among the most critical sources of variability, especially for fully depleted SOI transistors which are not affected by random dopant fluctuations.

The current ITRS requests for MPUs in 2011 a printed gate length of 35 nm – smaller than the theoretical resolution limit of 54 nm for dense lines printed with 193 nm wavelength lithography at a numerical aperture of 0.9. The consequence is shown in Fig. 1 with a simulation of the imaging of the acronym "IISB", using the research and development lithography simulator Dr.LiTHO of IISB [2]. For a numerical aperture (NA) of 0.9, the aerial image is largely blurred. State-of-the-art water immersion increases the NA to about 1.3 and results in an acceptable image quality. The resist pattern resulting from imaging with that NA and a usual development step is shown in Fig. 1d. Several elaborated physical methods are being used to further decrease the minimum feature size printed, including Extreme Ultraviolet Lithography (EUV) and double patterning techniques. Another key problem is that structures influence each other up to a distance of some

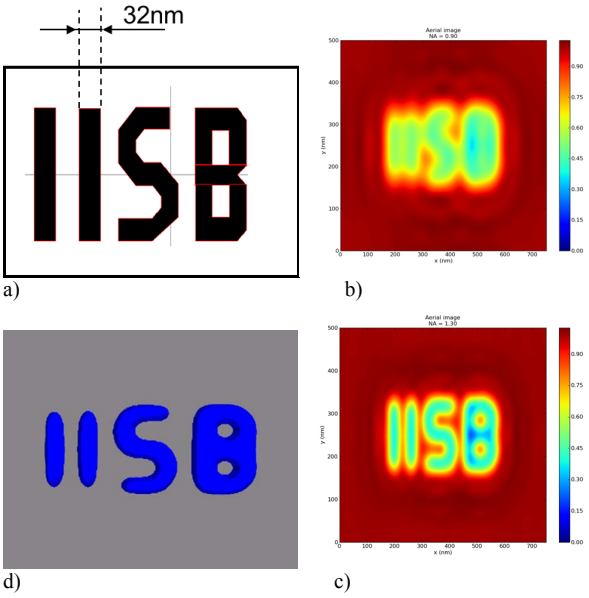

Figure 1. Basic sequence of lithography simulation (clockwise): a) mask; b) aerial image at NA = 0.9; c) aerial image at NA = 1.3; d) resist pattern after illumination with NA = 1.3 and resist development

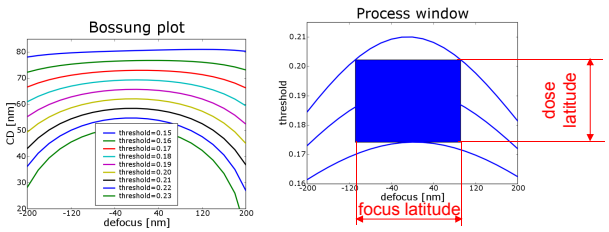

Figure 2. Bossung plot and process window for the printing of a dense array of 65 nm contact holes with 193 nm lithography at an NA of 1.35.

wavelengths, and that even small changes in a lithography step, e.g. the distance between the optical system and the wafer (defocus) drastically change the feature sizes printed (critical dimensions, CD). The immense experimental effort which would be needed to investigate these issues has led to a large demand for and wide usage of lithography simulation, and strong requirements on the accuracy and efficiency of lithography simulation tools. Within Dr.LiTHO, advanced physical models are implemented together with elaborated algorithms to meet at the same time the requirements on accuracy and CPU efficiency. This includes especially the rigorous solution of Maxwell's equations, alternatively with Finite Difference Time Domain (FDTD) and Waveguide Methods, treatment of oblique illumination with so-called Hopkins- and non-Hopkins approaches, domain decomposition, and various optimization tools. More information and especially a list of related publications is available at the internet [2], and will partly be given in the SISPAD presentation. In the following a few examples on the use of Dr.LiTHO are given. Fig. 2a shows the so-called Bossung plot for the printing of a dense array of 65 nm square contacts with 193 nm wavelength lithography at an NA of 1.35. Variations of the focus position or of the exposure threshold both change the printed CD from its desired nominal value of 65 nm. In the sketch of threshold vs. defocus extracted from this, see Fig. 2b, the resulting process window is shown, which is the maximum latitude in which focus and dose can vary independently but still lead to a maximum change of the CD of ±10%. Fig. 3 shows the resist structure for a contact hole area generated by double patterning. With this specific technique among others the usual rounding of the contact holes can largely be avoided. Generally, double patterning requires the capability to simulate lithography on topography, which is a specific feature of Dr.LiTHO. In Fig. 4, the simulation of the aerial image for the patterning of the polysilicon level of a 6T SRAM cell is shown. Due to the periodic boundary conditions

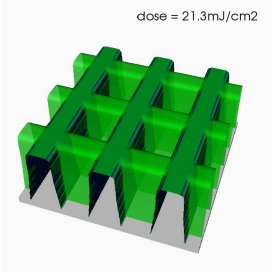

Figure 3. Simulation of contact hole area generated by 193 nm double patterning

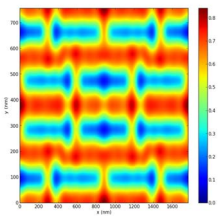

Figure 4. Aerial image of a 6T SRAM cell (domain extended due to periodic boundary conditions)

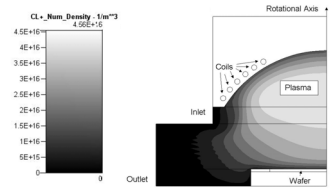

Figure 5. Concentration of Cl^+ ions in a plasma etching reactor

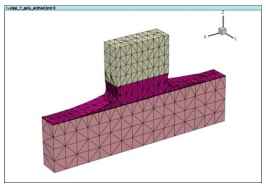

Fig. 6. Example of 3D etching simulation using triangulated surfaces

required, four neighboring cells were simulated, with an overall area of 1766 nm times 756 nm. Using the waveguide algorithm, the calculation of the mask spectrum took 40 seconds. A new algorithm then accelerated the calculation of the aerial image from 520 to 0.5 seconds.

B. Topography Simulation

Topography simulation is faced with the overall requirement to simulate the impact of the deposition, etching or CMP equipment on the features generated on the wafer, which leads to a multiscale simulation problem. At IISB, third-party computational fluid dynamics programs such as ESI-CFD [3] are used to extract ion concentrations and fluxes of relevant species just above the surface of the planar wafer. This information is then fed into feature-scale models which are specific for the deposition or etching process in question, and implemented in the IISB tools ANETCH [4] and DEP3D [5]. These models are used to calculate the local deposition or etch rates at each point of the feature in question, taking especially the feature geometry (e.g. shadowing) into account. Fig. 5 shows the concentration of Cl^+ ions in a plasma etching reactor, simulated with ESI-CFD. Using feature-scale models together with a surface triangulation [4] [5] as shown in Fig. 6, the 3D evolution of the geometry can be traced, resulting e.g. in quantitative data on the etch bias for dense and isolated lines, or on inhomogeneities across the wafer. Fig. 7 shows an example for Plasma Enhanced Chemical Vapor Deposition PECVD of oxide on a patterned substrate. A good agreement between simulation and experiment is obtained.

C. Simulation of Diffusion and Activation

Contemporary annealing processes primarily aim at achieving highest dopant activation at minimum diffusion and in parallel avoiding detrimental side effects such as increased leakage currents. Such processes are governed by the dynamics of dopants, point defects and their agglomerates. IISB has for many years cooperated with various partners in industry and academia to develop such models, e.g. in the projects

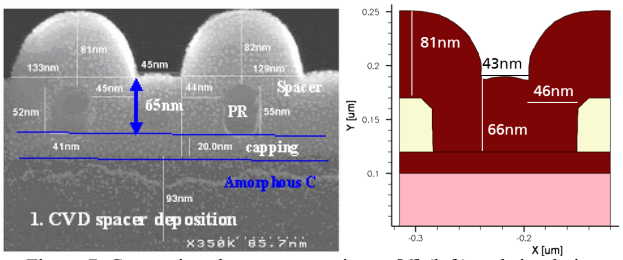

Figure 7. Comparison between experiment [6] (left) and simulation (right) of oxide spacer PECVD.

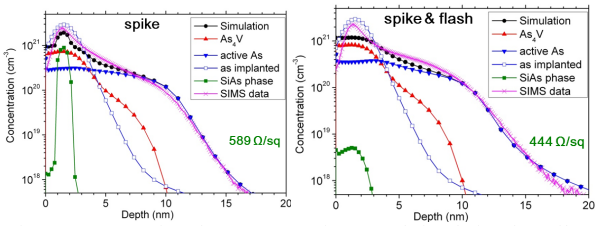

Figure 8. Comparison between experiment and simulation for spike (left) and combined spike/flash annealing (right)

ATOMICS [6] funded by the European Union from 2006 to 2009, and in the current EU project ATEMOX [7]. The key requirement has been to devise and carry out experiments which are suitable to separate between the various physical effects occurring, thus arriving with physical models and sets of parameters which describe not just some experiments used to calibrate the models, but furthermore predict experimental results for a wide range of process conditions. Models from these cooperations have been implemented into Sentaurus Process [8] and are thus being made widely available. Various papers (e.g. [9]) deal with the models developed, and a summary will be given in the SISPAD presentation. E.g. for arsenic, the model is based on the co-existence of active As together with As_4V agglomerates and a SiAs phase. Fig. 8 shows the comparison between experiment from Mattson Thermal products and simulation for spike and combined spike/flash annealing, yielding good agreement.

D. Investigation of Device Architectures

Various transistor architectures such as single- and double-gate fully depleted Silicon-in-Insulator (SG and DG FDSOI), FinFET or carbon-based devices have been suggested as options to replace bulk CMOS, and in turn intensively been simulated by several groups. Besides the nominal (and frequently very promising) performance of the "ideal" transistor it is crucial to also consider effects which may deteriorate device behavior. In view of this, IISB has studied the impact of parasitics (esp. contact resistance, capacitance) and variability on device performance, which challenge manufacturability and yield. For this work, mainly Sentaurus Device [8] has been used, after selection or adaptation of the required models. Bulk, SG and DG FDSOI and FinFET transistors have been compared with respect to various Figures of Merit, especially the delay which is approximated by CV/I and then depends on the parasitic resistances and capacitances considered. Fig. 9 shows the I_{on} and the CV/I, respectively, vs. I_{off} for typical 21 nm transistors in these architectures in comparison with high-performance specifications from the 2009 ITRS. Fig. 10 shows the CV/I for bulk and FinFET NMOS without considering contact resistance and with planar

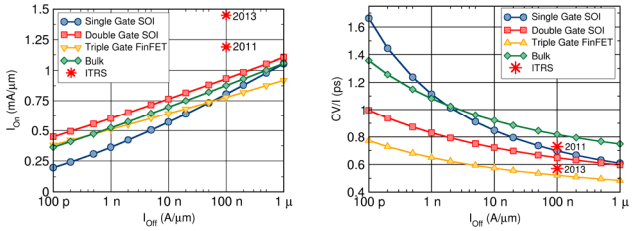

Figure 9. Comparison of different architectures of 21 nm NMOS transistors with ITRS specifications

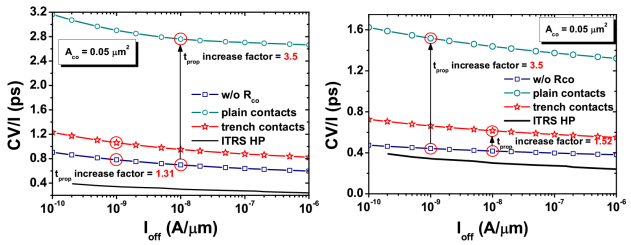

Figure 10. Comparison of delay CV/I between high performance specifications of 2007 ITRS and simulated values for 13 nm bulk NMOS (left) and FinFET (right) with various assumptions on contact resistance

and trench contacts, respectively [10]. The simulations show that the 2007 ITRS high-performance specifications seem to be too aggressive even if the contact resistance is neglected. Furthermore, there is no unique architecture which outperforms the others both for I_{on} and for CV/I and for all off-currents.

E. Process Variations

Most publications on process variations are limited to some effects like Random Dopant Fluctuations [11] [12] or Line Edge/Width Roughness [13] which can be treated directly in device simulation programs based on simple assumptions for the statistics of the variation. However, the impact of numerous effects like the focus variations in lithography or inhomogeneities of deposition and etch rates across the wafer, mentioned above, cannot be investigated without tracing the variability through the full chain of process and device simulation, and potentially up to circuit and system simulation. Moreover, it is very important to trace correlations between different variations, because standard corner models may be overpessimistic. This requires a holistic hierarchical approach which has been implemented by the five Fraunhofer institutes IISB, IIS/EAS, IMS, ITWM and SCAI in the internal Fraunhofer project HIESPANA [14]. Sources of process variations and the methodology to treat process variations including correlations have been discussed in a recent paper [15], whereas some results of variability studies from equipment up to circuit and system level have been presented in [16]. Fig. 11 shows a simple but nevertheless important result: A symmetric (Gaussian) distribution of the defocus in the lithography step used for gate patterning leads to an asymmetric (Generalized Extreme Value GEV) distribution of the gate length, which is also transferred to a GEV distribution of the threshold voltage for FD SOI transistors. The 32 nm bulk transistor also shown has a symmetric distribution of the threshold voltage, due to the pocket doping used.

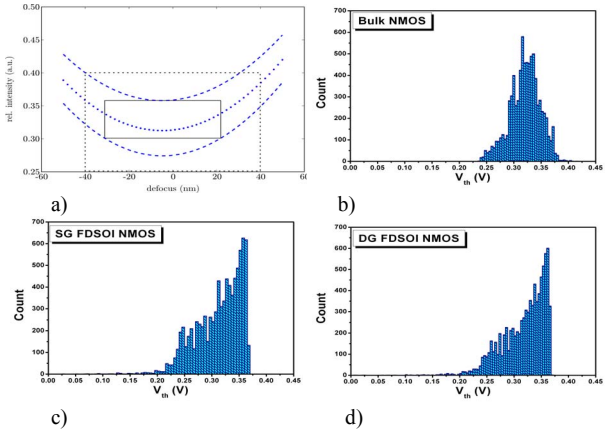

Figure 11. Typical process window (a) in a 193 nm water immersion lithography step and its simulated impact on 32 nm bulk (b), SG (c) and DG SOI (d) NMOS transistors [15]

IV. Conclusions and Outlook

With physical limits of scaling approaching, the importance of a sound physical understanding of materials, processes and devices is ever growing in order to be able to help to find workarounds and innovative solutions. Due to the diversity of the technological options and device architectures, the application of predictive simulation tools is indispensible, especially because moderate changes of some target figures, e.g. the off-current specified, may lead to a different choice of the optimum process or architecture. Especially, besides the nominal device or circuit behavior also its variability – and variability combined with reliability - must be considered.

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