Simulation of Line-Edge Roughness Effects in Silicon Nanowire MOSFETs

Tao Yu, Runsheng Wang and Ru Huang* Key Laboratory of Microelectronic Devices and Circuits, Institute of Microelectronics Peking University, Beijing 100871, China *E-mail: ruhuang@pku.edu.cn

Abstract—In this paper, the effects of nanowire (NW) lineedge roughness (LER) in gate-all-around (GAA) silicon nanowire MOSFETs (SNWTs) are investigated by 3-D statistical simulation in terms of both performance variation and mean value degradation. A physical model is developed for NW LER induced performance degradation in SNWTs for the first time. The results indicate large performance mean value degradations due to NW LER in SNWTs. However, the LER induced parameter variation is still acceptable. In addition, as the LER correlation length (Λ) scales beyond the gate length, new distribution of performance parameters is observed, which has dual-peaks rather than single in conventional Gaussian distribution. The optimization for NW LER parameters is given for SNWT design as well.

I. INTRODUCTION

Recently, the silicon nanowire MOSFET (SNWT) with gate-all-around (GAA) architecture has attracted much attention due to its excellent immunity to short channel effects [1-4]. On the other hand, line-edge roughness (LER), which is due to an inevitable difference between the designed pattern and the geometries after lithography and etching, has become a great challenge to device robustness [5]. Particularly, different from gate-LER in conventional devices, nanowire (NW) LER in SNWT has a direct impact on the device channel. Also, due to the unique feature of NW structure, the NW LER contains two degrees of freedom (Fig. 1), which may influence the device performance in a complicated way. However, only few studies on the impacts of NW LER to SNWTs have been reported [6-8].

In this paper, a 3-D statistical simulation is performed to estimate the NW LER effects in SNWTs. Furthermore, the modeling of LER effects is in ample necessity for device optimization and circuit design. Yet, few studies on LER modeling are proposed [9] due to the difficulty in analyzing stochastic behavior of LER. In this work, a compact model, based on the probability theory, is also developed to account for the performance degradation caused by the LER effect in SNWTs.

II. SIMULATION METHOD

In order to identify the relative importance of diameter variation and center position variation in NW LER, two basic types of LER are adopted in the simulation (Fig. 2): type A has aligned centers but varying diameters, while type



Fig. 1. The schematic view of nanowire with 2-D LER effect: the upper edge and the lateral edge vary differently.

B has fixed diameter but varying centers. Then, the random LER sequences with LER parameters from a variety of range are generated by using the Fourier synthesis on the power spectrum of Gaussian autocorrelation [5]. The full-3D device simulation is then performed using carefully calibrated TCAD Tools [10-11]. The geometry parameters of the SNWTs are listed in Table. 1. For each set of device and LER parameters, 200 samples are simulated for statistical analysis.

III. MODELING OF LER INDUCED DEGRADATION

Firstly, two assumptions are made for the modeling of LER induced degradations in SNWTs: (1) threshold voltage (V_{th}) is dominated by the largest V_{th} in the region under gate control; (2) the transport of carrier is restricted by the smallest diameter. Then, since the root mean square (Δ) of LER is the standard deviation of the lateral deviations along the edge (Fig. 3 (a))

$$\Delta^{2} = \frac{1}{N-1} \sum_{i=1}^{N} \left(y_{i} - \overline{y} \right)^{2}$$
(1)

the maximum/minimum lateral deviation value has the distribution

$$f_{\max}(y) = \frac{d(P(y_{\max} < y))}{dy} = \frac{d(P^{N}(y_{i} < y))}{dy}$$
$$= \frac{N}{\Delta} \left[\Phi\left(\frac{y}{\Delta}\right) \right]^{N-1} \frac{1}{\sqrt{2\pi\Delta^{2}}} e^{-\frac{y^{2}}{2\Delta^{2}}}$$
$$f_{\min}(y) = \frac{d(P(y_{\min} < y))}{dy} = \frac{d((1 - P(y_{i} > y))^{N})}{dy}$$
$$= \frac{N}{\Delta} \left[1 - \Phi\left(\frac{y}{\Delta}\right) \right]^{N-1} \frac{1}{\sqrt{2\pi\Delta^{2}}} e^{-\frac{y^{2}}{2\Delta^{2}}}$$
(2)

This work was partly supported by the NSFC (60625403 and 90207004), 973 Projects (2006CB302701), and National Science & Technology Major Project (2009ZX02035-001).



Fig. 2. The schematic view of SNWTs with two types of LER: type A has fixed center position and varying diameter, type B has unified diameter but varying center position.

TABLE. I. GEOMETRY AND DOPING PARAMETERS FOR SNWTS

Parameter	Value
Nanowire Diameter	10 nm
Gate Length	25 nm
Channel Doping	Intrinsic
Soure/Drain Extension	22.5nm
Oxide Thickness	2.5 nm

where $\Phi(x) = \int_{-\infty}^{x} (\sqrt{2\pi})^{-1} \exp(-\xi^2/2) d\xi$.

Fig. 3 (b) indicates that the distribution density function is similar to Gaussian shape, hence, Gaussian distribution with the same expectation value and variance is used to approximate the distribution of the maximum/minimum lateral deviation. As for electrostatics, $\overline{V_{th}}$ of SNWTs with type A LER can be obtained by substituting radius R with $R + y_{\min}$ in the expression of V_{th} . On the other hand, due to the excellent electrostatics of GAA structure, V_{th} shows little sensitivity to type B LER. As for transport, the whole NW can be regarded as several transmission conductors in series and each one has the same transmission coefficient, as shown Fig. 4. For a single transmission conductor, the transmission mechanism is different for the two types of LER and result in different transmission coefficient. The reflections in channel with type A LER occur at the same position and do not result in resonance effect, as in channel with type B LER. Also, considering the quantum confinement induced carrier profile, which can be obtained from variational wave-function in cylindrical channel [12]

$$\varphi(r;R_i) = a_i \sqrt{\frac{1}{R_i}} \sin\left(\frac{\pi(r+R_i)}{2R_i}\right) \exp\left(-\frac{b_i(-r+R_i)}{2R_i}\right)$$
(3)

where i=1, 2 for type A and type B LER, a_i is normalization factor and b_i is the variational parameter, the reflection coefficient of a single reflection flow can be written as:

$$R_{coeff}^{i} = \frac{1 - T_{i}}{2} = \frac{(1 - \gamma_{i}) \int_{R_{i}}^{R_{i}} |\varphi(r; R_{i})|^{2} dr}{2 \int_{0}^{R_{i}} |\varphi(r; R_{i})|^{2} dr}$$
(4)



Fig. 3. (a) The root mean square is the standard deviation of the deviation value of the *N* sample points, and y_{max} and y_{min} are critical parameters for LER modeling. (b) The probability density of y_{max} and y_{min} , and the inset: expectation and standard deviation of y_{max} and y_{min} with root mean square.



Fig. 4. The whole nanowire can be regarded as several transmission conductors in series. The two types of LER determine the transmission coefficient in different ways.

where γ is the mobility degradation factor, $R_1 = R_{ideal}$, $R_2 = R_{ideal} + \overline{y_{max}}$, $R'_i = R_i - (\overline{y_{max}} - \overline{y_{min}})$. The transmission coefficient of a single transmission conductor can be obtained

$$T_{coeff}^{i} = \begin{cases} T_{1} & \text{for } i = 1\\ \frac{1+T_{2}}{3-T_{2}} & \text{for } i = 2 \end{cases}$$
(5)

Finally, taken into account resonance effect between the conductors [13], the overall transmission coefficient is given as:

$$T_{coeff}^{i} = \frac{T_{coeff}^{i}}{n(1 - T_{coeff}^{i}) + T_{coeff}^{i}}$$
(6)

where
$$n = \begin{cases} L_g / \Lambda & (L_g \ge \Lambda) \\ 1 & (L_g < \Lambda) \end{cases}$$
,



Fig. 5. The model is compared with TCAD simulation results. The mean value of I_{on} degrades as Λ reduces, and Δ shows little impact on average I_{on} .

the drain current is estimated by $I = T_{coeff}^{i} \times I_{0}$. As can be seen from Fig. 5, $\overline{I_{on}}$ and $\overline{V_{th}}$ with varying LER parameters are in good consistence with numerical simulation result.

IV. RESULTS AND DISCUSSION

A. LER Induced SNWT Performance Degradation

Fig. 5 demonstrates the large mean value degradation in I_{on} as Λ decreases, which can be explained by the model of LER induced degradation. Besides, type B LER causes larger degradation by about 7%. Due to the strong quantum confinement, since the carrier centroids in SNWTs with type A LER are mostly aligned, the scattering at the surface is not as severer as in those with type B LER, in which the irregular carrier distribution results in irregular electric field and more scattering at the surface.

B. The Scaling of LER Parameter

As the gate length scales rapidly, Λ may exceed the gate length since the gate covers only part of the nanowire. On the other hand, process, such as self-limiting oxidation and H₂ annealing, may further accelerate such trend [14]. Under



Fig. 6. V_{th} distribution of SNWTs with (a) type A LER and (b) type B LER. Dual-peak property is observed in SNWTs with type A LER when $\Lambda > L_g$.



Fig. 7. The normalized variations of I_{on} and V_{th} with varying (a) Λ and (b) Δ .

such circumstance, anomalous statistics as shown in the histograms of V_{th} in Fig. 6 are observed, which shows distinctive dual-peak property in SNWTs with type A LER. Therefore, considering the asymmetric shape of either peak, the half-Gaussian statistics [15] is adopted, and the superposition of the two peaks is evaluated using the principle of variance superposition:

$$\sigma_{total}^2 = \sigma_1^2 + \sigma_2^2 \tag{7}$$

Conventional Gaussian statistics is used for type B LER due to its symmetric distribution.

C. Optimization for LER Parameters

Fig. 7 plots the normalized statistics (σ/μ) of V_{th} and I_{on} as functions of Λ and Δ . The result indicates that the variability of SNWTs remains stable under the condition of $\Lambda > L_g$, while in the case of $\Lambda < L_g$ type A LER causes decreased variation and type B causes increased variation. The larger variation caused by type A LER under $\Lambda > L_{g}$ originates from the dual-peak characteristics of performance parameters. Nevertheless, SNWTs still exhibit effective immunity against LER variation since all statistics pass the $\mu - 6\sigma$ test for matching consideration in SNWT-based ICs. On the other hand, as discussed in subsection A, LER induces non-negligible performance degradation in SNWTs, which should be carefully taken into account. As for an optimized Λ , since SNWTs demonstrate remarkable immunity to LER induced variation, $\Lambda/L_g > 1$ should be achieved to ensure acceptable performance degradation. For the rms Δ , the performance parameter variation can be further inhibited if $\Delta/R < 0.1$ can be obtained.

V. SUMMARY

In this paper, the LER effects in SNWTs are investigated by 3-D statistical simulation, and a physical model for NW LER is also developed for the first time. The results indicate large performance mean value degradation originated from small correlation length and center position variation. On the other hand, SNWTs exhibit effective immunity against NW LER induced performance variation. In addition, dual-peak distribution caused by type A LER under the condition of $\Lambda > L_g$ is observed, which requires the half-Gaussian statistics and variance superposition principle for reasonable statistics. Furthermore, the statistics provides a guideline for NW LER parameter optimization to meet various design specifications.

ACKNOWLEGEMENTS

The authors would like to thank Dr. Jiang Chen for valuable discussions.

References

- Y. Cui, Z. Zhong, D. Wang, W. Wang and C. M. Lieber, "High performance silicon nanowire field effect transistors," *Nano Lett.*, vol. 3, no. 2, pp. 149-152, Feb. 2003.
- [2] J. Wang, E. Polizzi, and M. Lundstrom, "A computational study of ballistic silicon nanowire transistors," in *IEDM Tech. Dig.*, 2003, pp. 29.5.1–29.5.4.
- [3] Y. Tian, R. Huang, Y. Wang, J. Zhuge, R. Wang, J. Liu, X. Zhang, and Y.Wang, "New self-aligned silicon nanowire transistors on bulk substrate fabricated by epi-free compatible CMOS technology: Process integration, experimental characterization of carrier transport and low frequency noise," in *IEDM Tech. Dig.*, 2007, pp. 895–898.

- [4] T. Ernst, L. Duraffourg, C. Dupré, E. Bernard, P. Andreucci, S. Bécu, E. Ollier, A. Hubert, C. Halté, J. Buckley, O. Thomas, G. Delapierre, S. Deleonibus, B. de Salvo, P. Robert, and O. Faynot, "Novel Sibased nanowire devices: Will they serve ultimate MOSFETs scaling or ultimate hybrid integration?" in *IEDM Tech. Dig.*, 2008, pp.745-748.
- [5] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness," *IEEE Trans. Electron Device*, vol. 50, no.5, pp. 1254-1260, May. 2003.
- [6] J. Zhuge, R. Wang, R. Huang, J. Zou, X. Huang, D.-W. Kim, D. Park, X. Zhang, and Y. Wang, "Experimental investigation and design optimization guidelines of characteristic variability in silicon nanowire CMOS technology," in *IEDM Tech. Dig.*, 2009, pp. 61-64.
- [7] S. D. Suk, Y. Y. Yeoh, M. Li, K. Hwan Yeo, S-H. Kim, D-W. Kim, D. Park, and W-S. Lee, "TSNWFET for SRAM cell application: performance variation and process dependency," in *Sympos. VLSI Tech. Dig.*, 2008, pp. 38-39.
- [8] T. Yu, W. Ding, J. Zhuge, R. Wang, and R. Huang, "Investigation on the effective immunity to process induced line-edge roughness in silicon nanowire MOSFETs," in *17th International Symposium on* VLSI Technology, Systems and Applications (VLSI-TSA), 2010, pp. 32-33.
- [9] K. Patel, T.-J. King, and C.J Spanos, "Gate line edge roughness model for estimation of FinFET performance variability," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 3005-3063, 2009.
- [10] Sentaurus TCAD User's Manual, Synopsys, CA, 2005;
- [11] R.Wang, J. Zhuge, and R. Huang, "Simulation of analog/RF performance and process variation in nanowire transistors", in *Proc.* of SISPAD, 2007, pp.381-384.
- [12] B. Cousin, O. Rozeau, M.-A. Jaud, J. Jomaah, "A physics-based compact model of quantum-mechanical effects for thin cylindrical Si-Nanowire MOSFETs", in 16th International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 2009, pp. 107-108.
- [13] S. Datta, Electronic Transport in Mesoscopic Systems, Cambridge University Press, 1997;
- [14] S. Bangsaruntip, G. M. Cohen, A. Majumdar, Y. Zhang, S. U. Engelmann, N. C. M. Fuller, L. M. Gignac, S. Mittal, J. S. Newbury, M. Guillorn, T. Barwicz, L. Sekaric, M. M. Frank, and J. W. Sleight. "High Performance and Highly Uniform Gate-All-Around Silicon Nanowire MOSFETs with Wire Size Dependent Scaling", in *IEDM Tech. Dig.*, 2009, pp. 297-300.
- [15] E. Baravelli, A. Dixit, R. Rooyackers, M. Jurczak, N. Speciale, and K. D Meyer, "Impact of line-edge roughness on FinFET matching performance," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2466–2474, Sep. 2007.