Characteristics of the Capacitorless Double Gate Quantum Well Single Transistor DRAM

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***Abstract*— We characterize and optimize Double Gate (DG) single-transistor (1T) DRAM via extensive simulations. We propose a new kind of DRAM: 1T-Quantum Well DRAM: which has a "storage pocket" for holes within the body. This memory gives the opportunity to engineer spatial hole distribution within the body of the device, which is not possible with the conventional 1T DRAMs. Using this novel device we demonstrate approximately 2 order of magnitude increase in the drain current (I_d) difference between the reads of two states of the memory. We study the retention characteristics of this novel DRAM, and also investigate the effect of Quantum Well depth on the retention characteristics.**

I. INTRODUCTION

Capacitorless DRAM, because of its smaller size, has been aggressively researched recently [1]-[5]. We experimentally demonstrated for the first time a Double Gate (DG) Vertical capacitorless 1-Transistor DRAM (current flow perpendicular to the wafer) on bulk silicon substrate [6]. In this device, one of the MOS gates is used as a conventional switching transistor whereas, the other (back) gate is used to create the floating body storage node to store excess holes. By reverse biasing the back gate, the excess holes are kept in the body and the memory operation is obtained. In the current work, we use extensive simulations to find the optimum parameters for the DG 1T DRAM. Subsequently, we introduce a novel capacitorless 1-Transistor Quantum Well DRAM (1T-QW DRAM). This new memory has superior characteristics, such as the ability to produce higher threshold voltage (V_t) shifts and also control over the distribution of the holes within the body. The distribution of stored holes can be effectively moved closer to the front gate, which is impossible in the 1T DRAM where holes are stored just close to the back gate interface. This property not only results in increased shift in V_t but also in a higher retention time.

TABLE I. COMPARISON OF SRAM & DRAMS

	1T QW DRAM	1T DRAM	DRAM	SRAM
Structure	1T	1T	1T/1C	6T
Cell Size	$4F^2$	$4F^2$	$8F^2$	$100F^2$
Storage	Quantum Well	Floating Body	Capacitor	Flip Flop
Speed	Fast	Fast	Fast	Ultra Fast
Read	Non destructive	Non destructive	Destructive	Non destructive
Scalability Issues	Lithography	Lithography	Capacitor	6T size
New Materials	Ge, SiGe, III-V	None	High K	None

II. RESULTS

Some features of SRAM and various DRAMs are summarized in **Table I.** SRAM is ultra fast, but occupies a very large area due to its 6-Transistor structure. DRAM is fast, but the existence of the capacitor is getting increasingly problematic for the scaled next generation devices. 1T DRAM gets rid of the capacitor, which also reduces the device cell size by half compared to conventional capacitor based DRAM. The 1T-QW DRAM also gets rid of the capacitor and in addition incorporates the Quantum Well (QW) for the charge storage. **Fig. 1** shows the schematics of the novel capacitorless double gate 1T-QW DRAM. **Fig. 2** illustrates the corresponding band diagrams. **Fig. 3** shows Sentaurus simulations explicitly demonstrating the operation of a DG 1T DRAM: the V_d, V_{g1}, and I_d corresponding to program (P), followed by read (R1), erase (E), and a second read (R2). Operating voltages are given in Table IIa.

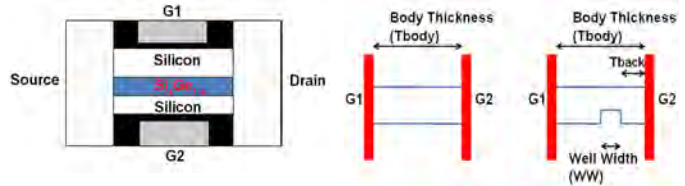

Fig. 1 The schematic of the novel single transistor double gate quantum well DRAM (1T-QW DRAM)

Fig. 2 Band diagrams of DG 1T DRAM and the novel single transistor double gate quantum well DRAM (1T- QW DRAM)

TABLE IIA. OPERATING VOLTAGES FOR THE 1T- QW DRAM CELL

	Program (Write "1")	Erase (Write "0")	Read	Hold
Gate 1 Voltage (V)	1	1.5	0.8	0
Drain Voltage (V)	1.2	-1.5	0.2	0
Gate 2 Voltage (V)	-1.5	-1.5	-1.5	-1.5

TABLE IIB. OPERATING VOLTAGES FOR THE 1T-QW DRAM CELL WITH POWERERASE

	Program (Write "1")	Erase (Write "0")	Read	Hold
Gate 1 Voltage (V)	1	1.5	0.8	0
Drain Voltage (V)	1.2	-1.5	0.2	0
Gate 2 Voltage (V)	-1.5	1.5	-1.5	-1.5

Fig. 4 shows the drain current difference between states R1 and R2 as a function of back gate voltage (V_{g2}) and body thickness (T_{si}) for DG 1T DRAM. The same parameter is shown as a function of body doping and T_{si} in **Fig. 5** and as a function of body doping and V_{g2} in **Fig. 6.** From these figures,

it is seen that the body thickness around 80nm yields the optimum results.

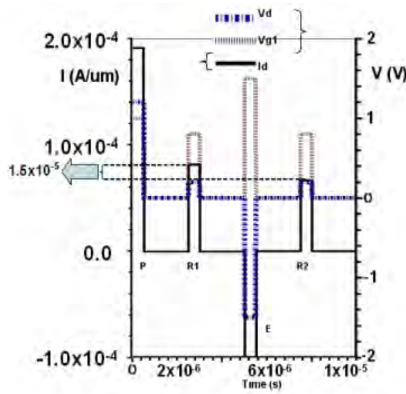

Fig. 3 Simulation result which shows the drain current and applied voltages vs. time. (Tbody=100nm)

Here, the parameter of interest is the difference in I_d at R1 and R2, since it captures not only information related to the V_t shift, but also to the retention (since the reads are done after some time passes after programming and erase). From the above results we see that the performance is unsatisfactory for thin body devices, which might be a problem from the scalability perspective. We circumvent this problem by introducing a novel Double Gate single transistor Quantum Well DRAM (1T-QW DRAM) [7]. This novel memory can be realized as a horizontal double gate structure using techniques similar to the transistor fabricated in [8]. It can also possibly be realized as a vertical double gate structure [6], or as a FINFET device if appropriate vertical epitaxial techniques become available. One example in which this concept can be realized is using Si and Ge (or SiGe). In this paper the QW width is taken as 5nm and Si/Ge/Si heterostructure is chosen, and the gate length is 250nm, unless otherwise is stated. Ge thickness larger than 5nm can result in defects due to strain relaxation.

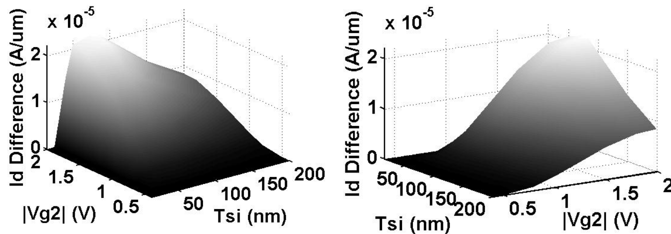

Fig. 4 Drain current difference between R1 and R2 as a function of gate2 voltage (Vg2) and body thickness (Tsi)

Fig. 7 compares I_d difference between R1 and R2 for the case with and without QW for devices for body thickness (T_{body}) of 100nm and 40nm. For the 100nm T_{body}, the QW device exhibits a 5x improvement, whereas the QW device performance is worse for thinner T_{body}. This is due to the fact that the holes cannot be purged as effectively in the presence of the QW. The problem is solved by introducing the "PowerErase" in which V_{g2} is switched to a positive value during Erase, in order to push holes away effectively. The new operating voltages are shown in Table IIb. In **Fig. 8**, it is seen that with the introduction of PowerErase, the improvement due to QWs in the 100nm and 40nm T_{body} devices is 7x and 8x, respectively.

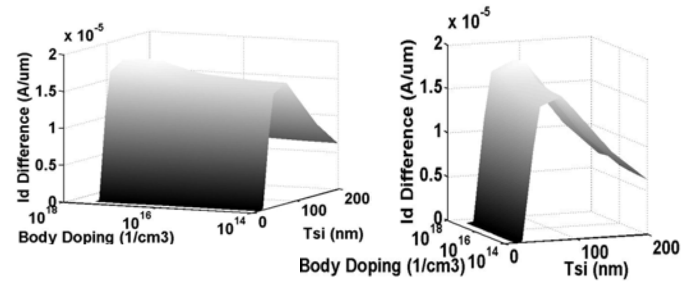

Fig. 5 Drain current difference between R1 and R2 as a function of body doping and body thickness (Tsi)

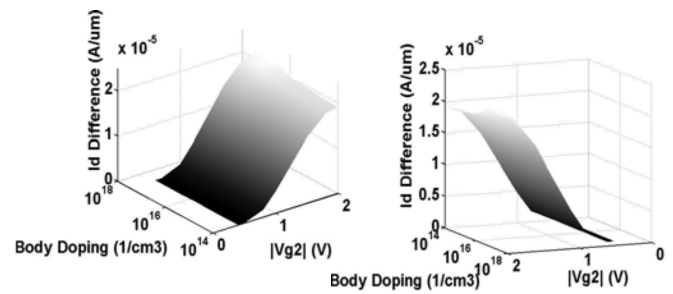

Fig. 6 Drain current difference between R1 and R2 as a function of body doping and Gate2 voltage (Vg2)

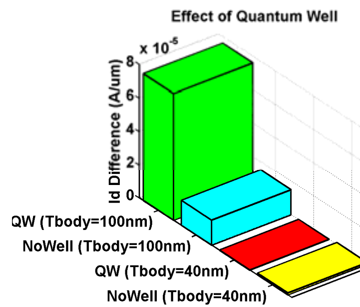

Fig. 7 Effect of quantum well on devices with Tbody={100nm, 40nm}. (WW=5nm, Tback=5nm, Lg=250nm)

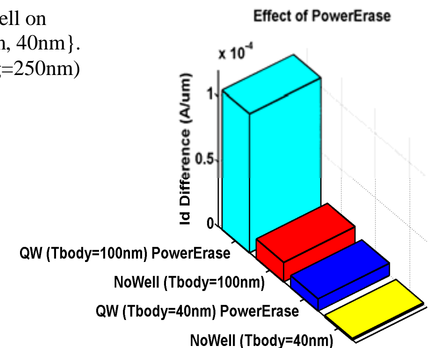

Fig. 8 Effect of PowerErase on devices with and without QW for Tbody= {100nm, 40nm}. (WW=5nm, Tback=5nm)

Apart from introducing a "storage pocket" for holes in the body via QW, this device also allows the engineering of

spatial distribution of the holes within the device body. **Fig. 9** shows the hole density within a device without a QW during programming, whereas, **Fig. 10** shows the results when there is a Ge QW 10nm away from the back gate interface (ie. T_{back}=10nm). The hole distribution is successfully shifted towards the front gate with the incorporation of the QW. **Fig. 11** shows that when the T_{back} is increased from 5nm to 10nm, the improvement in the 100nm body thickness device increases from 7x to 9x, and in the 40nm body thickness device it increases from 8x to 86x. The engineering of the spatial distribution of holes significantly improves the performance in the scaled device.

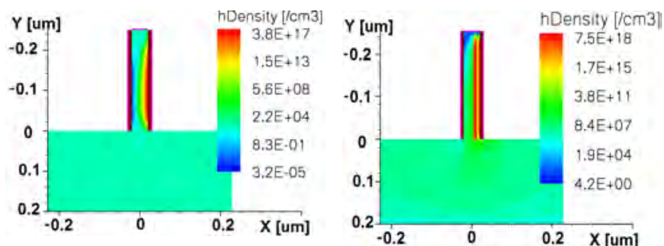

Fig. 9 Hole density during program (Tbody=40nm, No Quantum Well). **Fig. 10** Hole density during program in the device with Quantum Well (Tbody=40nm, Tback=10nm).

The QW gives us an effective control over the spatial distribution of the stored holes, which is not possible in the other 1T DRAMs. This novel DRAM makes it is possible to bring the stored holes closer to the front gate, thus, contributes to an increase in the amount of the V_t shift and signal margin. Also, in many cases it is desirable to keep the stored holes away from the back oxide interface due to presence of traps and dangling bonds. This further aids in improving extrinsic retention. This property is especially advantageous for materials such as Ge and III-V material systems, where passivation of interface traps is problematic.

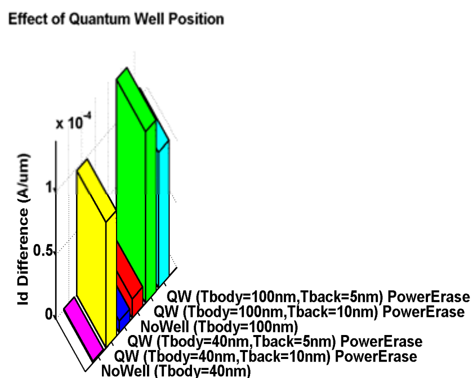

Fig. 11 Effect of QW position for Tbody={100nm, 40nm} and Tback={5nm, 10nm}

Fig. 12 shows the effect of gate length scaling on devices with and without QW. The devices with QW have better gate length scaling characteristics.

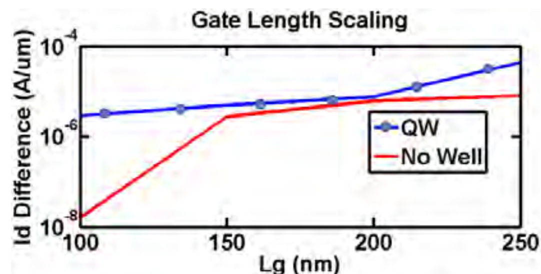

Fig. 12 Effect of Gate Length Scaling (Tbody=100nm, Tback=5nm)

Fig. 13 shows the retention characteristics at 300K & 358K for the devices with QW under read, and **Fig. 14** under the hold (for 60nm body thickness devices). **Fig. 15** compares the retention characteristics for the devices with and without QW at 358K. It can be seen that the QW devices have better characteristics in terms of higher difference in I_d and higher retention time. The characteristics of the QW devices can be improved further by using SiGe instead of pure Ge, and by engineering the depth of the QW, the '0' state (i.e. after Erase) behaviour is improved. **Fig. 16** shows the retention characteristics for devices with $Si_{(1-x)}Ge_{(x)}$ QW, where x is a parameter. It can be seen that one can use $Si_{0.5}Ge_{0.5}$ instead of pure Ge without getting much penalty in terms of retention and difference in I_d value corresponding to two memory states. This also helps to reduce the need for the PowerErase, since the QW is not as deep as the case with pure Ge. Furthermore, it is easier to obtain a better quality defect free interface in a Si/SiGe system, compared to a Si/Ge system, which also helps to achieve better retention times.

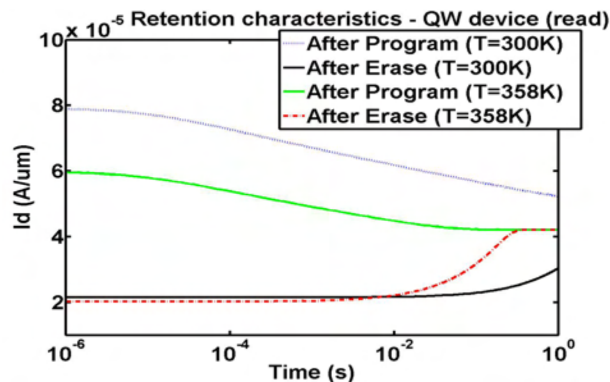

Fig. 13 Retention characteristics for devices with QW under read (Tbody=60nm, WW=5nm)

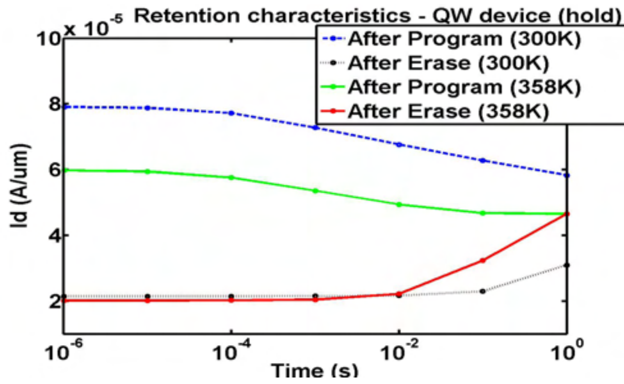

Fig. 14 Retention characteristics for devices with QW under hold (Tbody=60nm, WW=5nm)

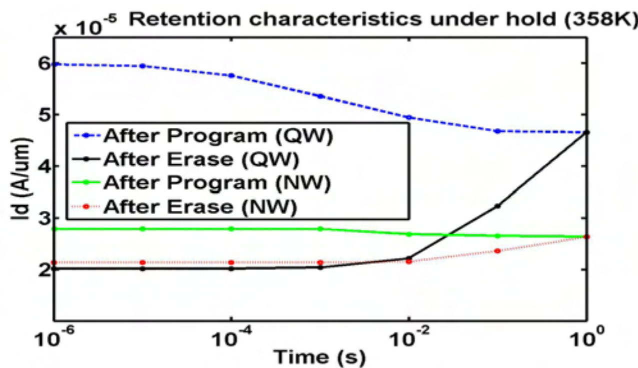

Fig. 15 Retention characteristics for devices with and without QW under hold at 358 K (Tbody=60nm, WW=5nm)

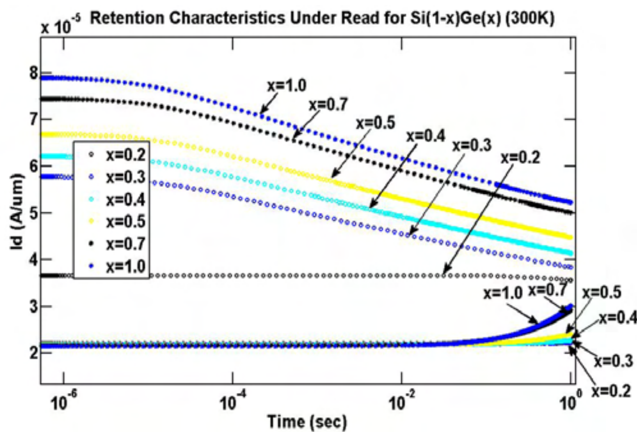

Fig. 16 Retention characteristics for devices with $Si_{(1-x)}Ge_{(x)}$ QW under read (Tbody=60nm, WW=5nm)

III. Conclusions

We characterized DG Capacitorless DRAM. In addition, we introduced a novel DRAM: 1T-QW DRAM. This new DRAM has several advantages in terms of performance and scalability. One of them is introducing a "storage pocket" within the device allowing the possibility of engineering the spatial distribution of the holes in the body of the device, which is not possible in the other 1T DRAMs. This new memory has the ability to have higher V_t shift, higher cell margin (ie. the difference in I_d corresponding to the reads of two states of the memory) and retention values, and therefore is a better candidate for scaled technology nodes. Furthermore, using SiGe in the Quantum Well instead of germanium brings additional advantages. We successfully quantify these advantages.

Acknowledgement

This work was supported by the Stanford University Initiative for Non-volatile Memory Materials and Devices (NMTRI) and a Stanford Graduate Fellowship.

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