Non-Quasi-Static Carrier Dynamics of MOSFETs under Low-Voltage Operation

M. Miyake, D. Hori, N. Sadachika,
U. Feldmann, M. Miura-Mattausch, and H.J. Mattausch
Graduate School of Advanced Sciences of Matter
Hiroshima University
Higashi-Hiroshima, Hiroshima 739–8530, Japan
Email: miyake-m053223@hiroshima-u.ac.jp

T. Iizuka, K. Matsuzawa, Y. Sahara,
T. Hoshida, and T. Tsukada
Semiconductor Technology Academic Research Center
Shin-Yokohama, Kanagawa, 222–0033, Japan
Email: tsukada.toshiro@starc.or.jp

***Abstract*—We analyze the carrier dynamics in MOSFETs under low voltage operation for a 90nm CMOS technology. For this purpose the displacement (charging/discharging) current, induced during switching operations is studied experimentally and theoretically. It is found that the experimental transient characteristics can only be well reproduced in the circuit simulation of low voltage applications by considering the carrier-transit delay in the compact MOSFET model. The switching frequency is found to decrease with reduced voltage due to diminished inversion condition and thus driving capability, which can be modeled with increased transit delay.**

I. Introduction

Low voltage operation of integrated circuits is an urgent requirement to expand the battery life in mobile applications as well as to contribute for reducing of global warming. However, it is no easy task to realize required circuit performances with low applied voltages. The main reason is the smaller driving capability of MOSFETs under this condition. It is well known that at low voltages the current is mostly governed by the diffusion rather than the drift mechanism, causing degradation of transient characteristics. However, it is an interesting task to investigate the feasibility. For this purpose we have investigated the MOSFET response at $V_{\rm gs}$ =1V (strong inversion) and 0.5V (weak inversion) with $V_{\rm ds}$ =0.1V experimentally and theoretically to analyze the differences in low voltage application. Long channel MOSFETs ($L_{\rm g} = 10\mu$m) fabricated with a 90nm CMOS technology are used to make the differences in the MOSFET behavior easily measurable and visible. The threshold voltage of the device is about 0.35V.

II. Method

A circuit simulator solves the continuity equation $\frac{dn(y,t)}{dt} = \frac{1}{qW}\frac{dI(y,t)}{dy}$ in the form

$$I(t) = I_0(V(t)) + \frac{dQ(t)}{dt} \qquad (1)$$

The first term is the conductive (transport) current and the second term is the displacement (charging/discharging) current. To derive Eq. (1) an instantaneous potential response to the voltage change is assumed [1]. Fig. 1 shows a schematic of the transient current on an arbitrary time scale. The second term of the right-hand side of Eq. (1), gives the current flow to fill or deplete the channel.

The question arises whether this formulation is still valid for low voltage applications with the resulting lower carrier speed. That means whether the separation of the transient current into the conductive current $I_0(V(t))$ and the charging current $\frac{dQ(t)}{dt}$ is still valid. For this purpose, we investigate the displacement current experimentally and theoretically.

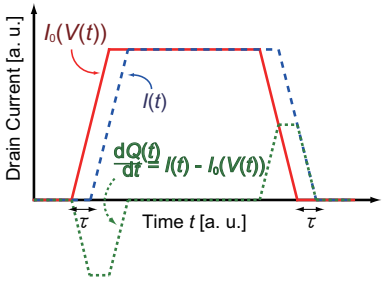

Fig. 1. Schematic of the switching characteristics for the transient currents as a function of time, comparing the quasi static current $I_0(V(t))$, with the total current where the displacement current is included.

III. Measurement Method

Fig. 2 shows a measurement setup for this study. Output

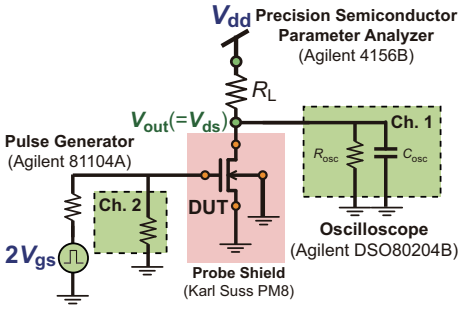

Fig. 2. Simplified measurement setup. $V_{\rm dd}$ is fixed and pulses are given on $V_{\rm gs}$.

voltage $V_{\rm out}$ of a resistance-loaded inverter is measured by an

978-1-4244-1753-7/08/$25.00 ©2008 IEEE

oscilloscope. Here, the voltage drop at the load resistance $R_{\rm L}$ is kept small about 1mV to consider the supply voltage $V_{\rm dd}$ to be equal to drain-source voltage $V_{\rm ds}$ of a MOSFET:

$$V_{\rm dd} - V_{\rm out} \simeq 1{\rm mV} \tag{2}$$

Drain current $I_{\rm d}$ can be calculated as

$$I_{\rm d} \simeq \frac{V_{\rm dd} - V_{\rm out}}{R_{\rm L}} - \frac{V_{\rm out}}{R_{\rm osc}} \tag{3}$$

where the conductive current through the input resistance of the oscilloscope $R_{\rm osc}$ is taken into account. However, the dynamic charging/discharging current at the input capacitance of the oscilloscope $C_{\rm osc}$ is not considered, since it can't be easily measured or calculated. Therefore, we solve the problem by using the 3dB-down cut-off frequency of the low-pass filter (LPF) consisting of $R_{\rm L}$ and $C_{\rm osc}$. The cut-off frequency is estimated with the relationship $f_{\rm c,LPF} = \frac{1}{2\pi R_{\rm L} C_{\rm osc}}$, where $R_{\rm L}$ is varied for each measurement bias condition according to the amount of on-state drain current. By substituting 1mV of Eq. (2) for calculating $f_{\rm c,LPF}$ using Eq. (3), we get $f_{\rm c,LPF}{}'$ at 1mV as

$$f_{\rm c,LPF}{}' = \frac{1}{2\pi \frac{1{\rm mV}}{I_{\rm d} + \frac{V_{\rm out}}{R_{\rm osc}}} C_{\rm osc}} \tag{4}$$

The switching speed must be slow enough compared to $f_{\rm c,LPF}{}'$ to ignore the dynamic current at $C_{\rm osc}$. All measurements for the present investigation were performed by keeping this condition valid.

Experimental extraction of the displacement current is explained in Fig. 3. Plots (a) and (b) show schematics of the transient current on an arbitrary time scale, comparing slow switching performance, of nearly steady-state characteristics, and fast switching performance. In the plot (c), the horizontal time axis is normalized to the rise/fall time of the switching pulse, and is named $t_{\rm norm}$. The difference between the fast and slow switching responses on the normalized time scale is the displacement current $I_{\rm disp}$, namely the second term of the right-hand side of Eq. (1).

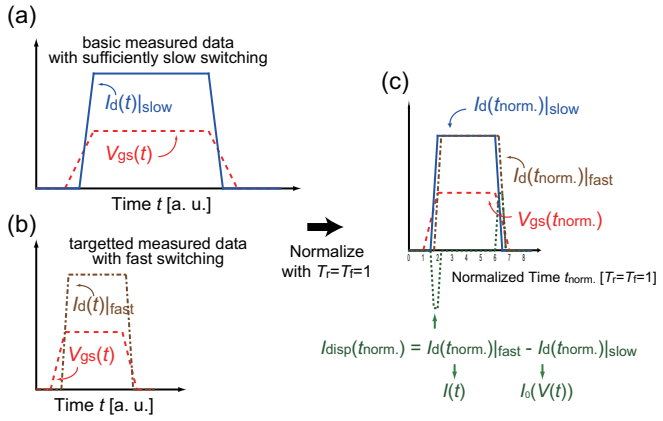

Fig. 3. Schematics of the switching characteristics for the transient currents as a function of time, comparing a slow switching performance, with a fast switching performance. The horizontal time axis $t_{\rm norm}$ of a schematic (c) is normalized to the rise/fall time of the fast switching pulse.

IV. Measured Results and Analysis

$V_{\rm dd}$ is fixed, and the pulse is given on $V_{\rm gs}$ with amplitudes of 1V and 0.5V. In this paper, we call the on-state value of the gate voltage pulse $V_{\rm gsH}$. Fig. 4 compares results of $V_{\rm gsH}$=0.5V to those of $V_{\rm gsH}$=1V at $T_{\rm r}$=100ns. Measurement inaccuracy is about 5% in the worst case, determined from the fluctuations in the current compared to its amplitude.

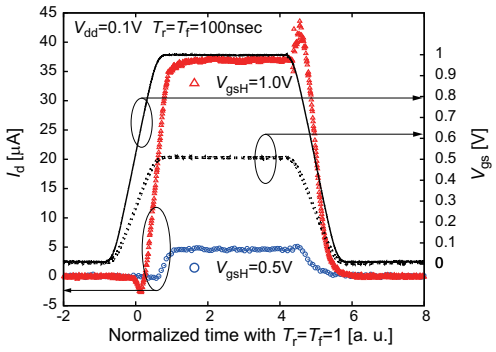

Fig. 4. Measured drain current $I_{\rm d}$ response for $V_{\rm gsH}$=1V and 0.5V with $V_{\rm dd}$=0.1V and $T_{\rm r}$=100ns. Device sizes are $L_{\rm g} = 10\mu$m and $W_{\rm g} = 20\mu$m. The x-axis is normalized so that $T_{\rm r} = T_{\rm f} = 1$.

Fig. 5(a) shows extracted displacement currents $I_{\rm disp}$ for switching pulses with $V_{\rm gsH}$=1V and 0.5V. For the extraction measured drain currents for $T_{\rm r}$=1ms are used as the slow-switching case. The $V_{\rm gsH}$=0.5V condition shows much smaller $I_{\rm disp}$. This can be understood from Fig. 6, showing smaller inversion charge for $V_{\rm gs}$=0.5V. The normalized $I_{\rm disp}$ for $V_{\rm gsH}$=1V and 0.5V are compared in Fig. 5(b). It is seen that $I_{\rm disp}$ for the low $V_{\rm gs}$ case shows different characteristics during switching-on and switching-off.

V. HiSIM and its NQS Model

HiSIM is a surface-potential-based MOSFET model for circuit simulation [2], [3]. In this work, SPICE3f5 is used as a circuit simulator.

Fig. 7 shows a comparison of simulated inversion-carrier-density distributions of a MOSFET along the channel with a 2D-device simulator for slow and fast switching frequencies (see Fig. 7(b)). The carrier deficit in the inversion layer in the fast frequency operation is due to the Non-Quasi-Static (NQS) effect. Carriers require time to respond to the potential change, which is modeled by considering the carrier delay τ in the NQS model of HiSIM. The delayed charge formation is modeled with τ as [4]

$$q(t_{\rm i}) = \frac{q(t_{\rm i-1}) + \frac{\Delta t}{\tau} Q(t_{\rm i})}{1 + \frac{\Delta t}{\tau}};\ \Delta t = t_{\rm i} - t_{\rm i-1}, \tag{5}$$

where $q(t_{\rm i})$ and $Q(t_{\rm i})$ represent the NQS and QS charge densities at the time $t_{\rm i}$, respectively.

τ consists of two delay mechanisms: One is responsible for the drift contribution, the other is for the diffusion contribution. These delay mechanisms are combined using the Matthiessen rule as shown in Fig. 8.

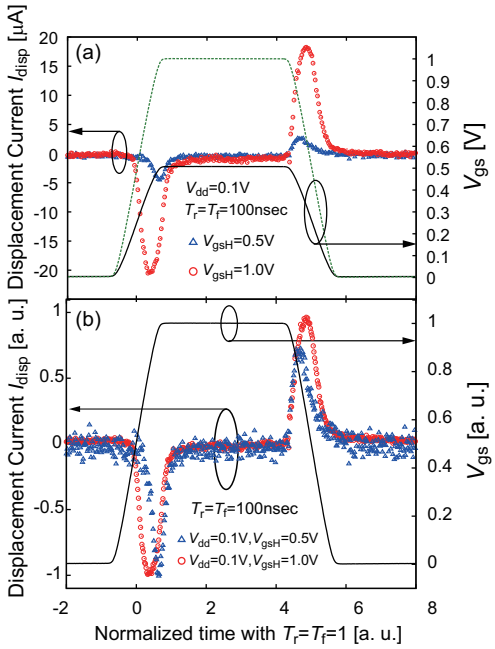

Fig. 5. Comparison of measured displacement currents at low gate voltage ($V_{\rm gsH}$ = 0.5V) and at high gate voltage ($V_{\rm gsH}$ = 1V). $T_{\rm r}$ for the fast switching is fixed to 100ns and $V_{\rm dd}$ = 0.1V is chosen for both cases.

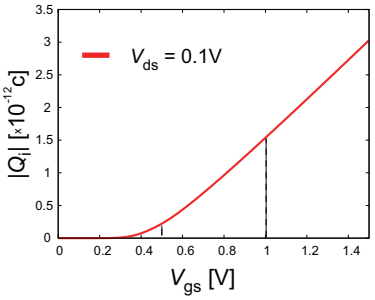

Fig. 6. Magnitude of the inversion charge of a MOSFET calculated by HiSIM as a function of $V_{\rm gs}$ for $V_{\rm ds}$=0.1V.

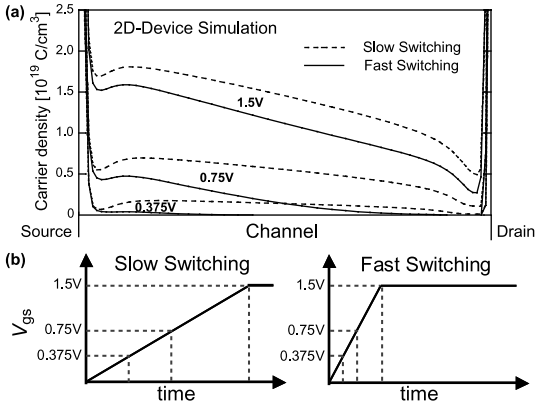

Fig. 7. (a) Carrier density distributions along the channel obtained by 2D-device simulation at two switching speeds shown in (b).

VI. Simulation Results with HiSIM

Figs. 9(a) and (b) show I-V characteristics of measured and simulated HiSIM results. Measured data is well reproduced.

Fig. 10 compares displacement-current measurements with HiSIM results. For the HiSIM simulation, the same circuit as shown in Fig. 2 is applied. The measured gate voltage pulse waveform is applied to the SPICE simulation of HiSIM by using a PWL (Piece-Wise Linear) waveform. Thus, numerical fluctuations in HiSIM results are due to the fluctuations of the input voltage. Fig. 11 compares measured $I_{\rm disp}$ with HiSIM results for switching pulses with $V_{\rm gsH}$ =1V and 0.5V. Good agreement of the calculated displacement currents both for $V_{\rm gsH}$ =1V and 0.5V proves the validity of Eq. (1) even for low voltage applications.

VII. Analysis of Low-Voltage Switching Performance

Fig. 5(b) provides information about the difference in carrier response under the low voltage operation. However, the displacement current is very much dependent on the waveform applied. To characterize the displacement current without the waveform influence, an ideal waveform is applied and compared with 2D-device simulation results in Figs. 12(a) and (b). Good agreements of the HiSIM results with those of 2D-device simulation proves the formulation of Eq. (1) is still

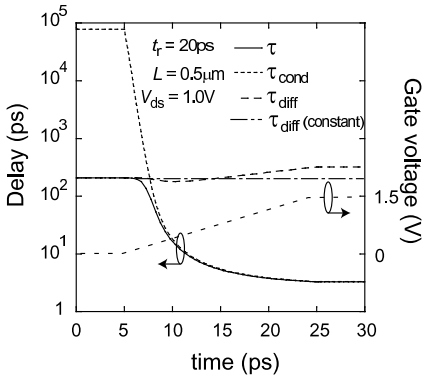

Fig. 8. Time-delay mechanisms as calculated for a 20ps switching time. $\tau_{\rm cond}$ describes the conduction delay which is the average time for the carriers to cross the channel once the channel is formed. $\tau_{\rm diff}$ describes the time delay due to diffusion of carriers. For efficient computer simulation time $\tau_{\rm diff}$ can be assumed as constant, as depicted by the straight line, since most of the delay is governed by $\tau_{\rm cond}$.

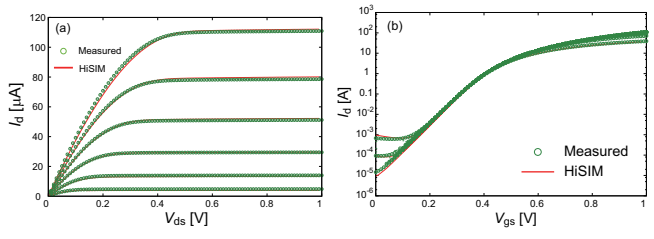

Fig. 9. $I_{\rm d}$-$V_{\rm ds}$ for $V_{\rm gs}$=0.5V to 1.0V by 0.1V steps, and $I_{\rm d}$-$V_{\rm gs}$ for $V_{\rm ds}$=0.1V to 1.0V by 0.1V steps.

valid. Fig. 12(a) with $V_{\rm gsH}$=1V shows similar characteristics as shown in Fig. 1, whereas Fig. 12(b) with $V_{\rm gsH}$=0.5V differs from the expectation. The reason can be explained by the transit delay time τ depicted in Fig. 8. The shorter τ leads to a constant $\frac{dQ}{dt}$ during the linearly increasing $V_{\rm gs}$ due to the also nearly linear function of the inversion charge as a function of $V_{\rm gs}$. However, the inversion charges required for the given $V_{\rm gs}$ value cannot be fulfilled within the switching period, and thus the charging continues even after reaching the DC condition resulting in the observed tail of $I_{\rm disp}$ during switching on. This degrades the switching speed of the MOSFET.

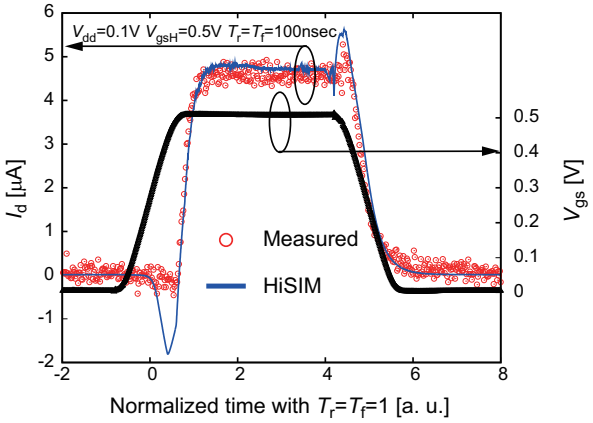

Fig. 10. Measured drain current $I_{\rm d}$ response (symbols) and HiSIM results (lines) with $V_{\rm gsH}$=0.5V and $V_{\rm dd}$=0.1V. The x-axis is normalized so that $T_{\rm r} = T_{\rm f} = 1$.

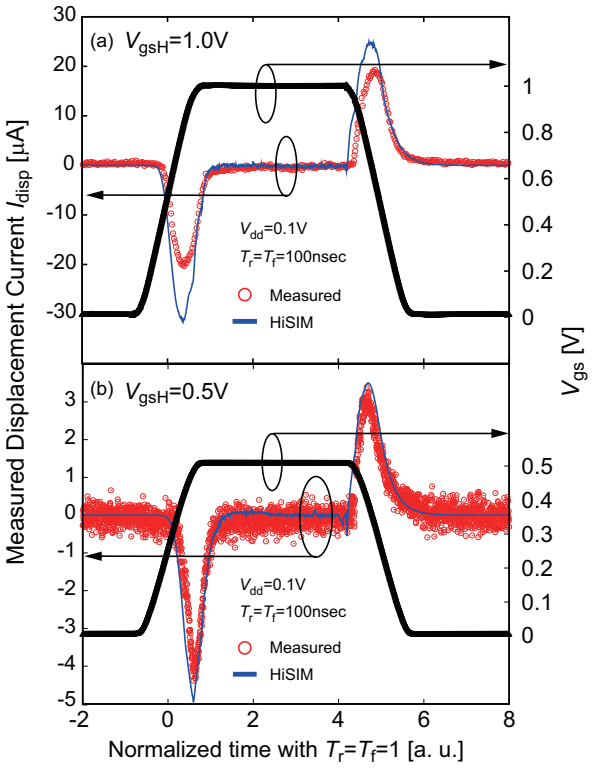

Fig. 11. Reproduction of measured displacement currents (symbols) with HiSIM results (lines) at $V_{\rm gsH}$ =1V (upper graph) and 0.5V (lower graph), respectively. $V_{\rm dd}$ =0.1V is chosen in both graphs. The dashed line shows the HiSIM result with carrier transit delay (NQS model).

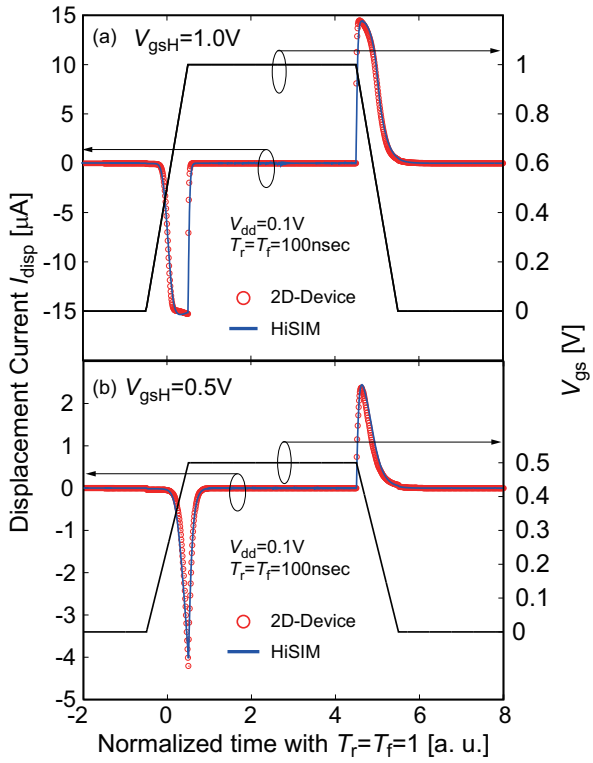

Fig. 12. Comparison of displacement current between the compact HiSIM model results and 2D-device-simulated results for $V_{\rm dd}$=0.1V. (a) $V_{\rm gsH}$=1V (b) $V_{\rm gsH}$=0.5V

VIII. Conclusion

We have investigated the transient response of the MOSFET for low voltage applications. It is found that the channel charging/discharging during switch-on/off at low voltages leads to an enhanced delay due to the lower driving capability. This characteristic can be still accurately modeled by considering the carrier transit delay.

References

[1] S.Y. Oh, D. Ward, and R. Dutton, *Transient Analysis of MOS Transistors*, IEEE Journal of Solid-State Circuits, SC-15, pp. 636-643, 1980.

[2] M. Miura-Mattausch, N. Sadachika, D. Navarro, G. Suzuki, Y. Takeda, M. Miyake, T. Warabino, Y. Mizukane, R. Inagaki, T. Ezaki, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, S. Kumashiro, and S. Miyamoto, *HiSIM2: Advanced MOSFET Model Valid for RF Circuit Simulation*, IEEE Trans. Electron Devices, vol. 53, no. 9, Sept., 1994-2007, 2006.

[3] M. Miura-Mattausch, H. J. Mattausch, T. Ezaki, *THE PHYSICS AND MODELING OF MOSFETS (Surface-Potential Model HiSIM)*, World Scientific Publishing, ISBN 978-981-256-864-9 (981-256-864-6), 2008.

[4] D. Navarro, Y. Takeda, M. Miyake, N. Nakayama, K. Machida, T. Ezaki, H. J. Mattausch, and M. Miura-Mattausch, *A Carrier-Transit-Delay-Based Nonquasi-Static MOSFET Model for Circuit Simulation and Its Application to Harmonic Distortion Analysis*, IEEE Trans. Electron Devices, vol. 53, no. 9, Sept., 2025-2034, 2006.