3-D Stress Simulation using Simple Quasi-Models of Gate Oxidation and Silicidation

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***Abstract*— We present 3-D stress simulation using simple quasi-models of gate oxidation and Silicidation. We show a good agreement between simulation and experiment about dependency of NMOSFET's saturation current (mobilities) on LOD (Local Oxidation Definition) and TWX (Trench Width of X-direction).**

Key words: 3-D stresss simulation, MOS transistor, Mobility, Oxidation, Silicidation, Piezo resistance model

I. INTRODUCTION

It is well known that stress in silicon strongly affects the electron/hole mobilities and threshold voltage of MOSFET. The control of stress such as stress liner films of nitride and stressor of SiGe makes it possible to improve the MOSFET performance [1]. On the other hand, the problem has occurred that MOSFET characteristics depends on not only channel length/width (L/W) but also the other nearby patterns like active region's length, and pitch of active region, gate and contact hole due to stress modification, which is recognized as the systematic variation.

3-D stress simulation is available to analyze the pattern dependence of MOSFET's characteristics systematically. Until now, there have been stress simulations of the dependence on the active region length [2-5] and distances between active regions. However, there is no good agreement report with actual data, because the previous analysis has not considered stress effects of gate oxidation and silicidation after filling in trench. The problems of these simulations can be caused by the difficulty of 3-D oxidation simulation and silicidation on a comparably wide region. Because the simulation of oxidation and silicidation for a wide region takes a long time to compute hard 3-D topography / meshing in visco-elastic model. Therefore, we propose simple quasi-models of oxidation and silicidation, which can be applied in the normal stress simulation. Using these proposed simple models, it is possible to calculate total steps for only 30 minutes with Intel Xeon (X5365 3.0 GHz). And then, we have succeeded in good agreement between experiment and simulation by the calibration of physical parameters such as intrinsic stress, Young's modulus of each material. In this work, we used 3-D process simulator (HySyProS) [6] and TiSSiEN-stress solver (TCADi's IP).

II. SIMPLE QUASI-MODELS OF GATE OXIDATION AND SILICIDATION

A. Stress effect of gate oxidation and quasi-oxide shape

We have simulated TWX-dependence of I/O-gate oxidation (about 8 nm) after filling in trench using the process simulator (HySyProS), and then its results are shown in Figs. 1 (a),(b) and (c), which mean 2-D topography, 2-D distribution of x-component (σ_{xx}) stress, and 1-D profiles of stress tensor components ($\sigma_{xx}, \sigma_{yy}, \sigma_{zz}$) 0.5nm below SiO_2/Si interface, respectively. Although the gate oxidation creates very thin oxide film, it causes strongly compressive stress in the corner of upper trench edge. Its stress peak value is about 1 GPa as shown in Figs. 1 (b) and (c). Then, it can be seen that compressive stress(σ_{xx}) of TWX=0.1μm is larger than that of TWX=0.03μm in Fig. 1(c). This reason is that the oxide film filled in trench becomes a relaxant of stress. If gate oxidation isn't considered, compressive stress (σ_{xx}) in silicon is increased as trench width of X-direction (TWX) becomes larger. Therefore it is possible to find which of gate oxidation or oxide film filled in trench is a dominant factor due to measured data . And then, it can be predicted that the final stress at the trench upper edge is more than 1 GPa since additionally there is a normal gate oxidation in the next process step.

We propose a quasi-gate oxide piece with an intrinsic stress instead of gate oxidation as shown in Fig. 2. Their oxide pieces have σ_{xx} and σ_{yy} as a constant intrinsic stress in the sides of yz and zx-interfaces, respectively. In this case, by considering above mentioned simulation of oxidation, width and height of the quasi-oxide pieces are set to 0.015μm and 0.03 μ m, respectively.

B. Quasi-silicidation shape

The physical parameters of silicide strongly affect the LOD-dependence of mobilities. We propose quasi-silicide shapes with an intrinsic stress, which are created on source/drain and the top of gate polysilicon, as shown in Fig.2. This silicide shapes are formed by using the functions of etching and deposition in the simulation.

III. EXPERIMENT AND SIMULATION

A. Procedure

We used the experimental data and TEG mask pattern in Fig. 3 of 65 nm process to calibrate several physical parameters such as intrinsic stress, Young's modulus and Poisson's ratio of materials. We have intrinsic stress values which are measured for all the used materials as references. In this calibration, we have used the piezo resistance model [7] to fit to the average of the measured mobility for 128 MOSFETs which is derived from saturation currents corresponding to various dynamic threshold voltages. An example of 3-D structure used for stress simulation and its result: x,y, and z-components (σ_{xx}, σ_{yy} and σ_{zz}) of stress tensor are shown in Fig. 4 and Fig. 5(a),(b) and (c), respectively. Figs. 5 show that the variation of σ_{xx} and σ_{yy} is large, and that of σ_{zz} is little. So, the variation of Tr.-characteristics is more affected by x/y-components (σ_{xx}/σ_{yy}) of stress than z-component (σ_{zz}). These stress simulation have been done in a quarter region of mask pattern in Fig. 3.

B. Discussion

Fig. 6 shows the calibrated result of 3-D stress simulation and the measured data, which is the graphs of dependence on LOD and TWX, of which horizontal axis is TWX. Basically, if the intrinsic compressive stress of quasi-oxide pieces becomes large, its graph shape becomes right side rise. Because oxide filled in trench is operated as the relaxation of stress. On the other hand, if the intrinsic stress of oxide filled in trench becomes large, its left side rises. The TWX-dependence (LOD=0.62, 1.3 μm) of the mobility for the NMOSFET in our measured data is a little right side rise as shown in Fig.6.

Therefore, it is found that the intrinsic stress of quasi-oxide pieces is more dominant than that of oxide filling in trench. And then, this intrinsic stress of quasi-oxide pieces need to be very large (~3 GPa), and it is reasonable for the mobility variation from the Piezo resistance model. We can see good agreement between simulations and measured data in Fig. 6.

IV. CONCLUSION

We propose a simple quasi-model instead of 3-D numerical simulations of gate oxidation and silicidation for the stress simulation in MOSFET channel region. It can be seen that our simulation agrees very well with measured data about the LOD/TWX-dependency of NMOSFET mobility, and then it is found that the stress induced by gate oxidation is dominant on stress variation of the channel region for our process..

ACKNOWLEDGEMENT

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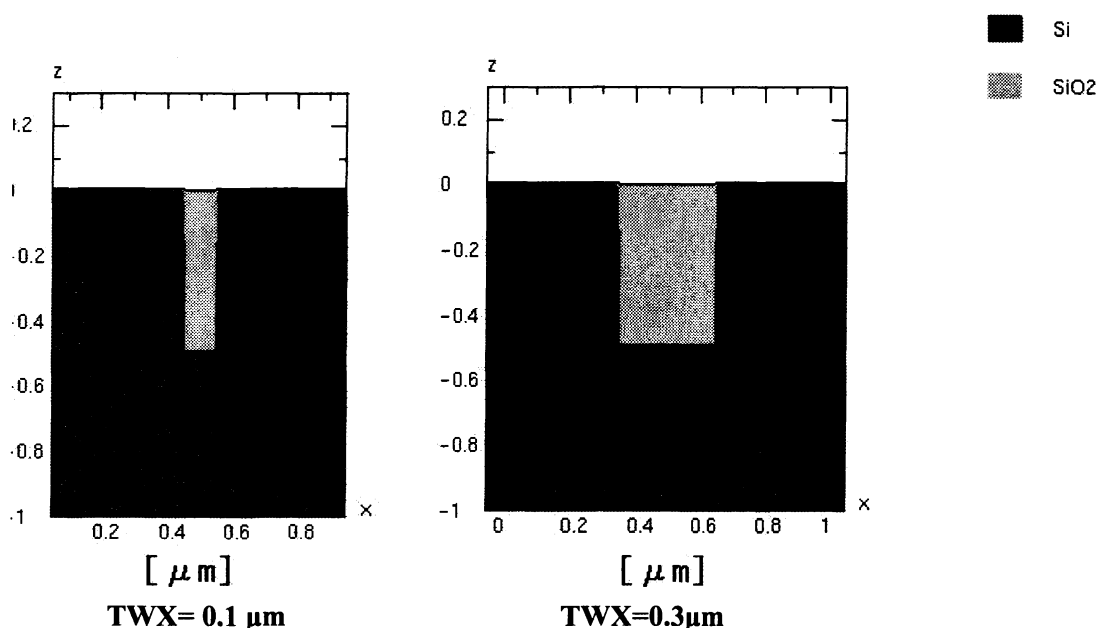
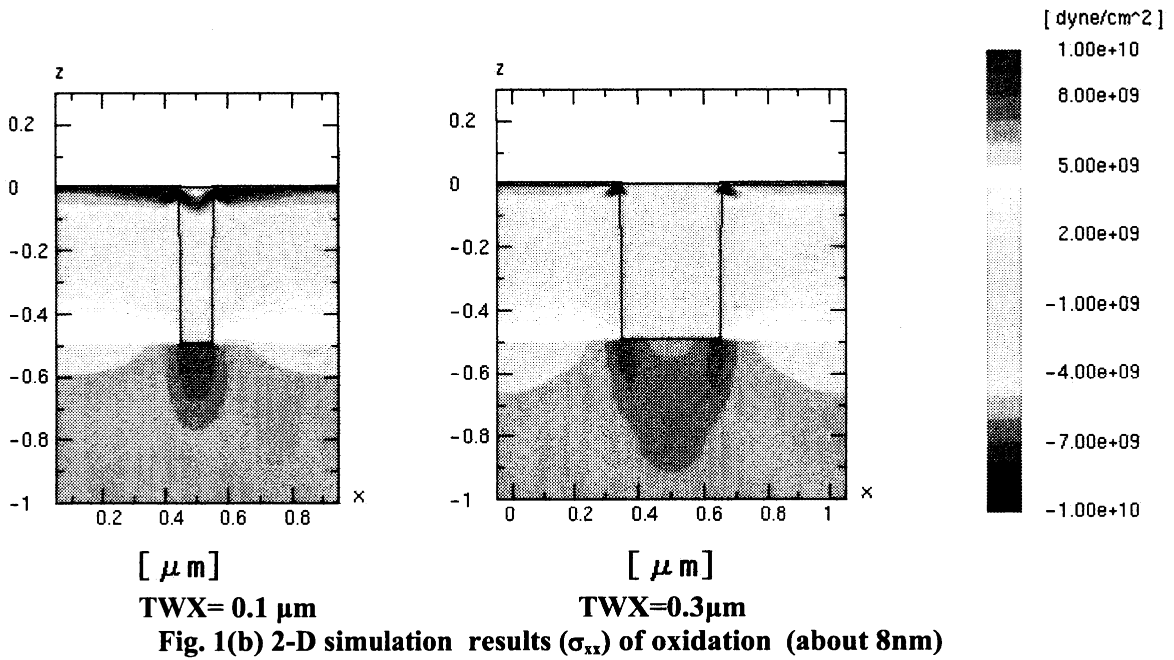
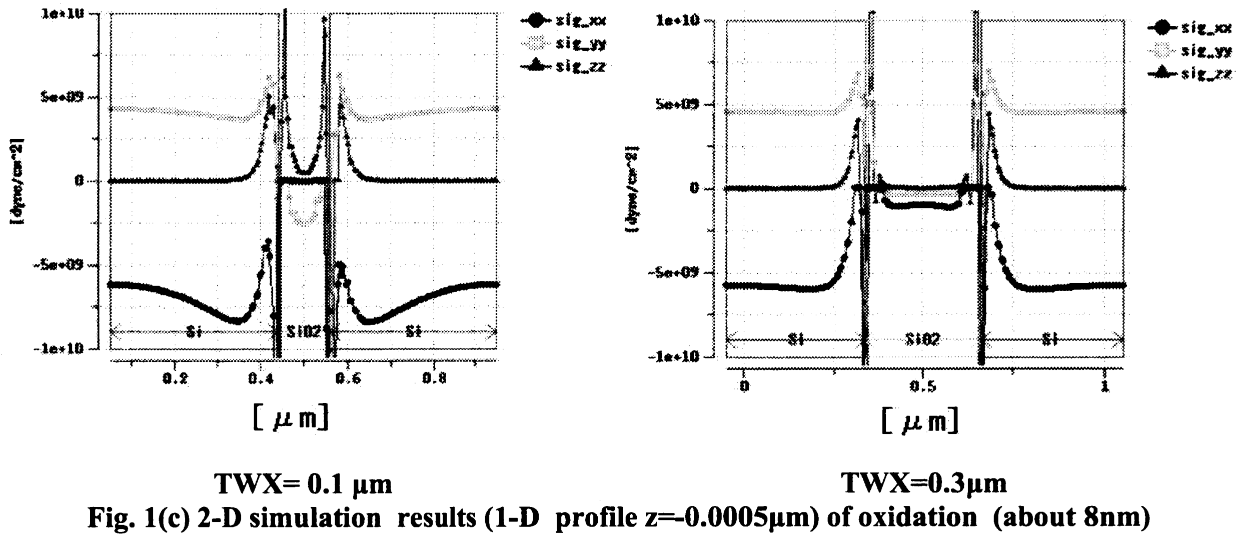


Fig. 1(a) 2-D simulation results (topography) of oxidation (about 8nm)



TWX= 0.1 μm TWX=0.3μm

Fig. 1(b) 2-D simulation results (σ_{xx}) of oxidation (about 8nm)



TWX= 0.1 μm TWX=0.3μm

Fig. 1(c) 2-D simulation results (1-D profile z=-0.0005μm) of oxidation (about 8nm)

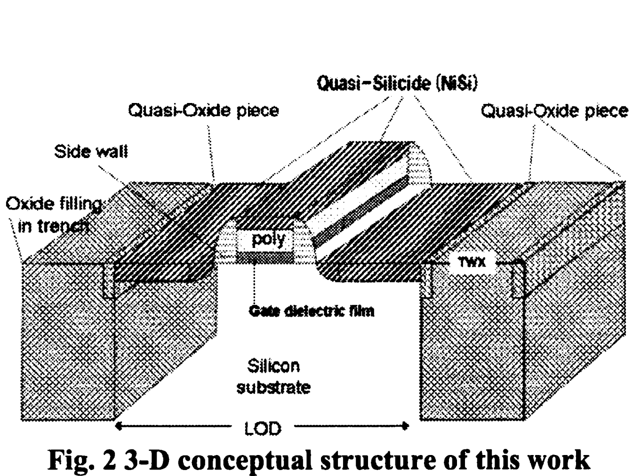


Fig. 2 3-D conceptual structure of this work

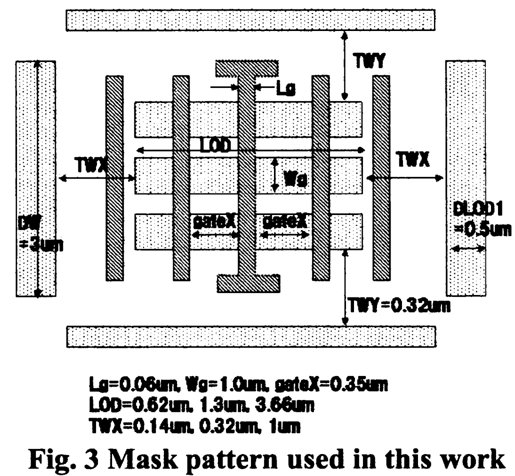


Fig. 3 Mask pattern used in this work

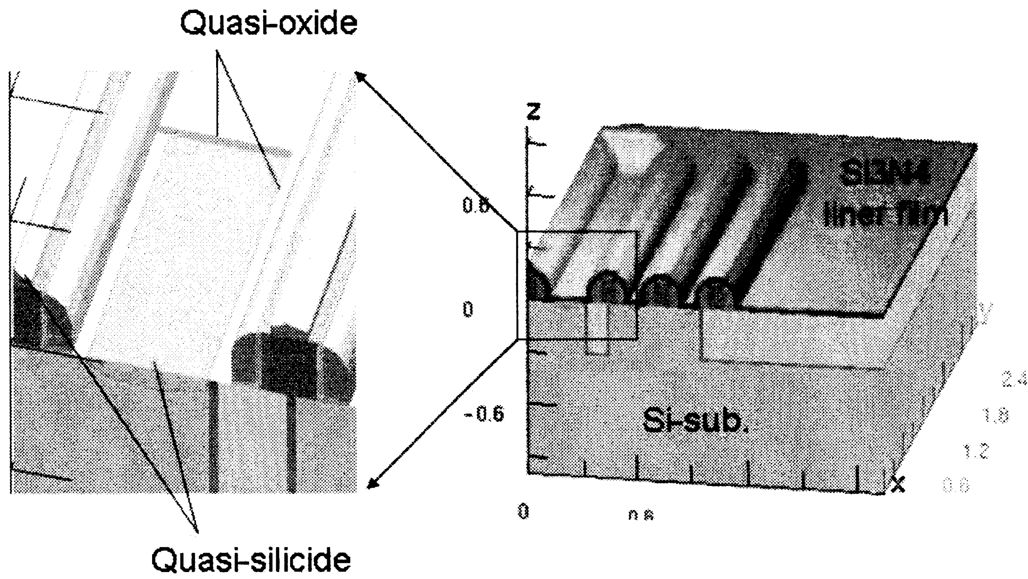


Fig. 4 An example of 3-D structure

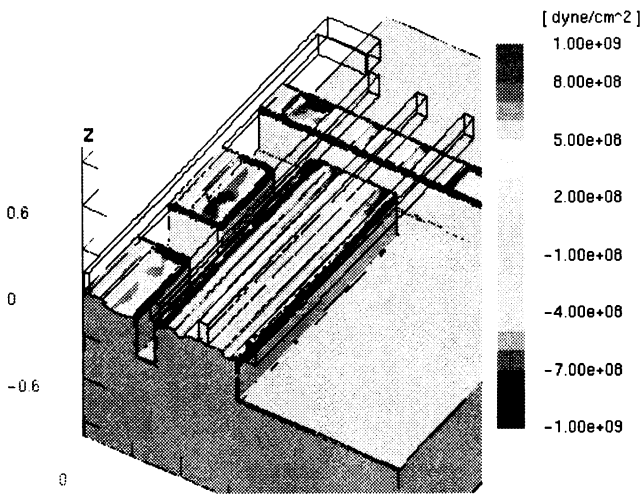


Fig. 5(a) 3-D stress simulation result σ_{xx}

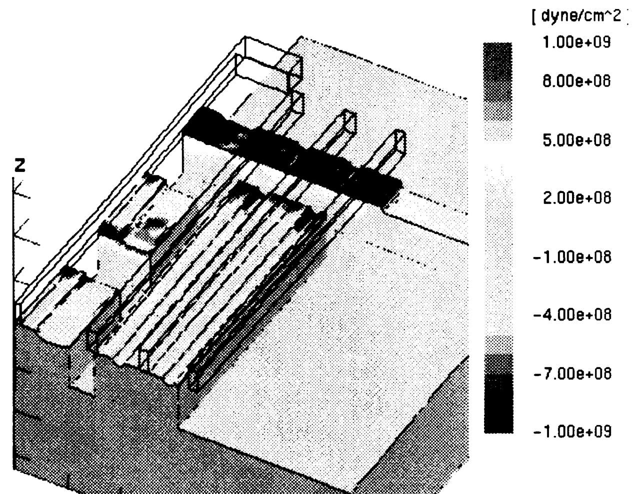


Fig. 5(b) 3-D stress simulation result: σ_{yy}

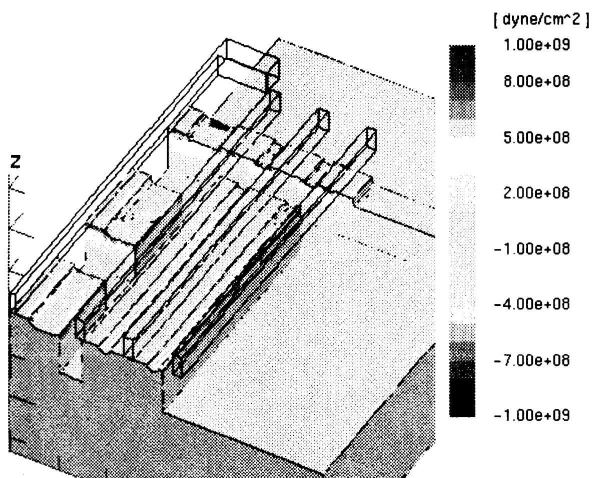


Fig. 5(c) 3-D stress simulation result σ_{zz}

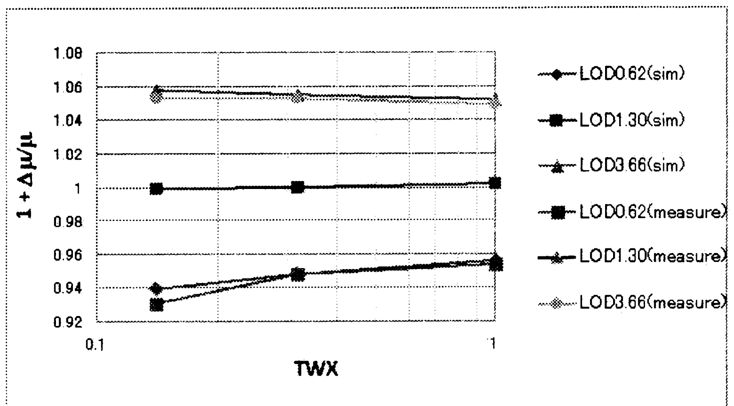


Fig. 6 3-D stress simulation (Calibrated result) and measured data