Reduction of Discrete-Dopant-Induced High-Frequency Characteristic Fluctuations in Nanoscale CMOS Circuit

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***Abstract*—As the dimension of semiconductor device shrunk into nanoscale, characteristic fluctuation is more pronounced, and become crucial for circuit design. Diverse approaches have been reported to investigate and suppress the random-dopant-induced fluctuations in devices. However, attention is seldom drawn to the existence of high-frequency characteristic fluctuations of active device. In this paper, intrinsic high-frequency characteristic fluctuations of the nanoscale MOSFET circuit induced by random dopants are intensively explored using an experimentally validated simulation methodology, where fluctuation suppression technique is further examined. The circuit gain, the 3db bandwidth and the unity-gain bandwidth of the tested circuit are estimated concurrently capturing the discrete-dopant-number- and discrete-dopant-position-induced fluctuations. This study provides an insight into discrete-dopant-induced intrinsic high-frequency characteristic fluctuations and examines the potential fluctuation suppression technique for nanoscale transistor circuit.**

Keywords-Random dopant, Fluctuation, Nanoscale MOSFETs, High Frequency Property, Suppression, Modeling and Simulation.

I. INTRODUCTION

Silicon-based devices are scaled down continually in order to increase density and speed. The gate lengths of scaled metal-oxide-semiconductor field effect transistors (MOSFETs) have been the sub-30 nm for 45 nm node high-performance circuit design. Yield analysis and optimization, which take into account the manufacturing tolerances, model uncertainties, variations in the process parameters, etc., are known as indispensable components of the circuit design methodology [1-8]. However, attention is seldom drawn to the existence of high-frequency characteristic fluctuations of active device due to random-dopant placement. With device scaling, various randomness effects resulting from the random nature of manufacturing process, such as ion implantation, diffusion and thermal annealing, have induced significant fluctuations of electrical characteristics in nanometer scale (nanoscale) MOSFETs. The number of dopants is of the order of tens in the depletion region of a nanoscale MOSFET, whose influence on device characteristic is large enough to be distinct. Various studies have recently been reported to examine fluctuation-related issues in semiconductor devices and circuit [1-8]. Unfortunately, the effect of the discrete-dopants-induced high-frequency characteristic fluctuations on nanoscale MOSFET circuits has not been well investigated yet.

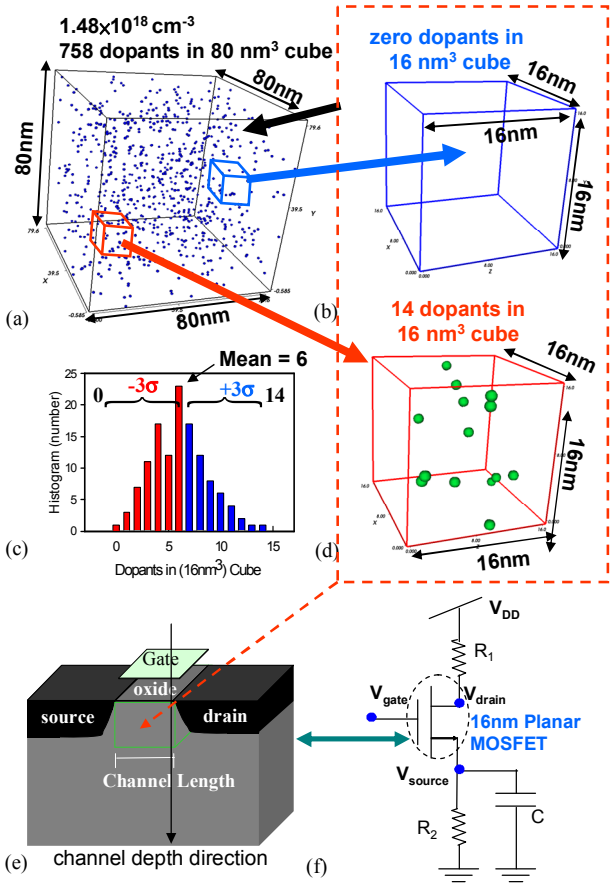

Figure 1. Discrete dopants randomly distributed in the 80 nm^3 cube with the average concentration of $1.48x10^{18}$ cm^{-3}. There will be 758 dopants within the cube, but dopants may vary from zero to 14 (the average number is six) within its 125 sub cubes of 16 nm^3, [(b), (c), and (d)]. The 125 sub cubes are equivalently mapped into channel region for dopant position/number- sensitive device simulation and device/circuit coupled simulation as shown in (e) and (f).

In this work, we study the discrete-dopant-induced high-frequency characteristic fluctuations of utilizing mixed-mode simulation, concurrently capturing "dopant concentration variation" and "dopant position fluctuation" in an explored

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nanoscale MOSFET circuit. Based on statistically (totally random) generated large-scale doping profiles, a three-dimensional (3D) device simulation is performed by solving a drift-diffusion model with quantum corrections by the density gradient equations on our parallel computing system [10]. This approach allows us to examine physical insight of the high-frequency characteristic fluctuation of the examined nanoscale MOSFET circuit, in contrast to SPICE circuit simulation. The accuracy of analyzing technique was quantitatively verified in the experimentally measured characteristics of sub-20 nm devices [2]. Channel engineering technique has been known to be an effective way to suppress the random-dopant-induced characteristic fluctuation [8-9]. To examine the fluctuation suppression on the high-frequency characteristic fluctuations of the explored nanoscale MOSFET circuit, an improved vertical doping profile along the longitudinal diffusion direction from the device's channel surface to the substrate is further implemented. We thus calculate the fluctuations of the circuit gain, the 3db bandwidth, and the unity-gain bandwidth of the tested circuit, and compare with the results before the improvement. Our comprehensive results show that the number of discrete dopants, varying from zero to 14, in the 16 nm MOSFET circuit, may result in 5.7% variation of the circuit gain, 14.1% variation of the 3db bandwidth, and 10.4% variation of the unity-gain bandwidth. For the aforementioned doping profile with less dopants locating near surface of channel, the fluctuations of the threshold voltage, the circuit gain, the 3db bandwidth, and the unity-gain bandwidth are 14.2%, 32.3%, 19.4%, and 51.8% reductions, simultaneously.

This paper is organized as follows. Sec. II shows the computational model for the random dopant-induced threshold voltage fluctuations. Sec. III presents the results and discussion. Finally, we draw the conclusions.

II. Simulation Technique

The nominal channel doping concentration of the device is $1.48\text{x}10^{18}$ cm^{-3}. Outside the channel, the doping concentrations in the source/drain and background are $1.1\text{x}10^{20}$ cm^{-3} and $1\text{x}10^{15}$ cm^{-3}, respectively. For the channel region, to consider the random fluctuation effect of the number and location of discrete channel dopants, 758 dopants are randomly generated in an 80 nm^3 cube, in which the equivalent doping concentration is $1.48\text{x}10^{18}$ cm^{-3}, as shown in Fig. 1(a). The 80 nm^3 cube is then partitioned into 125 sub-cubes of 16 nm^3. The number of dopants may vary from zero to 14, and the average number is six, as shown in Figs. 1(b), 1(c), and 1(d), respectively. These 125 sub-cubes are equivalently mapped into the device channel for the 3D device simulation with discrete dopants, as shown in Figs. 1(e). The source-follower circuit is considered as a tested circuit to explore the fluctuation of high-frequency characteristics. All statistically generated discrete dopants, shown in Fig. 1, are incorporated into the large-scale 3D device/circuit mixed-mode simulation which is performed in our parallel computing system [10]. The 3D device simulation is performed by solving density-gradient equation coupling with Poisson equation as well as electron-hole current continuity equations. There is no well-established device compact model for describing the discrete-dopant-fluctuated gate capacitance of such ultrasmall nanoscale

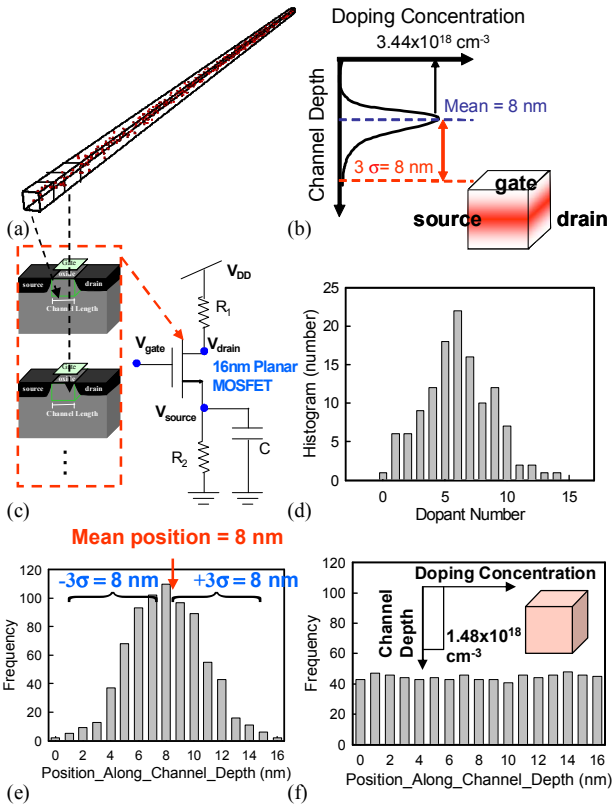

Figure 2. There will be 758 dopants are within a large rectangular solid, in which the equivalent doping concentration is $1.48\text{x}10^{18}$ cm^{-3}. The dopant distribution in the direction of channel depth, the arrow line in Fig. 1(e), follows the normal distribution (b). The partitioned cubes are equivalently mapped into channel region for dopant position/number-sensitive simulation, as shown in (c). Similarly, dopants within the 16 nm^3 cubes may vary from zero to 14 (the average number is six) (d). The vertical dopant distribution of the improved and the original doping profile, which is generated from Fig. 1, are shown in (e) and (f).

devices [1], so circuit simulation is directly coupling with the aforementioned 3D device simulation, where the circuit nodal equations of the tested circuit are formulated using the current and voltage conservation laws.

To examine the effectiveness of the channel engineering technique in both nanoscale device and circuit, along the longitudinal diffusion direction from surface to substrate, an improved vertical doping profile with less dopants locating near surface of channel [8,9] is further implemented. Similarly, 758 dopants are firstly randomly generated in a large rectangular solid, in which the equivalent doping concentration is $1.48\text{x}10^{18}$ cm^{-3}, as shown in Fig. 2(a). The statistically generated dopant distribution in the direction of channel depth, the arrow line in Fig. 1(e), follows the normal distribution, as shown in Fig. 2(b). Both the mean position and the three sigma of this distribution are eight nanometers, which can be controlled by the manufacturing processes of ion implementation and thermal annealing. The inset of Fig. 2(b) shows the nominal case of the improved vertical doping profile, where the darker region indicates the higher doping concentration. The large rectangular solid is then partitioned into 125 sub-cubes of 16 nm^3 cube and mapped into device

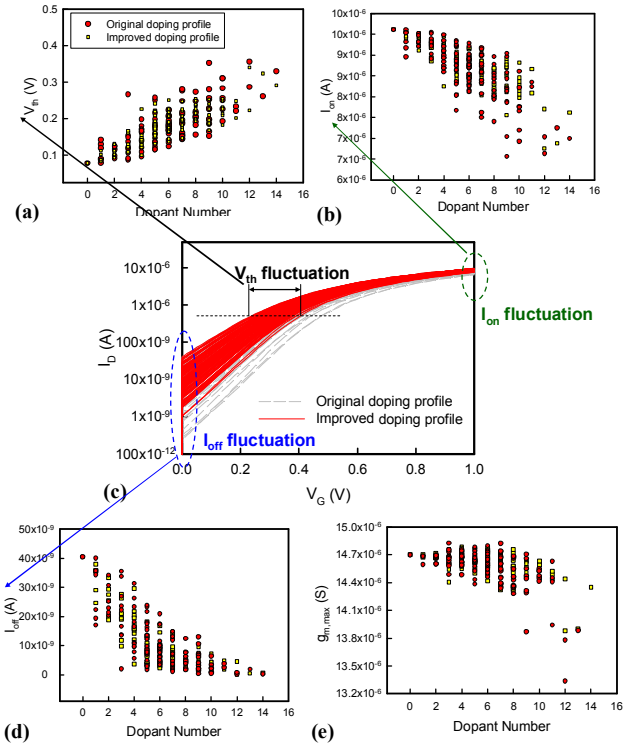

Figure 3. DC characteristic fluctuations of the 250 discrete dopant fluctuated 16-nm-gate planar MOSFET from the original and the improved doping profile. The studied fluctuations of (a) threshold voltage (V_{th}), (b) on-state current (I_{on}), (c) I_D-V_G curves, (d) off-state current (I_{off}), (e) and maximum transconductance ($g_{m,max}$).

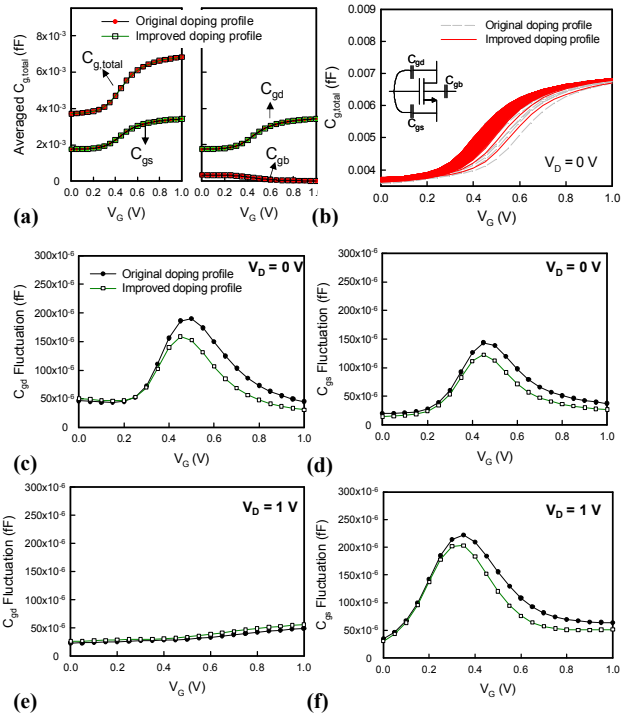

Figure 4. (a) The averaged gate capacitance of the studied devices. ($C_{g,total}$ = C_{gd} + C_{gs}+ C_{gb}). (b) The C-V characteristics of the discrete dopant fluctuated devices generated from the original (dashed lines) and the improved (solid lines) doping profiles. (c)(d) Fluctuation of C_{gd} and C_{gs} with V_D = 0 V. (e)(f) Fluctuation of C_{gd} and C_{gs} with V_D = 1 V.

channel for discrete dopant and device/circuit coupled mixed-mode simulation, as shown in Fig. 2(c). Similarly, the number of dopants may vary from zero to 14, and the average number is six, as shown in Fig. 2(d). The longitudinal dopant distribution of the improved and the original doping profile, which is generated from Fig. 1, are studied in Figs. 2(e) and 2(f), respectively. The inset of Fig. 2(f) shows the distribution of doping concentration for the original doping profile. We notice that the threshold voltages of the nominal devices for both the improved and original doping profiles, whose channel doping profile is continuously doped with $1.48\text{x}10^{18}$ cm^{-3}, are adjusted to be the same value 140 mV. Result shows that numbers of dopant appearing near the channel surface for the improved doping profile is significant less than that of the original doping profile, and thus may induce less surface potential fluctuation than the other.

III. Results and Discussion

Figure 3 shows the comparison of DC characteristic fluctuations for the original and the improved doping profile. The spreading range of the I_D-V_G curves, as shown in Fig. 3(c), illustrates the magnitude of fluctuations. The reduced spreading range of the improved doping profile indicates a suppression of fluctuation on DC characteristic of device. The fluctuation of the threshold voltage (V_{th}), on-state current (I_{on}), off-state current (I_{off}), and maximum transconductance ($g_{m,max}$) are shown in Figs. 3(a), 3(b), 3(d), and 3(e), respectively. As expected, the fluctuation of V_{th}, I_{on}, $g_{m,max}$ are effectively suppressed due to the less dopant locating near the channel surface. However, the suppression of Ioff fluctuation is not significant due to the similar numbers of dopant locating near the path of leakage current (about 4 nm below the gate oxide). This result implies the importance of the vertical doping profile design.

Figure 4(a) shows the averaged gate capacitances of the 250 discrete dopant fluctuated 16-nm-gate planar MOSFET. The total gate capacitance ($C_{g,total}$), is composed of gate-drain capacitance (C_{gd}), gate-source capacitance (C_{gs}), and gate-bulk capacitance (C_{gb}), and the shape and the value of the averaged C-V curves for the two doping profiles are quite similar. Figure 4(b) shows the C-V characteristics of the discrete dopant fluctuated device generated from the original (dashed lines) and the improved (solid lines) doping profiles. Although the averaged C-V curves of the two doping profiles are similar, the devices from improved doping profile show a more condensed distribution thus a smaller capacitance fluctuation than the others. The fluctuations of C_{gd} and C_{gs} are then studied in Figs. 4(c)-4(f). The capacitance fluctuation can be reduced effectively by optimization of doping profile. At drain voltage of 0 V, the fluctuation of $C_{g,total}$ are mainly contributed from C_{gd} and C_{gs} fluctuation. The fluctuations of C_{gd} and C_{gs} are similar, as displayed in Figs. 4(c) and 4(d). On the other hand, at drain voltage of 1 V, the fluctuation of gate capacitance is dominated by C_{gs}, as shown in Figs. 4(e) and 4(f). Figure 5(a) shows the circuit gain versus operation frequency for all

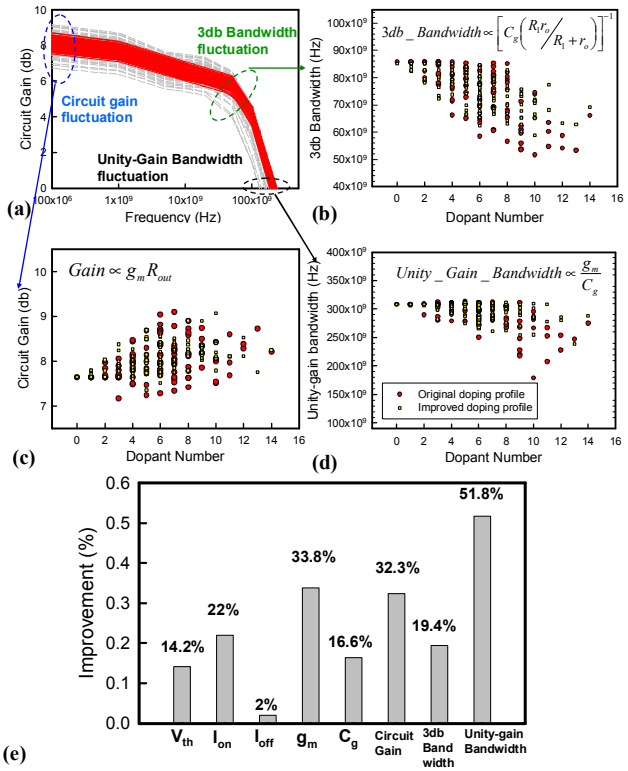

Figure 5. (a) High-frequency characteristic fluctuations for the original and the improved doping profile. The studied fluctuations of (b) circuit gain, (c) 3db bandwidth, (d) and unity-gain bandwidth. (e) Summary of the effectiveness of fluctuation suppression technique in both the nanoscale device and circuit.

fluctuated cases. The circuit gain, 3db bandwidth, and unity-gain bandwidth of the fluctuated cases are then explored in Figs. 5(b)-5(d), where the insets show the circuit gain, 3db bandwidth, and unity-gain bandwidth as a function of device characteristic and circuit element. The cases from the improved doping profile are less scattered than that from the original doping profile. The effectiveness of fluctuation suppression technique in nanoscale device and circuit is summarized in Fig. 5(e). The fluctuation suppressions of the characteristics of the nanoscale device circuit are more pronounced than that of device due to the second-order nonlinear effect of circuit characteristics.

IV. Conclusions

In this study, intrinsic DC and high-frequency characteristic fluctuations of 16-nm-gate N-MOSFET inverter circuit, induced by random dopants, have for the first time been explored intensively by using a 3D mix-mode simulation technique. The effectiveness of fluctuation suppression technique was discussed. The discrete-dopant fluctuated 16-nm-gate N-MOSFET inverter circuit exhibits 5.7% variation of the circuit gain, 14.1% variation of the 3db bandwidth and 10.4% variation of the unity-gain bandwidth. For the device with considering the suggested doping profile, the fluctuations of the threshold voltage, the circuit gain, the 3db bandwidth, and the unity-gain bandwidth are simultaneously reduced by 14.2%, 32.3%, 19.4%, and 51.8%, respectively. The fluctuation suppression of the high frequency characteristics is mainly resulted from less fluctuations of DC characteristic and gate capacitance of the 16-nm-gate N-MOSFET by introducing the doping profile with the normal distribution along the longitudinal direction from the channel surface to substrate. The examined vertical doping distribution with less dopants locating near surface of channel reduces the fluctuation of surface potential effectively and thus suppresses the DC and high-frequency characteristics' fluctuations. The result of this study provides an insight into random-dopant-induced intrinsic high-frequency characteristic fluctuations also preliminarily confirms the effectiveness of the channel engineering on suppression of high-frequency characteristic fluctuation of the explored nanoscale device circuit.

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