Analysis and Modeling of Capacitance-Voltage Characteristics of Poly-Si TFTs using Device Simulation

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***Abstract*—The $C-V$ characteristics of short-channel poly-Si thin-film transistors containing only a single grain boundary (GB) were investigated using a two-dimensional device simulator. It was found that the GB can cause differences in the characteristics of the gate-to-source and gate-to-drain capacitances as a function of the gate voltage, even if no bias is applied between the source and drain. A new equivalent circuit model is proposed to explain the differences in the characteristics due to the GB.**

I. Introduction

In recent years, poly-Si thin-film transistors (TFTs) have received a great deal of attention as attractive devices for system-on-panel applications. For such purposes, short-channel poly-Si TFTs with high performance are urgently required. It is well-known that poly-Si grain boundary (GB) traps in the channel region influence both the current-voltage ($I-V$) and capacitance-voltage ($C-V$) characteristics of the TFT [1], and that, compared to long-channel TFTs, short-channel TFTs are more sensitive to variation of the number and position of GBs, because fewer GBs are present in their channel regions. Although several studies have been performed so far on the $I-V$ characteristics, demonstrating that the GB variation strongly affects the threshold voltage [2] and on-current [3], there have been few studies on the $C-V$ characteristics.

In this study, the $C-V$ characteristics of short-channel poly-Si TFTs containing only a single GB are investigated using a two-dimensional device simulator. As a result, it is found that the GB can cause differences in the characteristics of the gate-to-source (C_{gs}) and the gate-to-drain (C_{gd}) capacitances as a function of the gate voltage (V_g), even if no bias is applied between the source and drain. From these findings, a new equivalent circuit model is developed to explain the differences in the characteristics due to the GB.

II. SIMULATION METHOD

Figure 1 shows schematic structures of the n-channel TFTs simulated in this study. The channel length is 1 μm. The thicknesses of the gate-oxide and Si layer are 30 nm and 50 nm, respectively. The TFTs contain only a single GB in the channel region, which was placed either (a) at the center of the channel or (b) 250 nm from the drain. The GB was set to be perpendicular to the Si/SiO$_2$ interface and its width is 5 nm.

Both donor-like ($g_D(E)$) and acceptor-like ($g_A(E)$) trap states at the GB were taken into account, as shown in Fig. 2. Both of the trap states are approximated by the sum of the exponential distribution of the tail states and the Gaussian shaped distribution of the mid-gap states [3] as

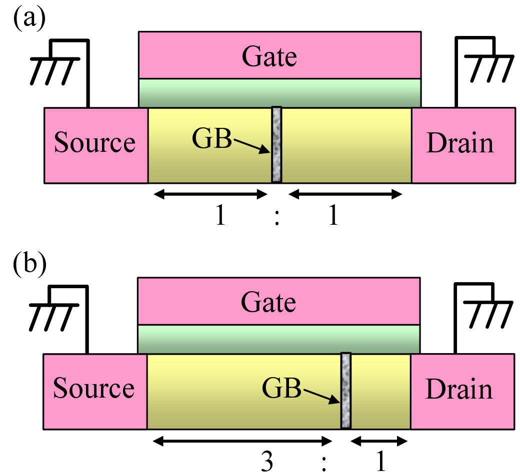

Fig. 1. Schematic view of the TFT structures simulated in this study. The channel length is 1 μm. A grain boundary (GB) was placed either (a) at the center of the channel or (b) 250 nm from the drain.

$$g_D(E) = g_{TD}(E) + g_{GD}(E) \quad (1)$$
$$g_A(E) = g_{TA}(E) + g_{GA}(E) \quad (2)$$

where the subscripts (T, G, D, A) represent tail, Gaussian, donor, and acceptor states, respectively. The expressions of these terms are given as

$$g_{TD}(E) = N_{TD} \exp\left(\frac{E_v - E}{W_{TD}}\right) \quad (3)$$
$$g_{TA}(E) = N_{TA} \exp\left(\frac{E - E_c}{W_{TA}}\right) \quad (4)$$
$$g_{GD}(E) = N_{GD} \exp\left[-\left(\frac{E - E_{GD}}{W_{GD}}\right)^2\right] \quad (5)$$
$$g_{GA}(E) = N_{GA} \exp\left[-\left(\frac{E_{GA} - E}{W_{GA}}\right)^2\right] \quad (6)$$

where E_c is the conduction band energy, and E_v is the valence band energy. The other symbols are defined in Table I.

The C_{gs}-V_g and C_{gd}-V_g characteristics of the TFTs were

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analyzed using the two-dimensional device simulator, ATLAS [4], at a frequency of 1 MHz.

III. Simulation Results and Discussion

Figure 3 shows the simulated C_{gs}-V_g and C_{gd}-V_g characteristics for the TFTs. For reference, that without a GB is also presented. As shown in Fig. 3(a), when the GB is at the center of the channel, C_{gs} and C_{gd} have the same dependence on V_g, because of the symmetric structure about the center of the channel, as well as the case without the GB. However, when the GB is at the drain side, C_{gs} and C_{gd} show different dependency on V_g, as shown in Fig. 3(b). Note that no bias is applied between the source and drain in the simulations. While C_{gd} gradually increases with V_g, C_{gs} rapidly increases until V_g = 0.8 V, then decreases. In addition, as V_g increases further, C_{gs} and C_{gd} asymptotically approach the same value as that calculated without the GB.

In order to elucidate the mechanism behind this phenomenon, the internal physical quantities (electron density distribution, potential) were analyzed in the TFTs. Figure 4 shows the simulated electron concentration close to the Si/SiO_2 interface along the channel direction. Note that the inversion layer is divided into two parts, that is, the source side and the drain side, at the position of the GB. This is due to the potential barrier (ϕ_B) of the GB. When the GB is at the center of the channel (Fig. 4(a)), the inversion layer is divided symmetrically into the source and drain sides. On the other hand, when the GB is at the drain side (Fig. 4(b)), the inversion layer is divided asymmetrically, which explains the differences in the characteristics of C_{gs} and C_{gd} shown in Fig. 3(b). Furthermore, as shown in Fig. 5, ϕ_B decreases as V_g increases from 0.8 to 5 V, due to the screening effect [5], which leads to the asymptotic behavior of C_{gs} and C_{gd} with increasing V_g.

TABLE I
Trap parameters used in the simulations.

Trap parameters	Value
Density of donor-like tail states N_{TD} ($cm^{-3}eV^{-1}$)	4×10^{19}
Density of acceptor-like tail states N_{TA} ($cm^{-3}eV^{-1}$)	1×10^{20}
Density of donor-like Gaussian states N_{GD} ($cm^{-3}eV^{-1}$)	5×10^{18}
Density of acceptor-like Gaussian states N_{GA} ($cm^{-3}eV^{-1}$)	5×10^{18}
Decay energy for donor-like tail states W_{TD} (eV)	0.05
Decay energy for acceptor-like tail states W_{TA} (eV)	0.05
Decay energy for donor-like Gaussian W_{GD} (eV)	0.1
Decay energy for acceptor-like Gaussian W_{GA} (eV)	0.1
Energy of Gaussian for donor-like states E_{GD} (eV)	E_v + 0.51
Energy of Gaussian for acceptor-like states E_{GA} (eV)	E_c – 0.51

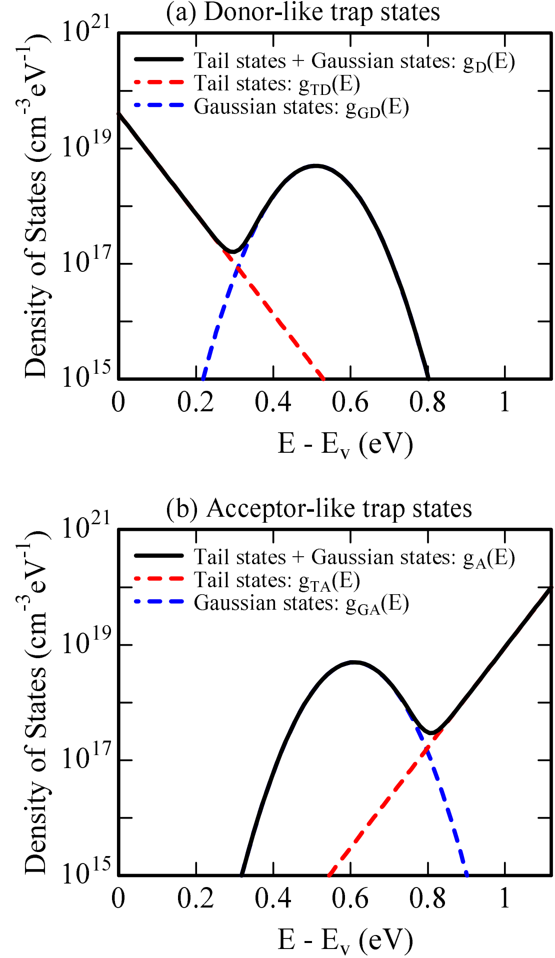

Fig. 2. Distribution of (a) donor-like trap states ($g_D(E)$) and (b) acceptor-like trap states ($g_A(E)$) at the GB used in this study. Both of the trap states are approximated by the sum of the exponential distribution of the tail states and the Gaussian shaped distribution of the mid-gap states.

IV. Equivalent Circuit Model

Based on the mechanism described above, a new equivalent circuit model was developed to explain the differences in the C_{gs} and C_{gd} characteristics. The influence of ϕ_B was incorporated into the channel resistance R_{ch} as

$$R_{ch} \propto \exp\left(\frac{q\phi_B}{kT}\right) \quad (7)$$

where q is the electron charge, k is the Boltzmann constant, and T is the absolute temperature. This means that a higher potential barrier of the GB results in a higher channel resistance. ϕ_B is given as a function of the channel electron density (N) [5,6]. Rather than use the piecewise model [5], a new model was developed to describe ϕ_B for all the range of N values using the unified equation as

$$1/\phi_B = aN^{-0.35} + b + cN \quad (8)$$

where a, b, and c are fitting parameters. Figure 6 shows a comparison of ϕ_B calculated using the device simulation and Eq. (8), which indicates a good agreement.

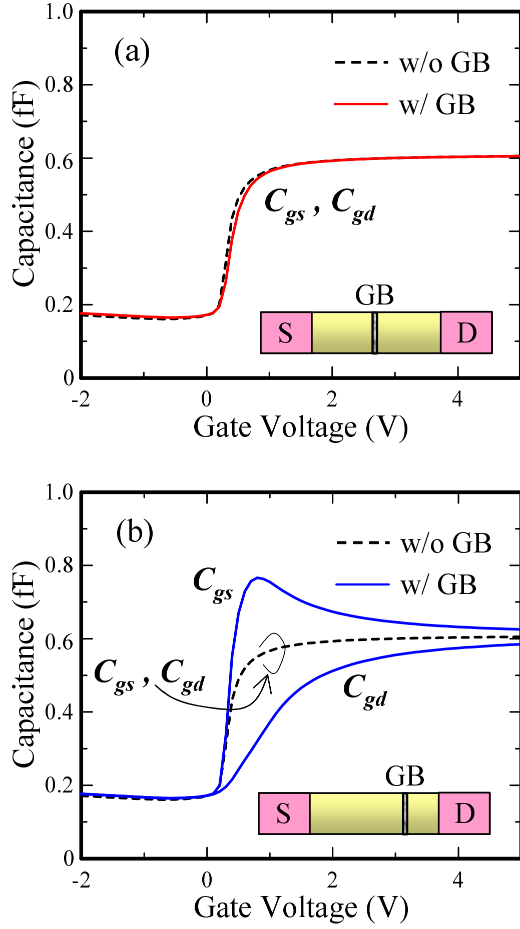

Fig. 3. Simulated capacitance-voltage ($C-V$) characteristics at 1 MHz for the TFTs when the GB is (a) at the center of the channel or (b) at the drain side. For reference, simulated $C-V$ characteristics without the GB are also presented (dashed line). No bias is applied between the source and drain.

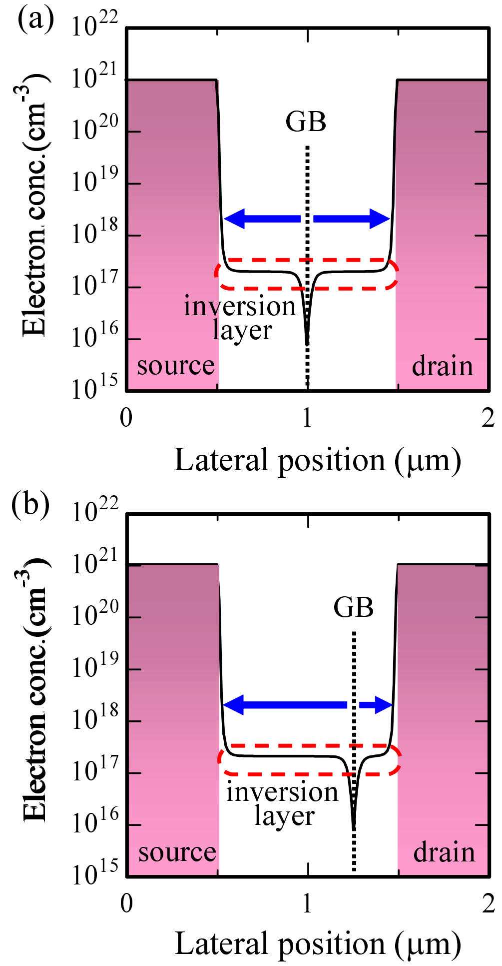

Fig. 4. Simulated electron concentration close to the Si/SiO_2 interface along the channel direction when the GB is (a) at the center of the channel or (b) at the drain side. In the simulations, V_g=0.8 V was used. The inversion layer is divided into two regions by the GB.

C_{gs} and C_{gd} are calculated from the following equations derived from the new equivalent circuit model shown in Fig. 7 as

$$C_{gs} = \frac{1-\alpha}{2}C + \frac{\alpha\left(1/R_{ch1}+1/R_{ch2}\right)C}{R_{ch1}\left[\left(1/R_{ch1}+1/R_{ch2}\right)^2+\left(\alpha\omega C\right)^2\right]} \quad (9)$$

$$C_{gd} = \frac{1-\alpha}{2}C + \frac{\alpha\left(1/R_{ch1}+1/R_{ch2}\right)C}{R_{ch2}\left[\left(1/R_{ch1}+1/R_{ch2}\right)^2+\left(\alpha\omega C\right)^2\right]} \quad (10)$$

where C is the total oxide capacitance, ω is the angular frequency, and α is a fraction factor with a value between 0 and 1. In the following calculations, α=0.5 was used for simplicity.

Figure 8 shows the capacitances calculated using Eqs. (9) and (10) as a function of the channel electron density

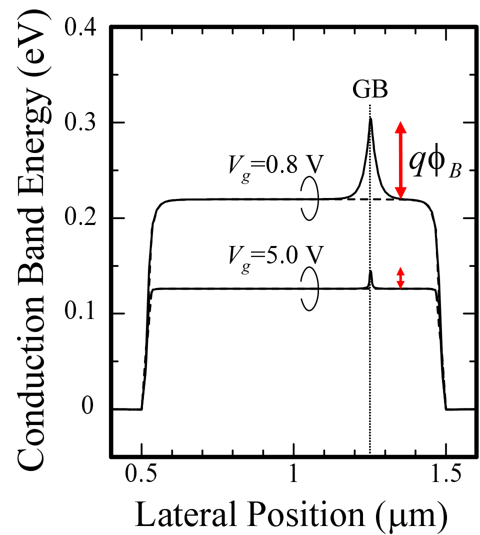

Fig. 5. Simulated conduction band energy close to the Si/SiO_2 interface when the GB is at the drain side. ϕ_B represents the potential barrier due to the GB.

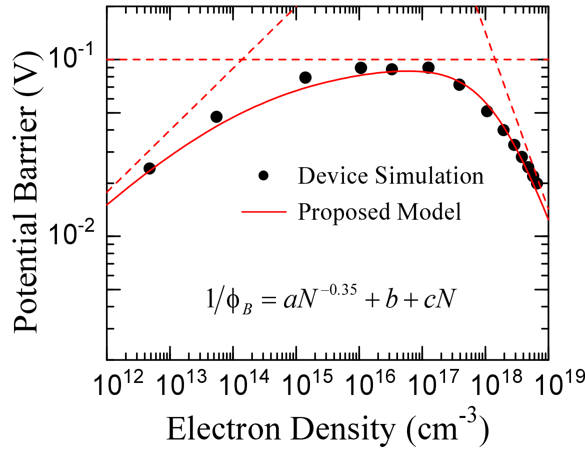

Fig. 6. Comparison of the calculated potential barrier due to the GB obtained using the device simulation (symbol) and the proposed model (line).

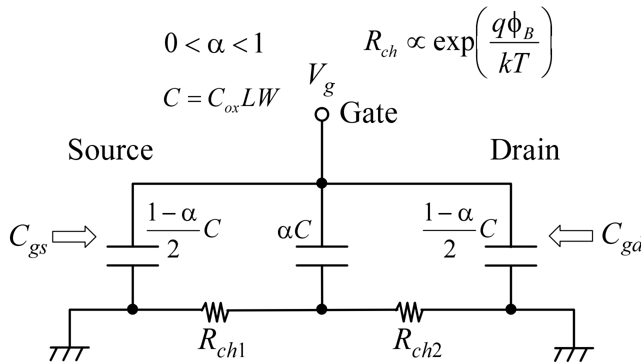

Fig. 7. Equivalent circuit model explaining the differences in the characteristics of the gate-to-source (C_{gs}) and the gate-to-drain (C_{gd}) capacitances due to the GB. The channel resistance R_{ch} is proportional to $\exp(q\phi_B/kT)$. α=0.5 was used in the calculations.

when the GB is at the drain side. The calculated results successfully reproduce the differences in the characteristics and the asymptotic behavior of C_{gs} and C_{gd} shown in Fig. 3(b), confirming the validity of the model.

V. Conclusion

The $C-V$ characteristics of short-channel poly-Si TFTs containing only a single GB were investigated using a two-dimensional device simulator. It was demonstrated that the drain/source charge partition is significantly affected by the position of the GB, which results in differences in the characteristics of C_{gs} and C_{gd}, even if no bias is applied between the source and drain. A new equivalent circuit model was also developed that explains the differences in the characteristics due to the GB.

Acknowledgment

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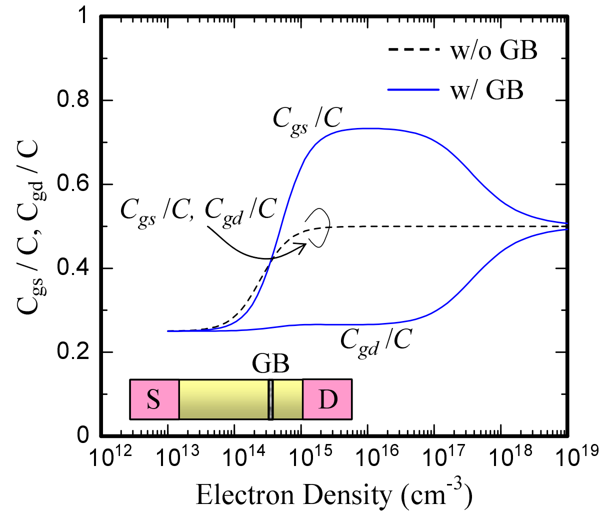

Fig. 8. Capacitances calculated as a function of the channel electron density using the equivalent circuit model shown in Fig. 7.

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