Study of Stress Effect on Replacement Gate Technology with Compressive Stress Liner and eSiGe for pFETs

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***Abstract*—The stress effect at the channel region of pFETs with compressive stress liner (c-SL) and eSiGe using replacement gate technology is firstly investigated in detail based on the combination of UV-Raman spectroscopy and 3D stress simulation. The gate length effect for the channel stress is confirmed by measurement and simulation. Moreover, the Ion dependence on the channel width is also investigated. It is found that the lateral stress along the channel is enhanced at the edge beside STI, resulting in high Ion at narrow gate width region.**

Keywords: Stress, Strain, Simulation, Mobility enhancement, Replacement-gate,Damascene-gate,Gate-last, Raman spectroscopy

I. INTRODUCTION

High-performance metal/high-k gate FETs with top-cut c-SL and eSiGe have been recently achieved by using replacement gate (gate last) technology [1][2]. We have already reported that the channel stress is significantly enhanced by this technology, especially in short gate length region [1][3][4]. Due to this stress enhancement, the Ion gain with stress boosters is greater than that of conventional gate first process. In order to understand this mechanism in detail, direct measurement of the channel stress is necessary. Recently, UV-Raman spectroscopy has been applied to the measurement for local and global strains [5-7]. In this paper, the stress in the channel region, derived from UV-Raman spectroscopy, is compared with 3D stress simulation, for the first time. The gate width effect for the channel stress distribution is also investigated, and the mechanism of the current enhancement for narrower channel width is discussed.

II. RESULTS AND DISCUSSION

Fig. 1 shows the basic concept of stress enhancement by replacement gate technology. The detailed fabrication process is reported in [1]. The eSiGe S/D is epitaxially grown after 80nm Si recess. A 40nm c-SL with 2GPa compressive stress is formed on dummy poly-Si gate (Fig.1(a)). Note that this figure (Fig.1(a)) also represents the conventional gate first process. After ILD deposition, the top of c-SL is cut by CMP process, and the dummy gate is removed (Fig.1(b)). As shown in Fig.1(a), the dummy gate has a reactive force against the stress from eSiGe and c-SL, resulting in reduction of the lateral compressive stress at the channel. On the other hand, as shown in Fig.1(b), removal of the dummy gate eliminates the reactive force at the dummy gate, thereby enhancing the channel stress. After dummy gate removal, metal/high-k gate stack is formed by TiN/HfO2 using damascene process. The simulated lateral stress distributions obtained by [8] with different gate lengths for gate first and replacement gate processes are shown in Fig. 2. As mentioned above, the lateral stress (Sxx) at the channel is enhanced for the replacement gate technology. This effect is remarkable for the shorter gate length.

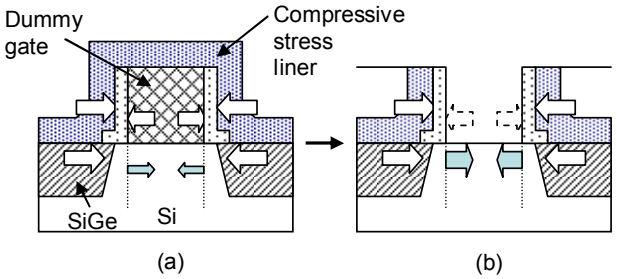

Fig.1 Schematic picture of stress enhancement effect with eSiGe S/D and top-cut c-SL for replacement gate process. (a) Aftre e-SiGe S/D and c-SL formation. (b) After CMP and dummy gate removal.

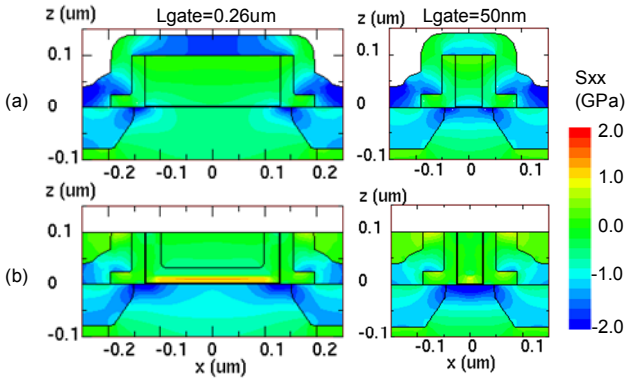

Fig. 2 Simulated lateral stress (Sxx) dependence on gate length for (a) gate first and (b) replacement gate processes.

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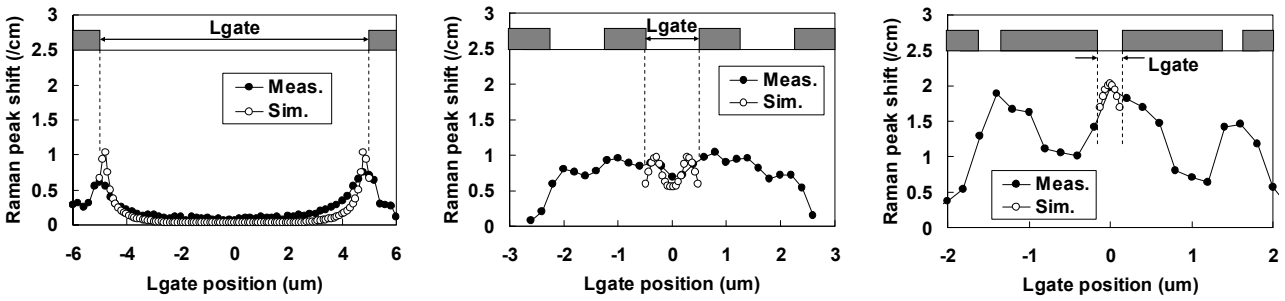


(a) Lgate=10um (b) Lgate=1um (c) Lgate=0.26um

Fig. 3 Measured and simulated Raman peak shift for different gate lengths. The space between gray boxes (showing "Lgate") represents the gate opening after dummy gate removal.

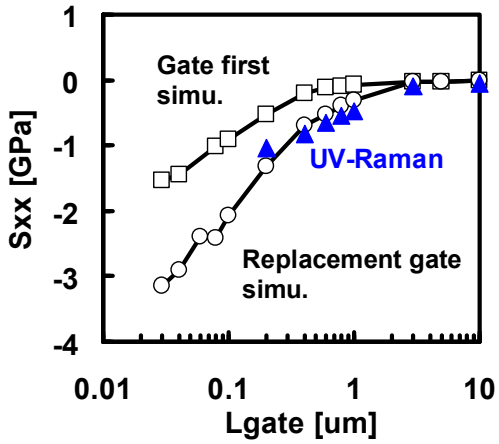
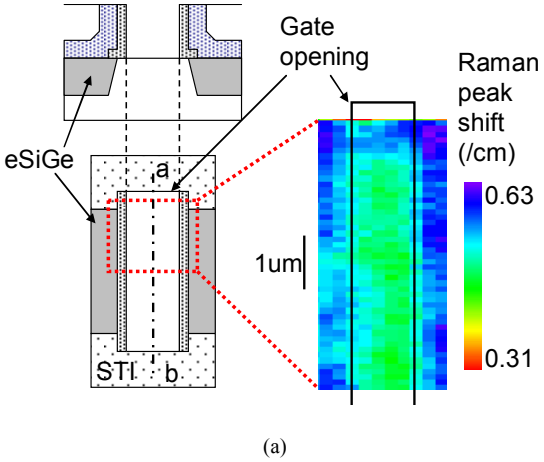
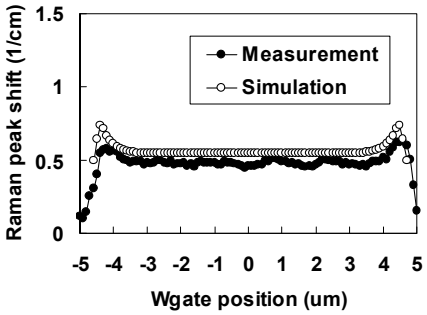


Fig. 4 Simulated Sxx at the center of the channel. The derived stresses from UV-Raman measurement are also plotted.



(a)



(b)

Fig. 5 (a) Raman peak shift mapping around the edge of the channel with L=1um and W=10um. (b) Measured and simulated Raman peak shifts at the channel center (from point a to b).

In order to measure the strain at the channel, the UV-Raman spectroscopy measurement was performed after dummy gate removal. The penetration depth of the excitation source (Ar ion laser, λ=364nm) is approximately 5nm [6]. This measurement is applicable only to the replacement gate process since the initial dummy poly-Si gate is eliminated during the process. Fig. 3 shows the Raman peak shift distributions at the channel region. The positive Raman peak shift represents the compressive strain. As can be clearly seen in the figure, shorter gate length devices have higher stress, which is expected by the stress simulation. The calculated Raman peak shifts based on stress simulation using [8] are also plotted in the figure. The simulated Raman peak shifts show good agreement with the measurement. This confirms the simulated stress values and distributions are considerably accurate for the replacement gate structures. Fig. 4 shows comparison of Sxx values at the channel center for gate first and replacement gate processes. The results of UV-Raman measurement are transformed to Sxx, where all the shifts are assumed to be due to uniaxial stress along x direction [9]. The estimated lateral stress based on the UV-Raman spectroscopy is in good agreement with the stress simulation. The replacement gate process has a potential to apply higher stress at the channel than the conventional gate first process.

Fig. 5(a) shows the 2D Raman peak shift mapping around the edge of the channel, where the channel length and width are 1um and 10um, respectively. The spatial resolution of the system is 200nm [6]. From the 2D mapping result, the high stress region is observed at the edge of Lgate direction due to

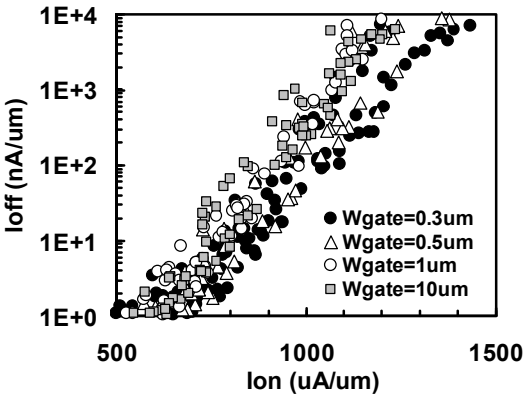
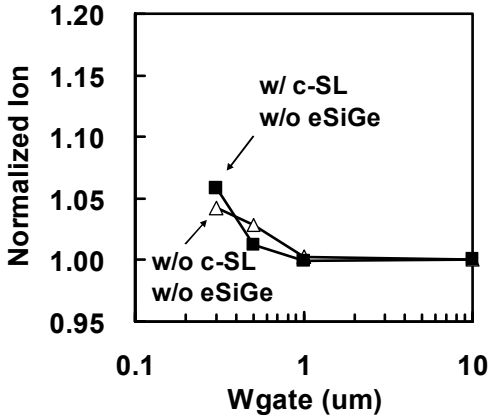
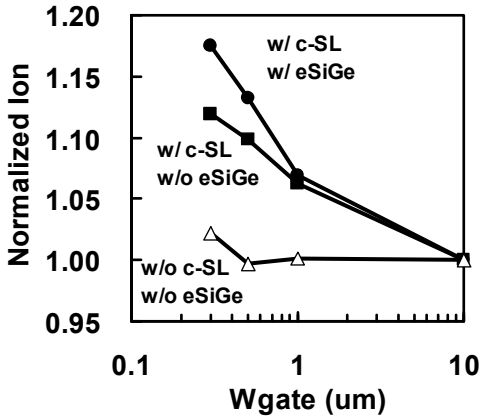


Fig. 6 Ion-Ioff characteristics for different Wgate with replacement gate. Vgs=Vds=-1.0V.



(a)



(b)

Fig. 7 Normalized Ion (Ioff=100nA/um, Vgs=Vds=-1.0V) dependence on Wgate. (a) Gate first. (b) Replacement gate.

eSiGe S/D. There is also high stress region at the edge of Wgate direction, where the stress is applied from STI. Comparison between measured and simulated Raman peak

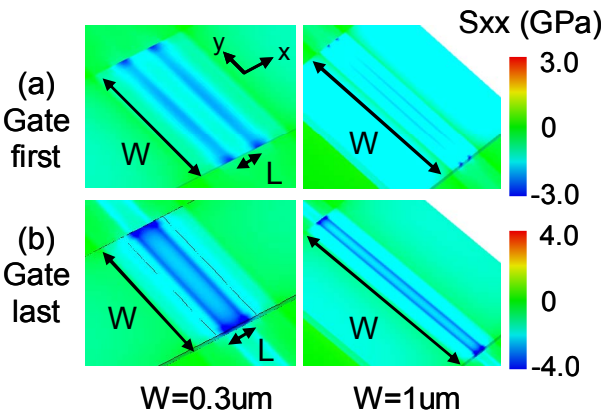


Fig. 8 Sxx distribution for W=0.3um and 1um. L=50nm. (a) Gate first. (b) Replacement gate.

shifts in Wgate direction is shown in Fig. 5(b). The stress distribution along Wgate direction also shows good agreement with Raman measurement. From Figs. 3 and 5, the stress simulation for both directions (L and W) is considerably accurate.

The Ion-Ioff characteristics for different gate width by replacement gate process with c-SL and eSiGe are shown in Fig. 6. This figure demonstrates the higher drivability for narrower width pFETs with c-SL and eSiGe. Fig. 7 shows the normalized Ion gain for different gate width by (a) gate first and (b) replacement gate processes. For the gate first process, the Ion variation for narrower Wgate is small. On the other hand, the Ion gain of replacement gate process is significant as the gate width is narrowed when c-SL and eSiGe is applied. This result indicates that the stress effects have an important role for Ion enhancement in replacement gate process.

The 3D stress simulation is performed for different gate width as shown in Fig. 8. In this calculation, the gate length is 50nm and c-SL and eSiGe are applied. It is clearly found that the high compressive Sxx stress is concentrated near the edge of the channel beside the STI in the replacement gate case. This effect is not observed in gate first process. The stress concentration is peculiar effect for the gate last process, and the width of the high stress region is almost the same even if the channel width is varied. This means that the stress enhancement is not the effect from the channel center, but the side effect of the channel.

Fig. 9 shows Sxx distribution along Wgate direction at the Lgate center, where the gate width is normalized and the position 0 and 0.5 represent channel center and edge in Wgate direction, respectively. The compressive stress in lateral-direction (Sxx) at the channel edge is significantly increased, and the magnitude of the stress at the channel edge is almost the same for each gate width. However, the relative width of high lateral stress region is wider for shorter gate width. In the case of W=0.3um, approximately 15% of the gate width has high lateral stress for each side of the channel. The mobility enhancement for each point is estimated by using piezo-resistance coefficients [10]. The estimated mobility is shown in Fig. 10. This result proves that the Ion enhancement of narrow

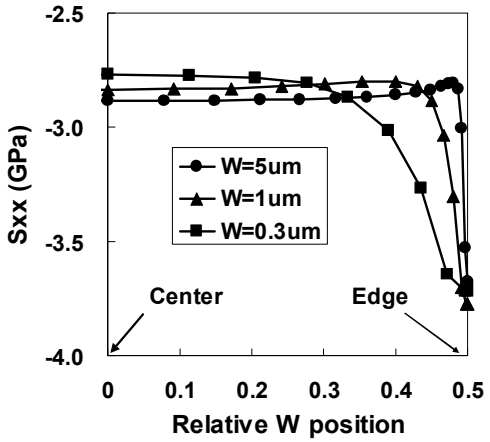


Fig. 9 Sxx distribution along Wgate direction. W position is normalized by gate width, where 0 represents the gate center.

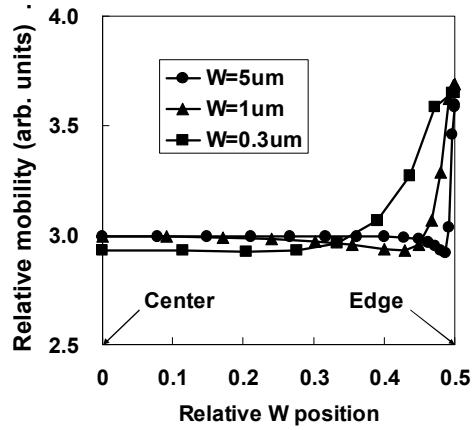


Fig. 10 Mobility enhancement variation at each relative W position.

Wgate pFETs is owing to the increase of high mobility region near the channel edge. Thanks to this effect, the high Ion current of 1090 uA/um at Ioff=100nA/um and Vdd=-1.0V with 0.3um gate width is achieved by our replacement gate technology.

CONCLUSION

The stress effect at the channel in pFETs with stress boosters is investigated in detail by means of stress simulation and UV-Raman spectroscopy. It is confirmed that the results of stress simulation considerably agree with the measured Raman shift data. The mechanism of Ion enhancement at narrower channel width for replacement gate technology is analyzed by 3D stress simulation. We concluded that the enhancement is due to stress concentration effect at the channel edge in Wgate direction. This technology has great potential for scaled devices.

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