A Unified Approach for the Reliability Modeling of MOSFETs

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***Abstract*—Modeling capabilities and considerations to achieve a unified reliability model (URM) are addressed. The causes of the trap generation and their effects on the device characteristics serve the unified reliability model. A strategy taken in the SNU group based on the CLESICO system is introduced, where the hydrogen transport and trapping in the gate dielectric to form active carrier trapping sites and their effects on the device characteristics such as the current degradation are treated in a systematic and statistical manner. The treatment of the discrete nature of the trapped charges to model the RTS and 1/*f* noises are also introduced.**

Keywords-unified reliabity model (URM), hydrogen transport, NBTI, SILC, RTS, noise, mobility, trapped electron

I. INTRODUCTION

As the size of MOSFET device has been continuously scaled down, the reliability issues such as threshold voltage shift, mobility degradation, gate leakage current, 1/*f* and random telegraph signal (RTS) noise become the limiting factor for the scaling [1]. The origin of these reliability degradations is the traps mostly distributed in the oxide region and the effects due to these traps become more important as the oxide thickness becomes thinner. In this paper, we introduce a unified modeling strategy taken by the SNU group based on the CLESICO systems which has been developed to model the effects of noise sources in the device on both the autonomous and the forced circuit system [2]. This unified picture includes the following steps:

(1) Mechanisms involved in the creation of active traps (Cause),

(2) the roles of the generated active traps on the device and circuits characteristics (Effect) in a statistical way,

(3) the effects of device operation to the cause of the trap generation (Feedback to (1)).

The 'Cause' activity gives the spatial and energy distribution of the traps in the gate dielectric in both short and long time scales. The obtained trap information will give the 'Effect' on MOSFET device/circuit parameters in a statistical manner. In this paper, a strategy taken in our group for each step (especially the step 1 and 2) and considerations to be made for the further development for the URM will be explained.

II. THE CAUSES AND EFFECTS OF THE TRAPS

A. The Cause of the trap

In the 'Cause' activity, the energy exchange mechanisms between carriers and interface/insulator bulk are involved. The dependencies of the defect generation on temperature, bias conditions are also involved and experimental observations on the dependency will help to generate the physically sound model for the cause of the traps. Several causes of the traps are summarized in Table I.

There is still a controversy whether the stress-induced gate leakage current (SILC) is caused by the anode hole injection (AHI) or hydrogen release (HR) as found in the negative-bias temperature instability (NBTI). Recently, it has been suggested that the SILC and NBTI have a common physical origin, which is caused by the generated hydrogen in the silicon interface [3][4].

B. The Effects of the trap

The spatial distribution of the traps in the gate oxide and its effects on the device reliability are summarized in Table II. The proposed physical origin of the traps and the degradation mechanisms are also shown.

In Table II, we can infer that the spatial distribution of the traps is the decisive factor for the device degradation. The trap which is in the middle of the oxide can contribute to SILC. This current can be calculated in a statistical way for MOSFETs and Flash memory cells [5]. Furthermore, the traps which are located near the interface contribute to 1/*f* noise effectively acting as the trap/capture centers for carriers. As the device dimension shrinks so small that the device contains a single trap, the RTS noise is observed [6]. The RTS noise is critically dependent on the spatial distribution of the traps in the oxide.

III. HYDROGEN RELATED TRAP

From the 'Cause' and 'Effect' chart, we can infer that NBTI and SILC are connected via the hydrogen release from the saturated SiH. The hydrogens generated by the NBT stress can be the source of the reaction creating the hydrogen bridges in the oxide, which results the active traps responsible for SILC [3][7]. We choose H^+ as a diffusing species here, because H_2 is not reactive to make the hydrogen bridge and H is not

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thermodynamically stable in the oxide. The diffusing species can be easily substituted in the model later if needed.

A. Generation of Hydrogen related Species

The continuous-time random walk (CTRW) formalism [9][11] is adopted here to describe the hydrogen transport mechanism. The hopping mechanism is simulated by the Monte-Carlo method with the hopping time distribution as $\psi(t) \sim t^{-(1+\alpha)}$ [10].

With this simulation method for the hydrogen transport, we simulate the hydrogen generation under the NBT stress. We adopt a conventional reaction-diffusion model to describe the generation (hence the interface states) and recombination of the hydrogen at the interface [12]. We carry out the simulation for the 1D MOS structure and with the gate oxide thickness of 30 nm. The rate of breaking of the SiH bonds at the interface should be known from the device simulation (step 3 in Section I).

In Fig. 1, the interface trap generation is shown as a function of time with the oxide complexity, α, as a parameter. In Fig. 2, the dependence of the interface trap generation on the field intensity is shown, which shows a fixed slope with a different field condition.

B. Hydrogen diffusion and SILC trap

The released hydrogens from the interface make the hydrogen bridges and contribute to the device instability such as the SILC and eventually the soft breakdown [3][7]. The hydrogen bridge profile under the NBT stress can be calculated using our hydrogen transport calculation including the chemical reaction rate equation of the oxygen vacancy and hydrogen. At the oxygen vacancy (a precursor for an active trap) site, the hydrogen can be captured by the following reaction [7]:

$$[\text{Si-Si}] + [\text{H}^+] \leftrightarrow [\text{SiHSi}^+]$$

For a given distribution for the precursors (uniform distribution in the present case), the spatial profiles for the hydrogen bridge and the oxygen vacancy are shown in Figs. 3 and 4, respectively[1]. From the hydrogen-bridge profile, we can calculate the SILC by the device simulation with the tunneling model [5].

IV. Effects of the Discrete Trapped Charges

Once the oxide trap sites are obtained, the effects of the trapped charge on the device characteristics can be predicted. It should be pointed out that the trapped charges are discrete in nature, so that three factors should be considered:

- the finite spatial distribution of the trapped charges,
- the effects of the charges on the carrier concentration,
- the mobility effect, none of which have been properly dealt with to our best knowledge.

A. Spatial Distribution of the trapped charge

In order to estimate the oxide charge distribution in the oxide, the density functional theory (DFT) calculations are carried out with the ABINIT code [12], using the pseudo-potentials and plane-wave basis. The Goedecker-Teter-Hutter pseudo-potentials are used for electron-ion interactions, and the exchange-correlation effects are treated in the local density approximation (LDA). The calculations were done in α-quartz. A tetragonal super-cell is used containing 72 atoms (24 SiO_2 formula units) [7]. The oxygen vacancy site and non-bonding oxygen site are incorporated. The trapped electron in the defect site having negative charge is depicted in Figs. 5 [2] and 6 (we neglect the lattice relaxation here).

B. Effects of carrier concentration

The trapping and detrapping of a charge in oxide layer result in the local modulation of channel carrier density and potential, which are manifested in the RTS noise [6][24]. An in-house 3D simulation tool based on the density-gradient (DG) model is used to include the quantum transport effects.

As an example, two cases are simulated to investigate the effect of the spatial distribution of a single trap; one is with a point charge in 5 Å mesh and the other is with a Gaussian distribution having a characteristic length of 4 Å (in 1 Å mesh). Fig. 7 a) and b) show the 3D potential profiles for two cases, respectively. The simulation is performed at V_G = 1.2 V and V_D = 0.05 V, and the single trap is located at 10 Å from the interface. The potential difference of about 0.75 V found in the figure is originated from the difference in the Coulomb potential, suggesting that proper treatment of the trap charge in oxide layer is critical in obtaining the correct surface carrier density in the numerical simulation. In Fig. 8, the effects of the trap on the carrier concentration are shown together with the drift-diffusion (DD) calculation as a reference.

Consequently, the effects of different treatments in the finite size of the trapped charge on the device current are critically dependent on the device size and the location of the trap. The statistical effects due to the random location of the traps on the drain current can be obtained by the CLESICO system with the 3D device simulation built-in. An application example will be shown in the literature [13].

C. Effects of the local mobility modulation

Not only the carrier number fluctuation but also the mobility fluctuation causes the degradation on device current. Therefore, the local mobility model is needed in the device simulation framework such as the 3D DD simulation used in this work[3].

Here, we propose a local mobility model for a single trapped charge. Let us assume that the total scattering due to the trapped electron is a function of the local electric potential variation only. Hence, as a first-order approximation, we also assume that the variation of scattering rate, $\delta\Gamma(\mathbf{r})$ is

[1] The generation rate for the hydrogen bridge is unknown and can be used as a fitting parameter. The reverse reaction is neglected for this simulation.

[2] The order of the states is not accurate since the alpha quartz is calculated. The Oxygen Vacancy in amorphous structure must be used to calculate a trapped charge [22].

[3] In this case, DD simulation is used since the experimental device size is large, i.e. W/L=385/187nm.

proportional to $\delta V(\mathbf{r})$ in the channel region. Therefore, we can write the local mobility model ($\mu(\mathbf{r})$) as follows:

$$\mu(r) = \frac{q}{m^*\Gamma(r)} = \frac{q}{m^*\left(\Gamma_0(r) + \delta\Gamma(r)\right)} = \left[\frac{1}{\mu_0(r)} + \frac{m^*\delta\Gamma(r)}{q}\right]^{-1} = \left[\frac{1}{\mu_0(r)} + \beta\delta V(r)\right]^{-1}$$

where β is a constant fitting parameter, q is the magnitude of electron charge, and m* is the effective mass. The fitting parameter β is about 600 (sec/m^2) in our simulation. Through our approach, we can calculate the mobility and carrier number fluctuation, separately.

Fig. 9 (a) shows that $\delta V(\mathbf{r})$ is very small compared to the surface potential and Fig. 9 (b) shows that the maximum value of the local mobility variation at the interface is about 50% at V_G = 0.6 V and V_D = 0.02 V. Our simulation shows good agreement with the experimental results as shown in Fig.10. The portion of mobility fluctuation is about 20% at V_G = 0.6 V and V_D = 0.02 V.

V. CONCLUSIONS

We have introduced our efforts to achieve the Universal Reliability Modeling (URM). The generation of discrete defects, 'Cause' of the reliability, has been modeled by simulating the proton transport and reaction with the vacancy in the oxide. The charge state has been studied by the ABINIT simulation in order to obtain the finite spatial distribution of the trapped charges. The effects of the 'Cause' on the device characteristics are predicted by a 3D simulation tool based on the density gradient model including the carrier number and mobility fluctuations. The statistical noise characteristics can be readily modeled through the help of CLESICO system with the 3D simulation built-in.

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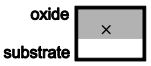
TABLE I. STRESS: CAUSE OF TRAP

Bias Condition	**Gate tunneling**	**NBTI**	**GOI (Gate Oxide Integrity) Stress**	**V_{DD} AC and/or DC**
Driving Force	***AHI***	***Field and Temperature***	***Field and Temperature (Thermochemical E, 1/E)***	***Hot carrier due to high drain voltage***
Physical Effect	***Bulk Trap generation [7] H emission [15]***	***Interface and Bulk trap due to H generation [3][19] Hole trapping [25]***	***Oxide Bulk [21]***	***Oxide Bulk Interface [18]***
Energetic Carrier	***Yes No (minority carrier injection [23]])***	***No***	***No***	***Yes***

TABLE II. DEVICE DEGRADATION DUE TO TRAP

EFFECT	**Vth degradation**	**SILC**	**TDDB**	**1/f**	**RTS**
Trap Distribution					
	interface	***Oxide bulk (mainly in the middle)***	***Percolation path***	***Near interface***	***Near interface***
Physical Origin	***Dangling bond at interface (Pb-center) [19]***	***Broken Si-O bonding [16] Hydrogen Bridge [7]***	***Broken Si-O bonding [21]***	***Hydrogen bridge? [17] Oxygen Vacancy? [17]***	***Hydrogen bridge? [17] Oxygen Vacancy? [17] Non-Bonding Oxygen?***
Degradation Mechanism	***NBTI [19] Hot Carrier [18]***	***AHI [16] NBTI(HR) [3]***	***Thermochemical E [20], 1/E [21]***	***Hydrogen Release?***	***Hydrogen Release?***

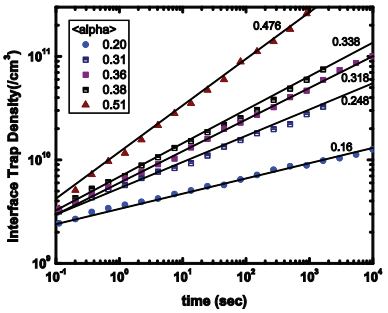


Figure 1. Interface trap generation under the NBT stress is simulated according to the oxide alpha parameter (alpha represents the oxide disorder).

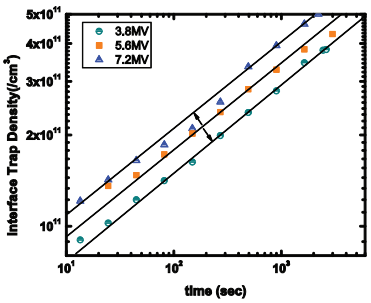


Figure 2. Interface trap generation under different oxide field conditions. The alpha number is 0.33 and the slope is uniform under field variation.

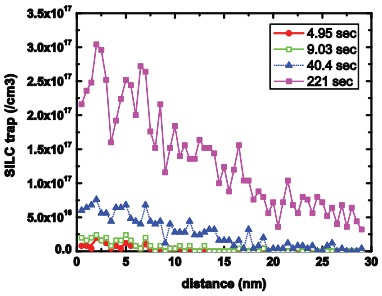


Figure 3. Hydrogen Bridge generation under the NBT stress (the initial precursor profile is uniform in space).

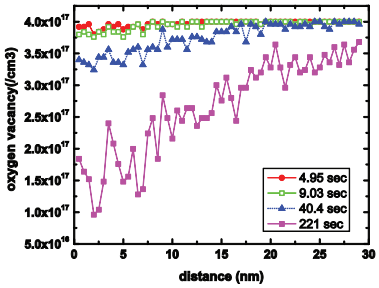


Figure 4. Oxygen vacancy consumption under the NBT stress (the initial profile is uniform in space).

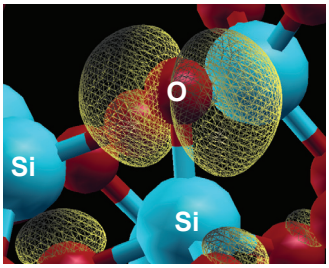


Figure 5. Trapped electron in the non-bonding oxygen defect site (HOMO).

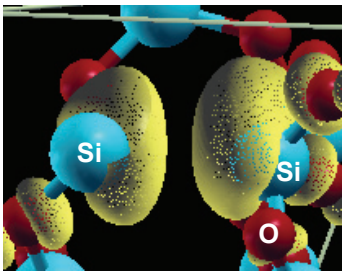


Figure 6. Trapped electron in the oxygen vcancy defect site (must be LUMO).

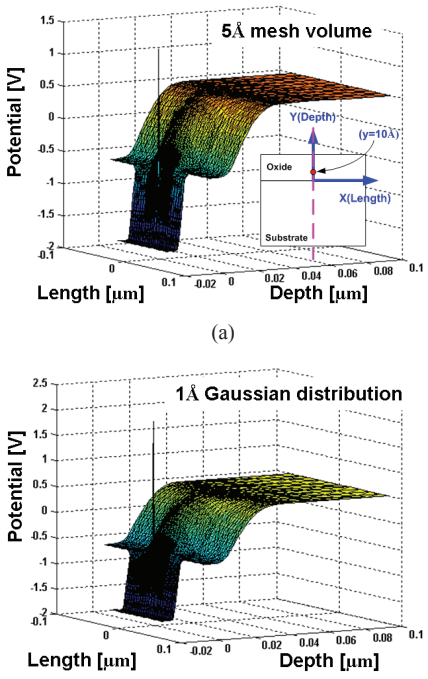


Figure 7. 3D potential profiles for a point electron trap in 5Å mesh (a) and a Gaussian distribution of 4Å characteristic length (b) in oxide layer.

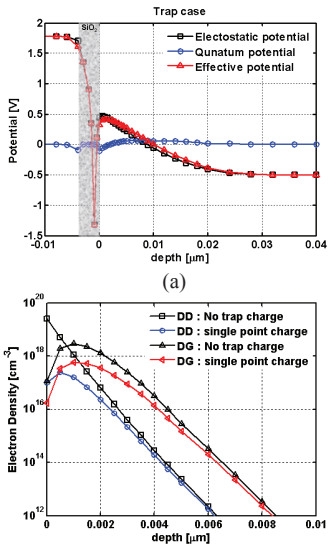


Figure 8. Potential (a) and electron density (b) profiles along the 1D cut line through the center of channel.

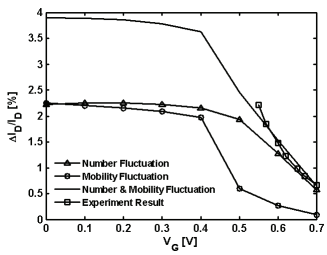
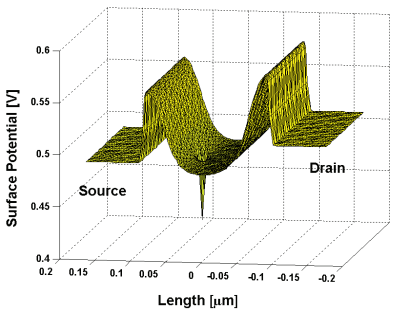


Figure 10. Experimental and simulated results of $\Delta I_D/I_D$ at V_D=0.02 V.



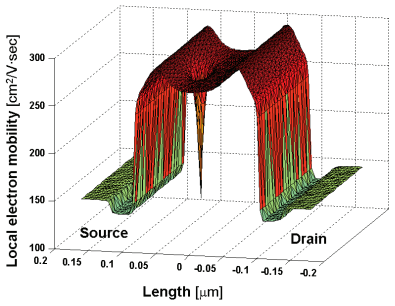


Figure 9. Electric potential (a) and local mobility (b) on Si-SiO_2 interface when the oxide trap is filled with a single electron at V_G=0.6 V and V_D=0.02 V.