

Transient device simulation of trap-assisted leakage in non-volatile memory cell

Hiroshi Watanabe

Advanced LSI Technology Laboratories,
Toshiba Corp.,
Isogo, Yokohama 235-8522, Japan
pierre.watanabe@toshiba.co.jp

Abstract—In order to study how a local trap degrades data retention characteristics of floating gate nonvolatile memory cell, a general-purpose Single-Electron Device Simulator (SEDS) developed for Si-dot is improved to carry out a very wide range transient analysis from 0.1 pico-seconds to 10 years. As a result, it is found that the data retention is degraded by the direct tunneling enhanced due to positive charge stored at the trap inside the inter-poly dielectric but not by trap-assisted tunneling.

Keywords-local trap; nonvolatile memory; device-simulation; transient analysis;

I. INTRODUCTION (HEADING 1)

Aggressive scaling of non-volatile memory (NVM) cells makes an impact of local trap on leakage current more significant. Since injection or emission of a few electrons modulates potential profiles around the traps that might cause trap-assisted leakage current, the operation of such an NVM cell might appear quite sensitive to single-electron hopping via local trap. Figs. 1 and 2 schematically describe all possible transitions among the charge-states of (+2), (+1), (0), (-1), and (-2) via the traps in oxide-nitride-oxide (ONO) inter-poly dielectric (IPD) between floating gate (FG) and control gate (CG) and tunnel oxide between substrate and FG, respectively. Fig. 3 schematically describes three-dimensional sample structure used in the present device simulation, in which there is a local trap, i.e., Trap-A at the center of ONO-IPD (effective oxide thickness, EOT=6.7nm) or Trap-B at the center of 10nm tunnel oxide. Considering the freedom of spin, the trap can store four electrons at most and it has two electrons at charge-neutral state. Then, we have 5 states, (+2), (+1), (0), (-1), and (-2), with regard to stored charges, of which the emission mode is dependent. A decrease of negative charges makes the

trap-level downward in energy band diagram, then enhancing the injection of electron to the trap and suppressing the emission, while increase of negative charges makes the trap-level upward, then suppressing the injection and enhancing the emission. The electron emission from the upper state is fast-mode in leakage and that from the bottom state is slow-mode [1]. It is noted that the local trap has too small volume for us to define capacitance couplings around the trap. Therefore, since we cannot determine the potential of local trap using the capacitance couplings around the trap, we need a solver which is sensitive to single-electron potential change due to emission-injection of single-electron, which is so-called “*single-electron sensitivity*” in calculation, as similar to Si-dot [2].

Next, let us consider a detailed balance at which the rates of injection and emission are the same between two adjacent charge-states in Figs. 1 and 2. The hopping of electrons via local trap would make the potential oscillate around the detailed balance point. When electric field is low, the detailed balance may exist between (-2) and (-1). Increasing the electric field, it would transport to between (-1) and (0), between (0) and (+1), and between (+1) and (+2). This is quite similar to the hopping transport via Si-dot [2]. However, since the data retention is a long-term transient phenomenon, at most decade, the oscillation period would be a few months. Then, we have to improve general-purpose Single-Electron Device Simulator (SEDS) that has *single-electron sensitivity*, as demonstrated in [2], for studying whether such a long-term single-electron oscillation occurs or not.

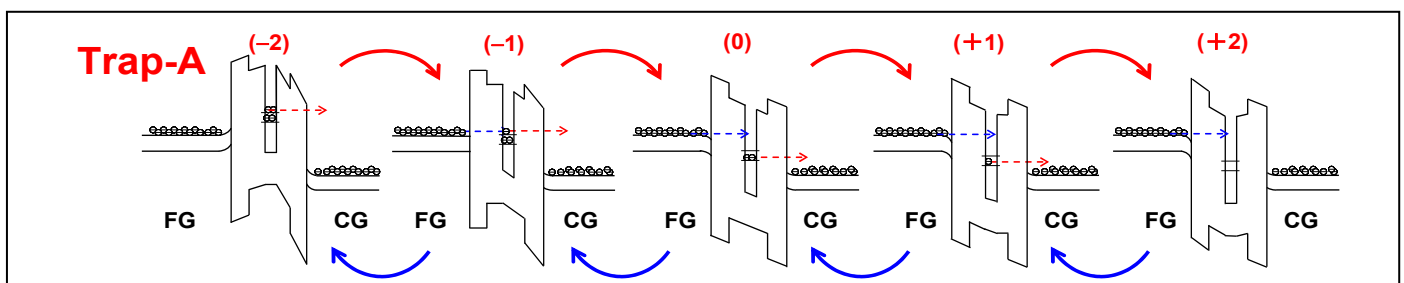


Figure 1. Hopping transport via local trap (Trap-A in Fig. 3)

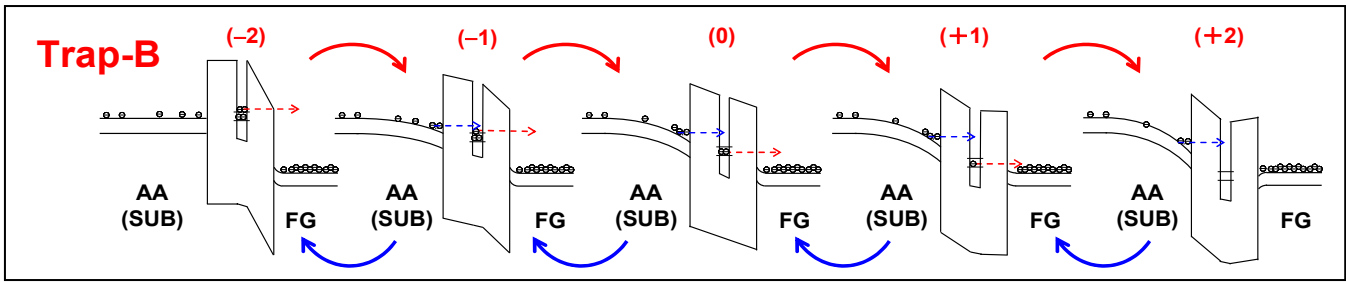


Figure 2. Hopping transport via local trap (Trap-B in Fig. 3)

II. CALCULATION

As mentioned above, since local traps are quite small and not connected to any electrode defining the boundary condition of potential profile there, it was difficult to solve the potential profile around the local traps. We, however, have already resolved this problem in a case of Si-dot, using a self-consistent iteration method of high-precise physical models [3-6] and Harrison's formula for calculating emission and injection rates [7]. This enables us to achieve an amazing precision which can detect single-electron modulation in potential profile, *single-electron sensitivity*, with general-purpose device-simulation [2]. We implemented these modules to the long term transient device simulator [8] and apply it to a local trap having bi-state levels according to [9], assuming that the upper and bottom states exist at the level that is lower than the conduction band edge by 0.8eV and 2eV, respectively [1].

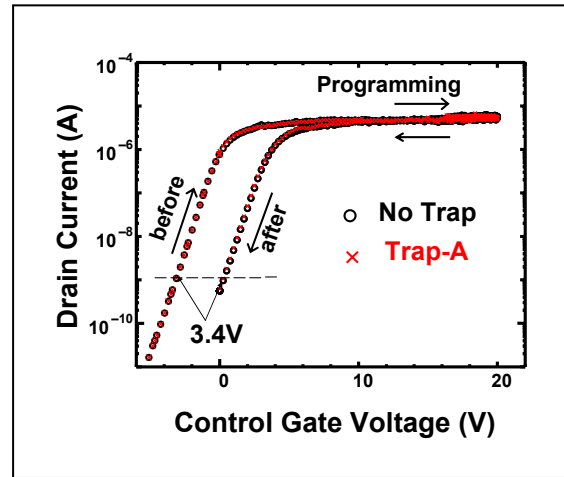


Figure 5. I_D - V_G characteristic Profile of applied bias

III. RESULTS

The device simulation was carried out in cases of no trap, Trap-A, and Trap-B. The applied biases on CG and the drain are shown in Fig. 4. The source and substrate are grounded. Fig. 5 is the calculation result of I_D - V_G characteristics. The data were plotted under bias condition from -2 nano-seconds to 2 nano-seconds in Fig. 4. In other words, starting voltage is $V_{CG} = -6V$, increasing it to 20V, after that decreasing to 0V. The V_{TH} -shift, defined as discrepancy between before and after programming in control gate voltage at $I_D = 1$ nano-ampere, is 3.4V irrespective of with or without Trap-A. This means that Trap-A has a negligible impact on the programming characteristic.

In Fig. 6, it is shown that we have no oscillation after Trap-A is saturated at (+2) during the programming, while the one-by-one emission appears in scale of 0.1 nano-second before the saturation. This leaves a fixed positive charge in IPD layer. In right side, we have no pumping (i.e., no oscillation) even after the control gate bias is turned off. Since EOT of the IPD layer is much smaller than the tunnel oxide thickness, the electric field across IPD layer is so low that energy level of tunneling electron is lower than levels of Trap-A. As shown in Fig. 7, the IPD-leakage mechanism is therefore the direct tunneling enhanced by barrier lowering due to the fixed positive charge, which is similar to ultrathin gate SiON [10].

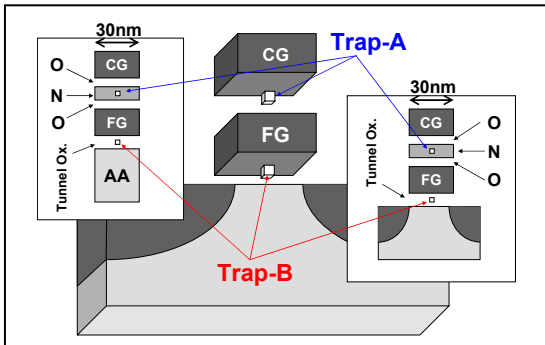


Figure 3. Hopping transport via local trap (Trap-B in Fig. 3)

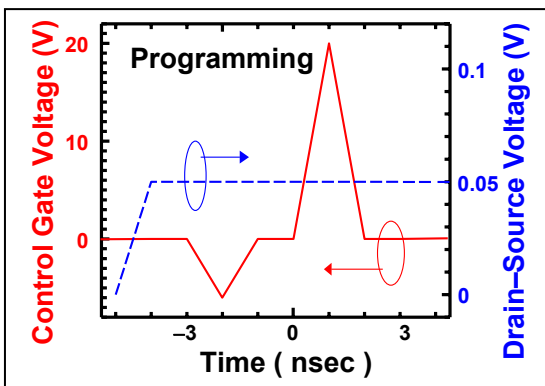


Figure 4. Hopping transport via local trap (Trap-B in Fig. 3)

Figs. 8 and 9 are the calculation results of data retention. The drain voltage is fixed 0.05V during retention state after 2 nano-seconds, as shown in Fig. 4. It is found that the drain current grows up to 1 nano-ampere and the stored electrons begins to be emitted at 4.7 months, which means that the retention characteristics of FG-NVM cell is substantially degraded due to the fixed positive charge at only one local trap in ONO-IPD layer (Trap-A).

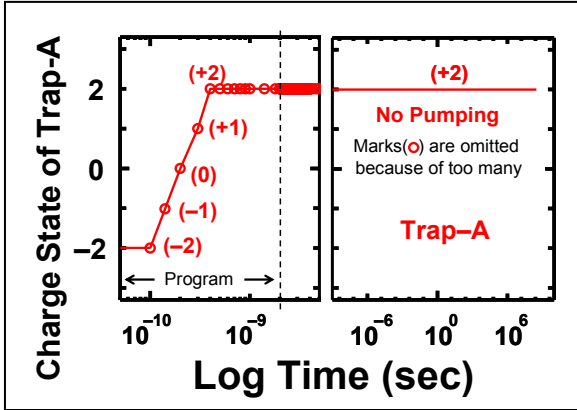


Figure 6. Stored charge at Trap-A

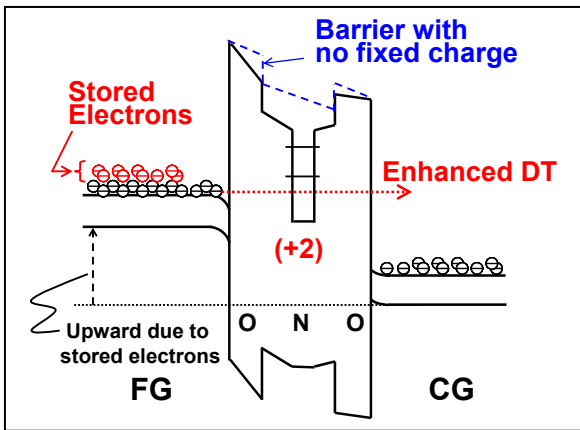


Figure 7. Band-profile around Trap-A in retention state

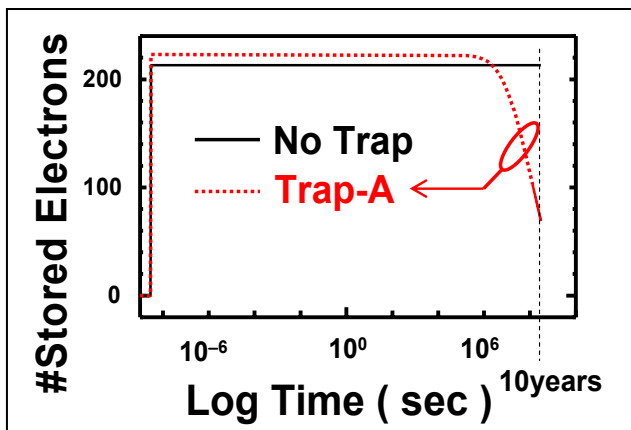


Figure 8. Transient analysis of stored electrons in FG

On the other hand, since the tunnel oxide is too thick for Trap-B to have any impact on data retention. We then removed Trap-B from the long-term plot. In order to investigate an impact of Trap-B, we reduce the thickness of tunnel oxide from 10 nm to 3.2nm, which is equivalent to that thinnest required for 10 years data retention with no trap [8], and EOT of IPD from 6.7nm to 2.2nm. Fig. 10 is the calculation result of charge-states at $V_{CG} = 6V$. We gave four electrons to Trap-B at the initial state, then artificially making non-equilibrium state, (-2). With the elapse of time, these excess electrons are emitted up to 10 pico-seconds, which results in (+2). After that, we can see the potential oscillation between (+1) and (+2), whose phase and period agree with the hopping of electron to FG. Although the broken circle might appear to show the hopping of double electrons at the same time, the insertion clearly shows that the electron hopping must be done with one-by-one. An electron passes through Trap-B to FG during (+1), while another electron transfers from Trap-B to FG during the transition from (+1) to (+2).

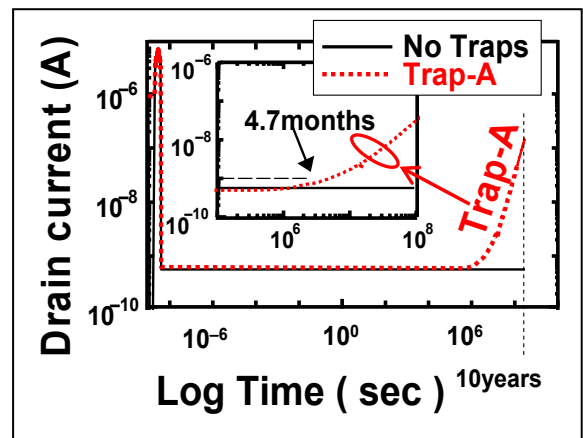


Figure 9. Transient analysis of drain current

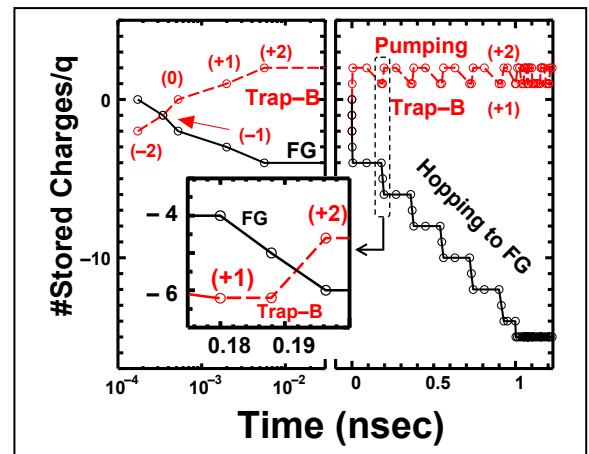


Figure 10. Transient analysis of Trap-B

After 1 nano-second, the oscillation of Trap-B continues while the number of stored electrons in FG is unchanged. This means that the electron comes and goes between Trap-B and the channel, i.e., we have no detailed balance in single-electron phenomena via local trap, while FG is saturated, reaching equilibrium. By this way, the trap-detrap phenomena has too short period to have any impact on long-term transient phenomena, i.e., data retention characteristics. The shortest period is 0.1pico-second in the present demonstration with SEDS, which means that the SEDS's potential meets the study of 10 tera-hertz random telegraph noise. Additionally, the present bi-state trap model is similar to Ielmini's ones for SILC [11] and PCRAM [12], which suggests a substance of trap-detrap phenomena.

IV. SUMMARY

We improved a general-purpose Single-Electron Device Simulator (SEDS) to carry out a very wide range transient analysis from 0.1 pico-seconds to 10 years. It is then found that data retention of FG-NVM cell is degraded from 10 years to less than 5 months with only one trap in ONO-IPD layer, which mechanism is the enhancement of direct tunneling due to fixed positive charge and not trap-assisted tunneling that causes much higher frequency phenomena, for example, random-telegraph noise.

ACKNOWLEDGMENT

The author would like to thank A. Fathurahman and D. Hagishima for their fixing bug of the source-code.

REFERENCES

- [1] T. Maruyama and R. Shiota, "The low electric field conduction mechanism of silicon oxide-silicon nitride-silicon oxide interpoly-Si dielectrics", *J. Appl. Phys.* vol. 78, pp. 3912-3914, 1995.
- [2] H. Watanabe, "Hopping transport of electrons via Si-dot", *SISPAD07*, Vienna, 2007.
- [3] H. Watanabe and S. Takagi, "Effects of incomplete ionization of impurities in poly-Si gate and band gap narrowing on direct tunneling gate leakage current", *J. Appl. Phys.* vol. 90, pp.1600-1607, 2001.
- [4] H. Watanabe, "Depletion layer of gate poly-Si", *IEEE TED* vol. 52, pp.2265-2271, 2005.
- [5] H. Watanabe, D. Matsushita, and K. Muraoka, "Determination of tunnel mass and physical thickness of gate oxide including poly-Si/SiO₂ and Si/SiO₂ interfacial transition layers", *IEEE TED* vol. 53 pp.1323-1330, 2006.
- [6] H. Watanabe, K. Nakajima, K. Matsuo, T. Saito, and T. Kobayashi, "Reduction of accumulation thickness in metal gate", *Abs. SSDM05*, pp. 504-505, 2005.
- [7] W. A. Harrison, "Tunneling from an independent-particle point of view", *Phys. Rev.* vol. 123, pp. 85-89, 1961.
- [8] H. Watanabe, T. Ishihara, Y. Matsunaga, K. Matsuzawa, D. Matsushita, and K. Muraoka, "Numerical study of data retention due to direct tunneling for nonvolatile memory cell", *IEEE TED* vol. 52, p. 955-961, 2005.
- [9] J. Robertson and M. J. Powell, "Gap states in silicon nitride", *Appl. Phys. Lett.* vol. 44, pp. 415-417, 1984.
- [10] H. Watanabe, D. Matsushita, K. Muraoka, and K. Kato, "Leakage mechanism of ultrathin SiON gate dielectric", *Abs. SSDM06*, pp. 1126-1127, 2006.
- [11] D. Ielmini, A. S. Spinelli, A. L. Lacaita, D. J. Dimaria, G. Ghidini, "Experimental and numerical analysis of the quantum yield", *IEDM Tech. Dig.*, pp. 331-334, 2000.
- [12] D. Ielmini and Y. Zhang, "Physics-based analytical model of Chalcogenide-based memories for array simulation", *IEDM Tech. Dig.*, 2006