# Full 3D String-level Simulation of NAND Flash Device

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***Abstract*—We present results of full 3D sting-level process and device simulation for a typical 60nm NAND flash device, whose read/program/erase characteristics are successfully simulated using the quasi-steady state simulation method. Self boosting and local-self boosting phenomena are also successfully simulated in string-level applying realistic pulse waves to the entire wordlines and string select line in a fully transient manner. The comparison between the simulation results and the experiments in various bias conditions shows the capability of our simulation methodology for the design optimization of NAND flash device in string level.**

***Keywords-component; NAND flash device; process simulation; device simulation; self boosting; local-self boosting; TCAD***

## I. INTRODUCTION

Nowadays, NAND flash device has become one of the most important devices in semiconductor market, and many researchers have reported its cell-level simulation results [1, 2]. However, with the drastic scaling down of NAND flash device below 60nm, it has become increasingly difficult to control the interference between the neighboring cells, so that it has also become more difficult to design the NAND peripheral circuits optimally. Consequently, the string-level design optimization using TCAD simulation has also become much more important [3], but there has been little report on the concrete simulation methodology for the string-level until now.

The main difficulties in the string-level simulation of NAND flash device are the following;

- Firstly, how to generate the large-scale mesh structure automatically and optimally in string-level.
- Secondly, how to bias all the electrodes for each read/program/erase NAND operation considering their convergence and computational time.
- Thirdly, how to handle a lot of floating regions such as floating gates (FG) and source/drain regions of every cell to avoid convergence problem.
- Finally, how to suppress the numerical noise in the transient calculation of tunneling currents for the entire cell transistors.

Dealing successfully with these difficulties, we have succeeded in full 3D sting-level process and device simulation for the 60nm NAND flash device and demonstrated its capability for the design optimization of NAND peripheral circuits.

## II. SIMULATION METHOD

### A. Simulation Struture and Physical Models

Full 3D process and device simulations in string level are carried out using the latest version of ENEXSS [4]. For the structural information of simulation domain, we referred a typical 60nm NAND flash device [5]. Drift diffusion model is used for the calculation of carrier transport with various generation/recombination models such as SRH/BTBT tunneling and Auger/surface recombination model. Wentzel-Kramers-Brillouin (WKB) and transfer matrix (TM) methods are applied to the calculation of tunneling current during program/erase operation case by case.

### B. Simulation Flow

To generate the N-cells NAND string automatically and optimally, all the structural dimensions are parameterized according to key structural features such as gate length, active width and tunnel oxide thickness. Octree-based tetrahedron mesh satisfying the Delauney condition is generated with normal offset algorithm and optimized with adequate mesh refinement in channel region as shown in Fig.1.

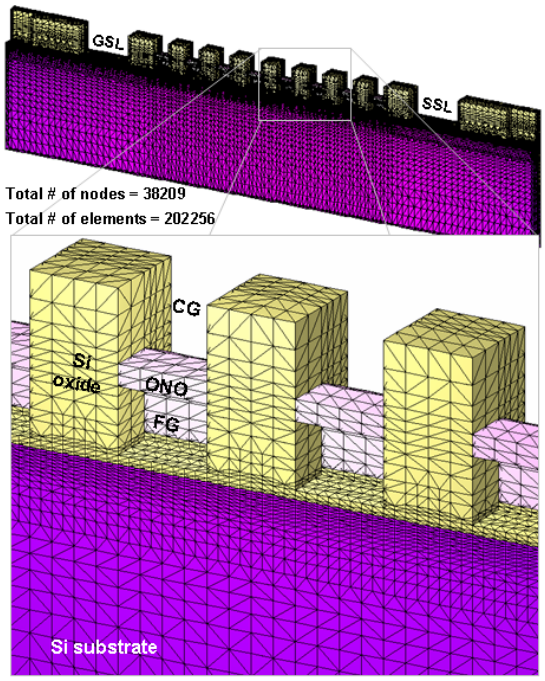
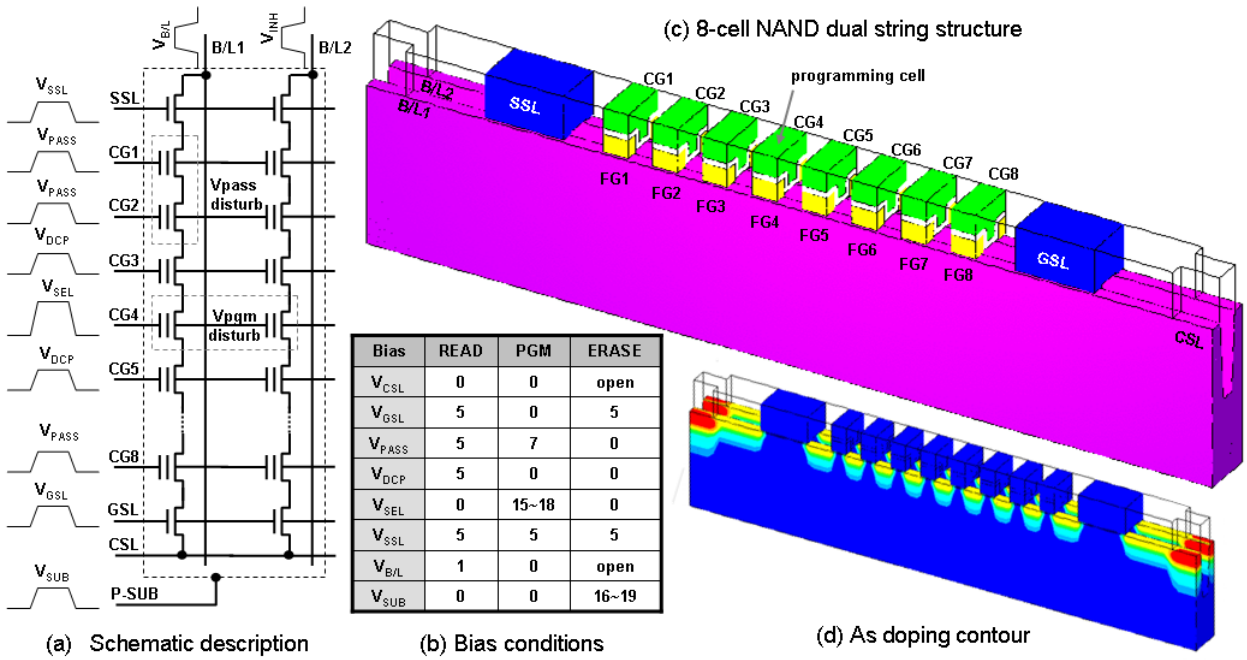



Figure 1. Mesh structure.




| Bias | READ | PGM | ERASE |
|---|---|---|---|
| $V_{CSL}$ | 0 | 0 | open |
| $V_{GSL}$ | 5 | 0 | 5 |
| $V_{PASS}$ | 5 | 7 | 0 |
| $V_{DCP}$ | 5 | 0 | 0 |
| $V_{SEL}$ | 0 | 15~18 | 0 |
| $V_{SSL}$ | 5 | 5 | 5 |
| $V_{B/L}$ | 1 | 0 | open |
| $V_{SUB}$ | 0 | 0 | 16~19 |

Figure 2. (a) Schematic description of NAND flash device, (b) bias conditions for read/program/erase operation, (c) simulation domain and (d) its source/drain arsenic doping contour simulated by HySyProS.

Fig.2(a) shows a schematic description of NAND flash device showing the bias scheme in string-level. Fig.2(b) lists the typical bias conditions [6, 7] applied to common source line ($V_{CSL}$), ground select line ($V_{GSL}$), pass gates ($V_{PASS}$), decouple voltage for adjacent wordlines ($V_{DCP}$), selected wordline ($V_{SEL}$), string select line($V_{SSL}$), bit-lines ($V_{B/L}$), and P-well substrate region ($V_{SUB}$) for string-level read/program/erase operations. Fig.2(c) and (d) are the 8-cell NAND dual string structure consisting of two bit-lines (B/L1 and B/L2) and its source/drain arsenic doping contour generated by the process simulator (HySyProS), respectively.

For the simulation of NAND device characteristics in two different time scales of msec and μsec, two simulation schemes are adopted. For long-time program/erase characteristics (time scale of msec), we applied the quasi-steady state method, combining the steady state DC calculation and the sequential transient calculation, that is, the voltage of electrodes are ramped by DC calculation but the tunneling currents for programming/erasing operations are transiently calculated as shown in Fig.3.

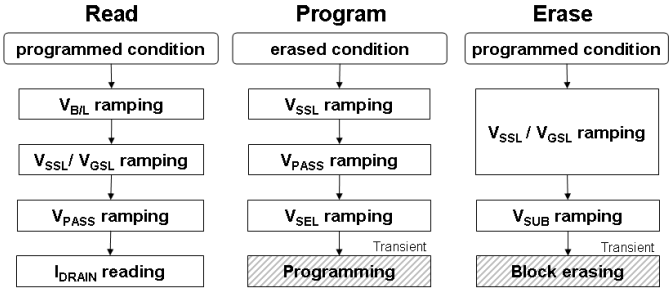



Figure 3. Bias schemes for the read/program/erase NAND operations in the quasi-steady state method.

On the other hand, short-time NAND device characteristics (time scale of μsec) such as self-boosting (SB) and local self-boosting (LSB), prevailing techniques to suppress program disturb in unselected B/Ls [6], are simulated using the fully-transient method, in which the electric pulses of trapezoidal wave are applied to the entire row of wordlines (W/Ls) and string select line (SSL) simultaneously as shown in Fig.4.

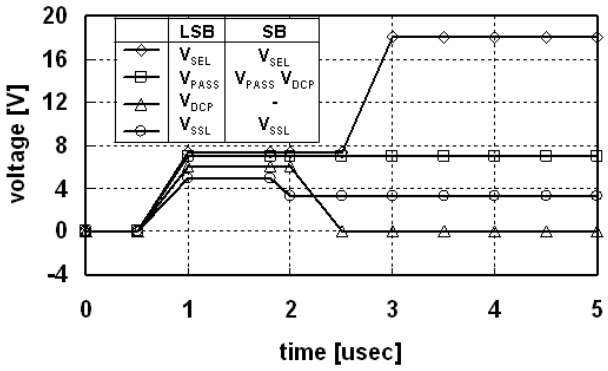



Figure 4. Pulse waves applied for the SB and LSB simulations.

To overcome convergence problem caused by many floating regions within a NAND string, we assigned a specific electrode boundary condition to every floating region, i.e. the charge boundary condition for the floating gate region and the floating potential boundary for the source/drain regions of every cell transistor.

## III. RESULTS AND DISCUSSION

Based on the above-mentioned simulation methodology, full 3D simulations of an 8-cell NAND string are carried out. Fig.5 shows the read/program/erase characteristics in the 8-cell NAND string structure simulated with the device simulator

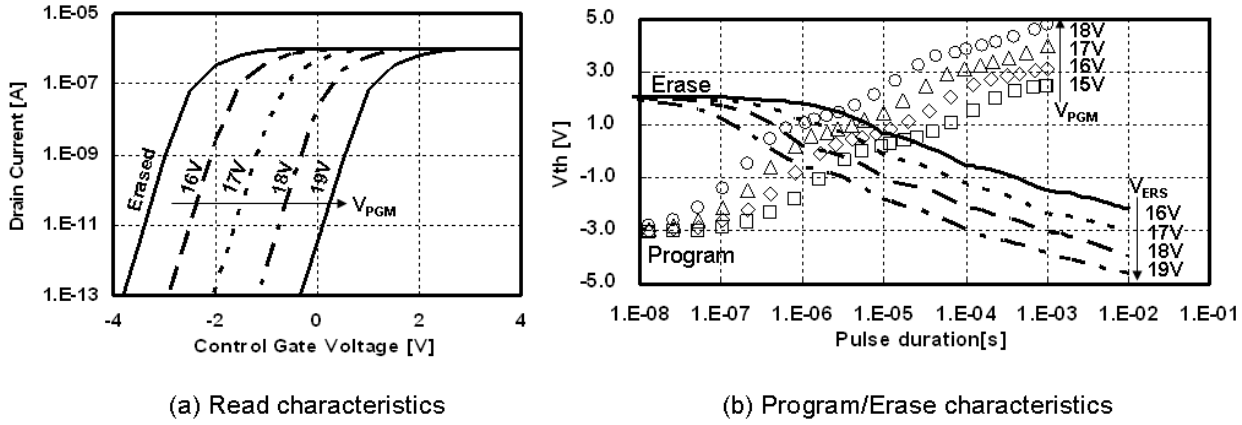



Figure 5. Simulated (a) read characteristics and (b) program/erase characteristics.

(HyDeLEOS) using the quasi-steady state method. Fig.5(a) shows the $I_{DRAIN}$-$V_{CG}$ curves for the erased condition and the followed programmed conditions at the programming voltage ($V_{PGM}$) of 16V/17V/18V/19V, and Fig.5(b) shows the program characteristics for $V_{PGM}$ of 15V/16V/17V/18V, and erase characteristics for erasing voltage ($V_{ERS}$) of 16V/17V/18V/19V. The threshold voltage ($V_{TH}$) variation of a unit cell transistor depending on floating gate charge ($Q_{FG}$) is formulated and utilized for the conversion of time-dependent $Q_{FG}$ curve to time-dependent $V_{TH}$ curve for the program/erase simulation. The conversion equation is obtained from the fitting curve as shown in Fig.6. The sting-level potential, electron density, and tunneling current distributions, simulated for (a) the programmed and (b) the erased condition, are shown in Fig.7, respectively. Both selective programming for program operation and block erasure for erase operation are successfully demonstrated.

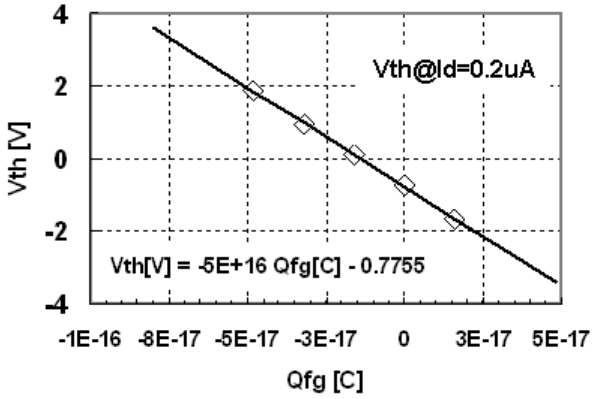



Figure 6. Floating gate charge (Qfg) versus threshold voltage (Vth) curve. Conversion euquation is obtained by linear fitting of simulation data.

The states-of-the-art multi-level cell (MLC) NAND flash

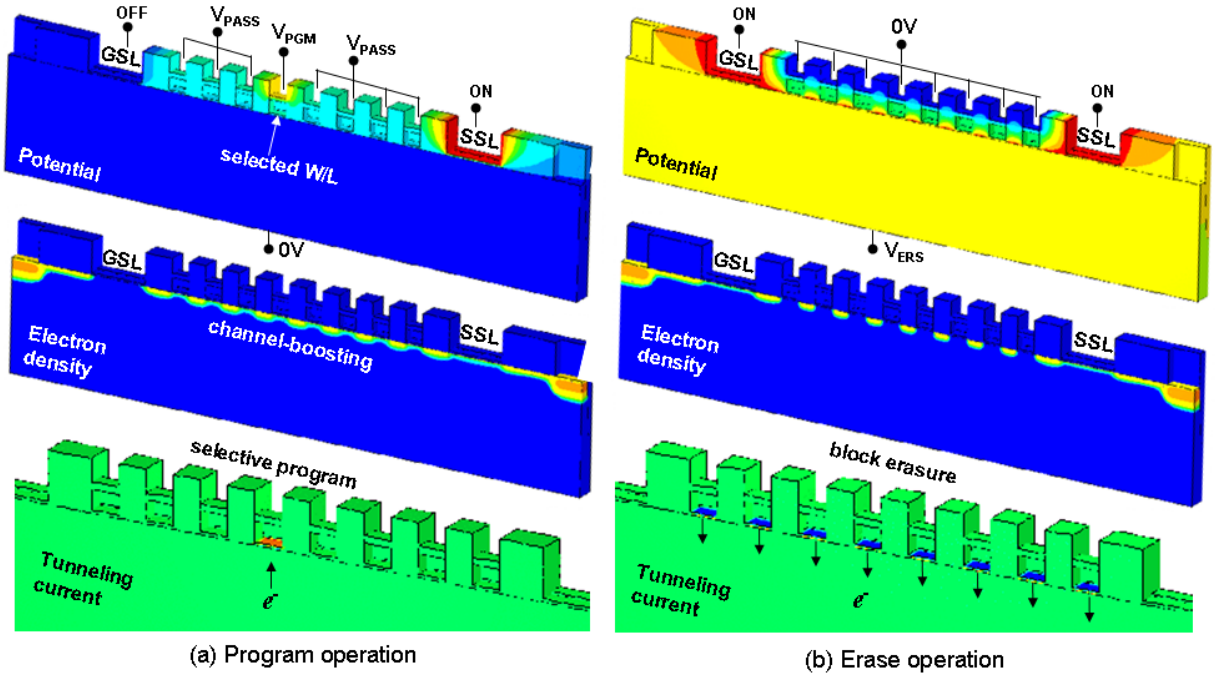



Figure 7. Simulated potential/electron density/tunneling current distributions for (a) program operation and (b) erase operation.

device requires a high $V_{PGM}$ to cover a wide range of $V_{TH}$ levels, which demands high $V_{PASS}$ to suppress program disturb in the unselected B/Ls. But, too high $V_{PASS}$ causes another problem such as $V_{PASS}$ disturb. To overcome this problem, LSB scheme is introduced. LSB localizes the effect of high $V_{PGM}$ to the boosted channel of the selected W/L by applying $V_{DCP}$ of 0V, rather than $V_{PASS}$, to the W/Ls adjacent to the selected W/L.

To confirm the applicability of our simulation methodology to the design optimization of NAND boosting scheme, fully transient device simulations are carried out in string level. The typical pulse waves, as shown in Fig.4, for SB and LSB schemes are applied to the entire row of W/Ls and SSL. Fig.8 shows the effect of boosting scheme on the electron density distributions in the selected B/L and in the unselected B/Ls, which can be explained as follow;

- At the initial stage, only the channel of selected W/L is inverted (erased condition), but those of other unselected W/Ls are not inverted (programmed condition), which depends on background pattern.
- At 1μs, all the channels are inverted by applying $V_{PASS}$ (7V) and $V_{SSL}$ (5V) and electrically connected to B/L. There is a voltage drop as much as the threshold voltage of SSL ($V_{TH,SSL}$) so that all the inverted channels are pre-charged to $V_{B/L}$-$V_{TH,SSL}$. (channel boosting)
- At 2μs, in both SB and LSB schemes, $V_{SSL}$ becomes equal to $V_{B/L}$, so that the boosted channel is disconnected from B/L in the unselected B/L (mark ① in Fig.8) but still connected in the selected B/L (②).
- At 3μs, in SB scheme, the boosted channel of the selected W/L is still electrically connected to those of other W/Ls (③), but becomes isolated in LSB scheme (④) as $V_{DCP}$ is set to 0V. That is, by adopting LSB scheme, we can localize the capacitive coupling effect of high $V_{PGM}$ to the channel of the selected W/L.

The program inhibition condition in the unselected B/Ls is obtained by the capacitive coupling between the pass gates ($V_{PASS}$) and the boosted channel (floating condition). And, it is one of the most critical issues in designing NAND flash device to sustain its inhibited channel potential to prevent $V_{PGM}$ disturb. For this purpose, it is essential to suppress the junction leakage from the boosted channel to the p-well substrate over the entire string. Consequently, the design optimization based on an elaborate TCAD simulation in string level is mandatory for the efficient development of sub-60nm NAND flash device.

## IV. CONCLUSIONS

The read/program/erase characteristics of a typical 60nm NAND flash device are successfully simulated using the quasi-steady state method. We also succeeded in the fully transient simulation of SB/LSB schemes in string-level, which indicates the potential for optimizing the boosting scheme of NAND flash device with our string-level simulation methodology.


## ACKNOWLEDGMENT

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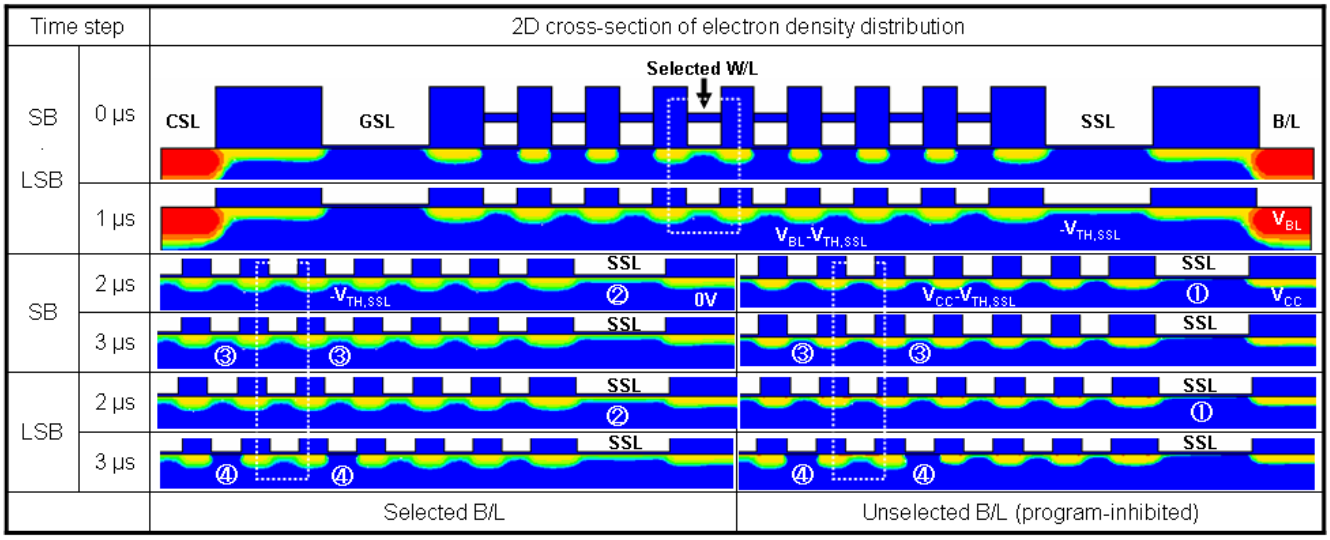


Figure 8. Fully transient simulation results of SB and LSB schemes for the selected B/L and the unselected B/Ls.