Compact Double-Gate MOSFET Model Correctly Predicting Volume-Inversion Effects

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Abstract

The compact double-gate MOSFET model HiSIM-DG considering the volume inversion effects is developed solving the Poisson equation iteratively including bulk charge. The developed model reproduces the bias dependence of not only the surface but also the center potential of the silicon layer. The model proves accurate dependence of silicon layer thickness in comparison to the 2 dimensional device simulation results. It is observed that the volume inversion effect prevents devices from performance degradation for a reduction of device sizes.

1 Introduction

The Double-Gate MOSFET (DG-MOSFET) shown in Fig. 1a is considered to be the most promising candidate for the next generation device structure beyond 45nm node. The reason is its drastic reduction of short-channel effects due to a reduced silicon-layer thickness T_{si}. The physical origin causing smaller short-channel effects is the volume inversion effect, which results from the potential increase in the middle of the silicon layer as illustrated in Fig. 1b. However, other problems, such as the increase of parasitic contributions and the influence of the technology variations, occur and are intensively studied [1, 2].

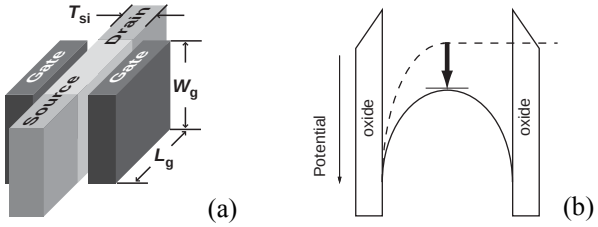

Figure 1: Schematic of the double-gate MOSFET and its potential distribution. The dashed line is that of a bulk MOSFET.

Another question concerns circuitry aspects, namely whether the DG-MOSFET can provide a solution to prevent circuit performance degradation due to the inevitable device size reduction. Our aim here is to investigate these aspects. For this purpose we have developed the compact DG-MOSFET model HiSIM-DG that includes the potential distribution perpendicular to the channel, overcoming the restrictions of the conventional charge sheet approximation for the carrier density. This innovation is a prerequisite for accurately including the volume inversion effect, which is the dominant new feature of the DG-MOSFET

2 Model Description

Most previously developed DG-MOSFET models are based on the Taur approximation [3-5], namely, that the Poisson equation is reduced to an analytical form by neglecting the bulk charge. To investigate the DG-MOSFET advantages for any technology generation, we have developed a model including the bulk charge contribution explicitly for the first time. The major quantum effect is considered as an increase of the effective oxide thickness. The calculated potential distribution is compared for various bias conditions and different device structures in Figs. 2-3 for T_{si}=10nm and the substrate impurity concentration N_{sub} of 1×10^{16}cm^{-3}.

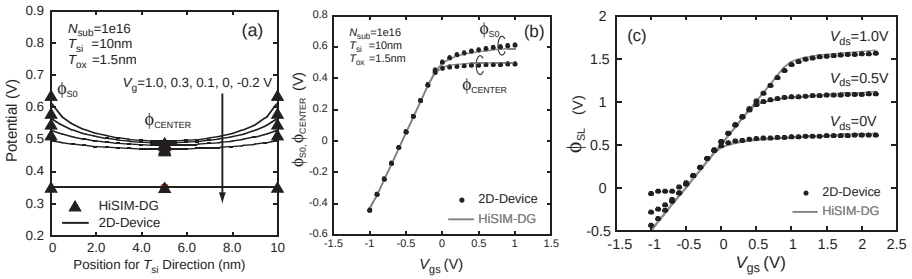

Figure 2: Comparison of calculated potential values with HiSIM-DG and those with a 2D-device simulator; (a) potential distribution perpendicular to the channel, (b) potential values at the surface and the middle of the silicon layer, (c) the potential value at the drain side ϕ_{SL} .

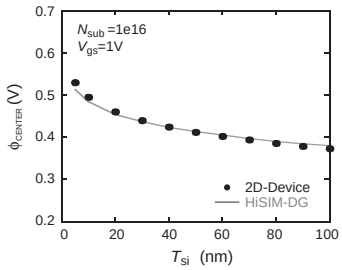

Figure 3: Calculated potential values in the middle of the silicon layer with HiSIM-DG as a function of T_{si} are compared with those obtained with a 2D-device simulator.

3 Analysis of The Volume Inversion

The volume inversion effect prevents the thresh-old voltage from rolling off as L_g reduces as shown in Fig 4 [6]. The effect on the surface potential is illustrated in Fig. 5. A potential shift for smaller gate source voltage (V_{gs}) is observed, which is enhanced for larger substrate impurity concentration N_{sub}. This effect is most pronounced around the threshold condition. The potential modification due to the volume inversion effect influences the capacitances as well, which is verified in Fig. 6. The smoother increase of the capacitance as a function of V_{gs} is a result of the volume inversion.

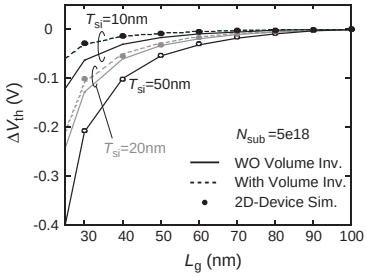

Figure 4: Influence of the volume inversion effect on the threshold voltage shift ΔV_{th} ($=V_{th}(\text{long})-V_{th}(L_g)$) for various T_{si} thicknesses. To enhance the effect N_{sub} is fixed to $5\times10^{18}\text{cm}^{-3}$.

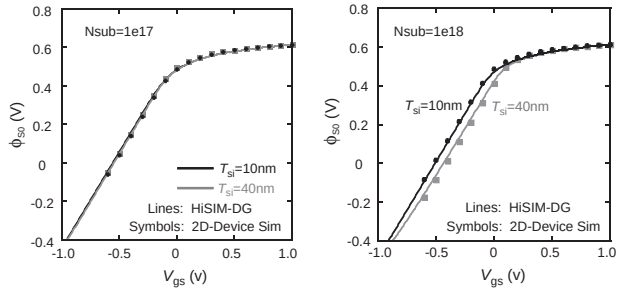

Figure 5: Comparison of calculated surface potential ϕ_{S0} for two different T_{si} values. When reducing N_{sub} the difference becomes nondetectable.

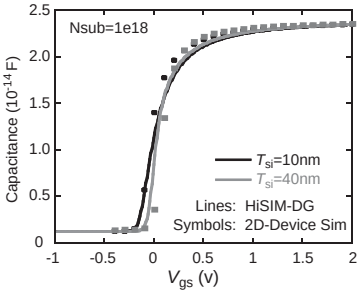

Figure 6: Influence of the volume inversion effect on capacitance. The effect is enhanced for T_{si}=10nm and negligible for T_{si}=40nm. For comparison 2D-device simulation results are depicted together. The influence is enhanced before strong inversion is established.

4 Circuit Performance

Fig. 7 compares the switching performance of the DG-MOSFET for different T_{si} thickness. For the simulation, the carrier mobility is approximated to be a constant, so that the effect of the potential distribution change due to the volume inversion effect can be extracted more clearly. An obvious feature of the DG-MOSFET is that the current is reduced as T_{si} becomes smaller. However, the potential gradient into the substrate is drastically reduced, which results in a larger average carrier distance from the surface, shown in Fig. 8, and is expected to suppress the carrier scattering leading to an effective current increase. This has to be investigated with real measurements.

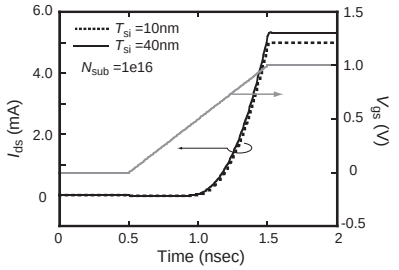

Figure 7: Switching characteristics of the DG-MOSFET with two different T_{si} thicknesses.

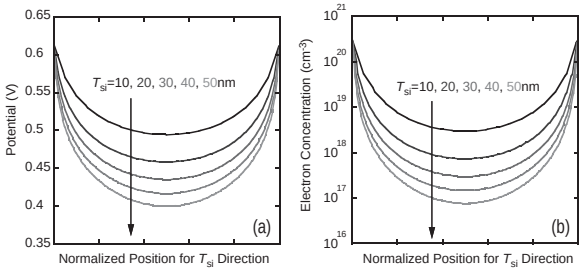

Figure 8: Potential (a) and electron (b) distribution for diffrent T_{si} .

5 Conclusion

We have developed the Double-Gate MOSFET model HiSIM-DG. With this model, the volume inversion effect is investigated. If the mobility is approximated to be constant, the drain current reduces as T_{si} reduces. On the other hand, the T_{si} reduction causes a reduction of the potential gradient perpendicular to the channel, which is expected to result in a mobility and therefore also a current increase, enabling a continued performance enhancement for the application to integrated circuits.

References

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