Compact Modeling of Phase-Change Memories

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Abstract

A compact model for a phase-change memory cell is presented and confirmed by measurement. The model reproduces the non-linear current-voltage behavior of both set and reset states. The temperature-dependent crystallization and amorphization of the phase-change layer are taken into account in order to express resistance changes between set and reset states. The heat of fusion is also taken into account in the calculation of the amorphization.

1 Introduction

Chalcogenide-based phase-change memory is one of the most promising candidates for the next generation non-volatile memory[1]. An accurate compact model for the phase-change memory cell is a prerequisite in the process of designing circuits. Several attempts have been made to model the resistance switching caused by phase-change between amorphous and crystalline states[2][3][4][5]. In these models, however, temperature-dependent crystallization[6][7][8] is not fully taken accounted for.
In this paper, a compact model for the phase-change memory cell is proposed considering the temperature-dependent crystallization and amorphization. The heat of fusion is also taken into account in the calculation of the amorphization.

2 Modeling

The current-voltage characteristics and the temperature of the memory cell are expressed by the equivalent circuits shown in Fig. 1. The amorphous volume, V_a in the phase-change layer having thickness t_gst is assumed to vary between zero and $V_\mathrm{amax} \equiv (2/3)\pi t_\mathrm{gst}^3$ due to amorphization and crystallization. The amorphous ratio, C_a is defined as $C_\mathrm{a} \equiv V_\mathrm{a}/V_\mathrm{amax}$.
The current through the phase-change layer is expressed as $I_\mathrm{gst} = (1-F)I_\mathrm{off} + FI_\mathrm{on}$ using the variable F[5]. The variable, F asymptotically approaches 1 if I_gst is equal to or greater than the threshold current, I_t in order to express the threshold switching, which is shown in Fig. 6. The current before turn-on, I_off is expressed by $I_\mathrm{off} = V_0 \sinh(V_\mathrm{gst}/V_0)/R_0$ [9], using the low-field resistance, R_0 and the nonlinearity parameter, V_0. Both R_0 and V_0 are dependent upon C_a. The low-field resistance, R_0 is tentatively expressed by logarithmic interpolation between a minimum, R_0min and a maximum, R_0max. This is because the detailed configuration of amorphous regions, of which three possibilities are schematically shown in Fig. 2, is not fully understood in the real phase-change memory device. The logarithmic interpolation locates between two extremes,

the serial and parallel cases, as shown in Fig. 3[10]. The current after turn-on, I_{on} is expressed using the formula for I_{off} except that neither R_0 nor V_0 is dependent upon C_a. The temperatures at the top and the bottom of the phase-change layer are expressed by the thermal equivalent circuit which consists of the electric power, P_t, the thermal resistances, R_{tt}, R_{tgst} and R_{tb} and the thermal capacitance, C_t as shown in Fig. 1 (c). The temperature at the amorphous-crystal interface, T_a is estimated to be $T_a = (1-C_a)T_b + C_aT_t$, as shown in Fig. 4.

The amorphous volume, V_a decreases when T_a is less than the melting point, T_m because of the crystallization of the amorphous region as shown by Case 1 in Fig. 4. Crystallization is described by the nucleation and crystal growth model[6]. The decrease rate of the amorphous volume, V_a by nucleation is given by $P_nV_nV_a/V_m$, where P_n is the nucleation rate, V_n is the volume of a nucleus and V_m is the volume of a monomer[11] of the phase-change material. The decrease rate of V_a by crystal growth is S_av_g, where S_a is the area of amorphous-crystal interface and v_g is the crystal growth velocity. The rate equation of V_a is, therefore, $dV_a/dt = -\left(P_nV_nV_a/V_m + S_av_g\right)$ when $T_a < T_m$. Both P_n and v_g are dependent upon the temperature, T_a as shown in Fig. 5. The nucleus volume, V_n is assumed to be the critical volume of nucleation[11], and is evaluated using the temperature at which P_n is at its maximum. The area, S_a is approximated as $(1/2)4\pi r_a^2$ assuming a hemispheric amorphous region with the radius, r_a and the volume, $V_a = (1/2)(4/3)\pi r_a^3$.

The amorphous volume, V_a increases when $T_a \geq T_m$, because part of the crystal region melts and changes into its amorphous state as shown by Case 2 in Fig. 4. Assuming that the liquid phase is amorphous, the rate equation of V_a is expressed by $dV_a/dt = (T_a - T_m)/(R_t\Delta h_1)$ when $T_a \geq T_m$, where $R_t \equiv ((R_{tgst} + R_{tt})^{-1} + R_{tb}^{-1})^{-1}$ is the total thermal resistance and Δh_1 is the heat of fusion[6].

3 Results and Discussion

The compact model of phase-change memory described in the previous section was implemented using Verilog-A[12] hardware description language.

The simulated curve of a logarithmic current ramp is compared with the measured curve in Fig. 6. The crystallization occurs during the upside of the ramp in both the measurement and simulation, resulting in hysteresis.

The resistance of the memory cell after applying the reset pulse is shown in Fig. 7 (a). As the word-line voltage increases, the resistance rises due to amorphization.

Finally, the resistance after applying the set pulse is shown in Fig. 7 (b). As the word-line voltage increases, the resistance declines due to crystallization.

4 Conclusion

A compact model for a phase-change memory cell was presented and confirmed by measurement. The temperature-dependent nucleation and crystal growth were taken into account in the calculation of the crystallization. The heat of fusion was also taken into account in the calculation of the amorphization.

Acknowledgments

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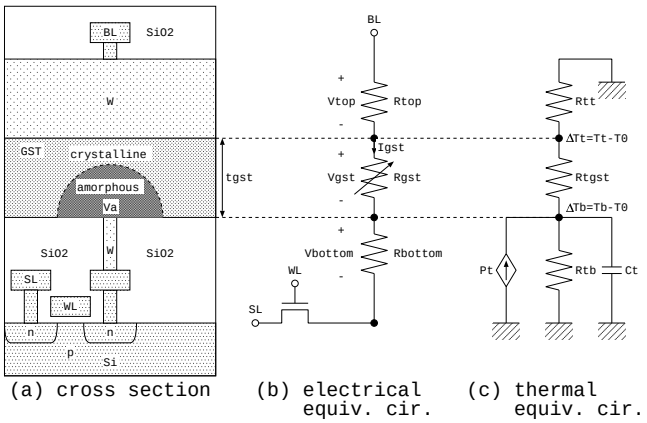

Figure 1: Schematic cross section, electrical and thermal equivalent circuits of a phase-change memory cell. t_{gst} is the thickness of the phase-change layer, V_{a} is the amorphous volume, $P_{\mathrm{t}} \equiv (V_{\mathrm{gst}} + V_{\mathrm{bottom}})I_{\mathrm{gst}}$ is the electric power and T_0 is the ambient temperature.

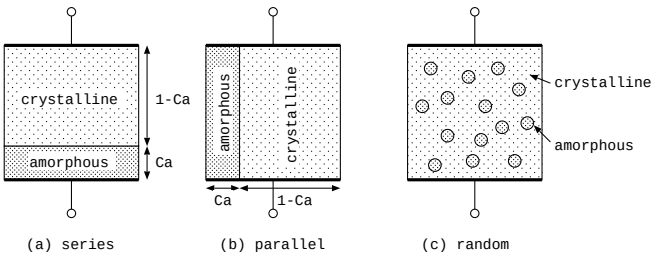

Figure 2: Some possible configurations of amorphous regions in crystalline medium.

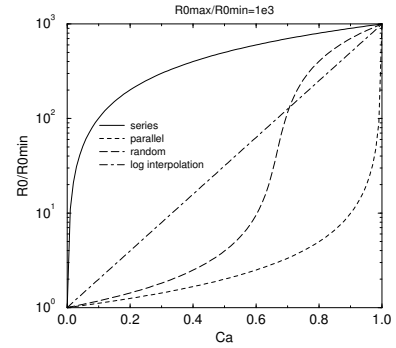

Figure 3: The low-field resistance as a function of the amorphous ratio. $R_{0\min}$ and $R_{0\max}$ are the resistances at $C_\mathrm{a} = 0$ and 1, respectively. The configurations are shown in Fig. 2.

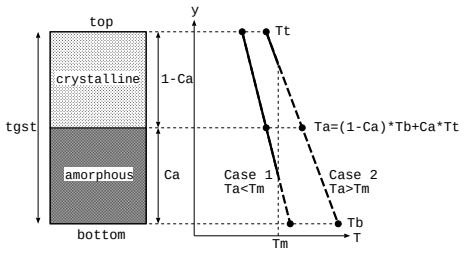

Figure 4: Temperature distribution in the phase-change layer.

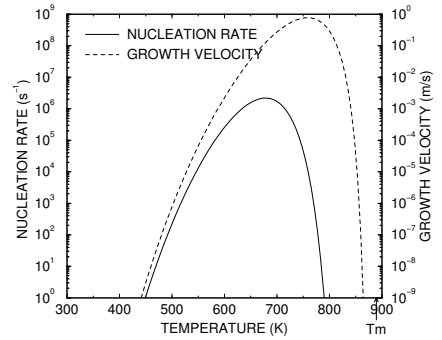

Figure 5: Nucleation rate and crystal growth velocity[6]. $T_\mathrm{m} = 889\mathrm{K}$ is the melting point of the phase-change layer.

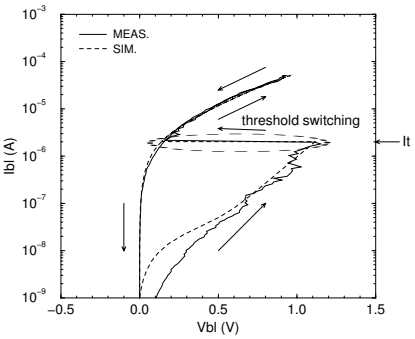

Figure 6: Measured and simulated current-voltage characteristics of the memory cell. I_t is the threshold current.

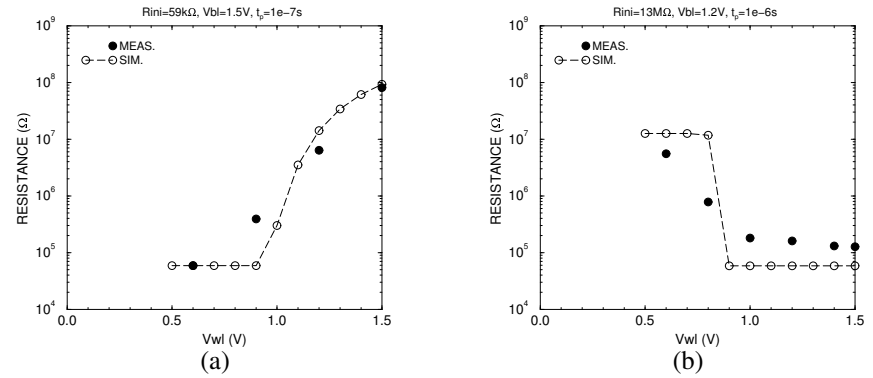

Figure 7: Measured and simulated cell resistances as a function of the program word-line voltage. R_ini is the initial resistance, V_bl is the program bit-line voltage and t_p is the program pulse width. (a) Reset operation, (b) Set operation.