Simulation Study of Multiple FIN FinFET Design for 32nm Technology Node and Beyond

Xinlin Wang, Andres Bryant†, Omer Dokumaci, Phil Oldiges and Wilfried Haensch*

IBM Semiconductor Research and Development Center
Systems and Technology Group, Hopewell Junction, NY 12533
†System and Technology Group, Essex Junction, VT, 05452
*Research Division, IBM T.J. Watson Research Center
Email: xinlinw@us.ibm.com Phone:(845)894-4740 Fax:(845)892-6483

Abstract

In this work, we investigate multiple FIN FinFET source/drain designs to reduce series resistance and source/drain-to-gate capacitance. The tradeoffs between the increased parasitic capacitance and reduced parasitic resistance are explored using 3D device simulations.

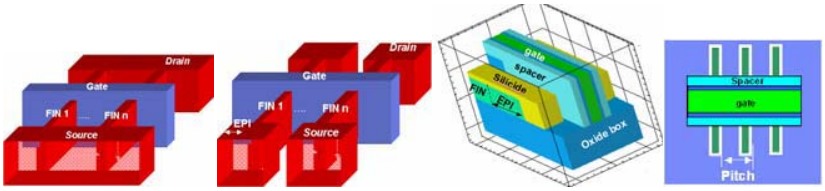
1 Introduction

Multigate MOSFETs such as FinFET [1,2] or tri-gate [3] devices are considered as potential candidates for 32nm node technology and beyond. The primary FinFET advantage is its improved short channel effect (SCE) control, which offers performance benefits and enables further device scaling. However, the source/drain structure is a critical aspect of thin-body FinFET design that is impacted by the choice of FIN pitch. Epitaxy (Epi) layer growth in the source/drain region is needed to reduce parasitic resistance (Rext), but it also raises parasitic overlap capacitance (Cov or Cgs/Cgd). This high resistance and capacitance of the FinFET can be significant detractors to the overall device performance. In this simulation work, we focus on multiple FIN source/drain design to optimize Rext and Cov.

2 Simulation and Characterization Methodology

The drift-diffusion equations are solved for 3D FinFET structures as shown in Fig 1. One is an un-merged FIN case (Fig. 1a) and the other one is a merged FIN case (Fig. 1b) as the Epi layer is thick enough to fill the gap between neighboring FINs. For the first case, sidewall and top source/drain (S/D) areas are silicided as shown in Fig 1c; for the merged FIN case, only the top S/D areas are silicided. FIELDAY [4] was used to perform the device simulations. The external resistance of the device is extracted from plots of Ron vs. Leff [5] and the gate-to-S/D (Cgs) or overlap capacitance is obtained by A.C. small-signal analysis [6]. In order to accurately model the external resistance variation due to FinFET S/D structure changes, a calibrated distributed contact model is applied in this work. Width of the FIN is 15nm or 20nm, and pitch (as defined in Fig. 1d) varies from 40nm to 120nm. FinFET height, spacer thickness,

Epi layer thickness and silicide thickness are also varied in the simulations to study their sensitivity. It is assumed that nominal channel length is 28nm.



(a) (b) (c) (d)

Fig. 1 FinFET structures. (a) A multiple FIN FinFET with merged FIN. (b) A multiple FIN FinFET with un-merged FIN. (c) Simulated 3D half structure of FinFET with Epi in the source/drain (d) top-view of simulated FinFET structure. pitch is defined as a distance between the neighboring FINs.

3 Simulation Results and Discussions

Figs. 2(a-c) show the SCE control of un-doped body FinFETs with different FIN thickness. When the FIN thickness is less than 13nm, thin body FinFETs exhibit superior SCE control when the channel length is scaled down to 25nm.

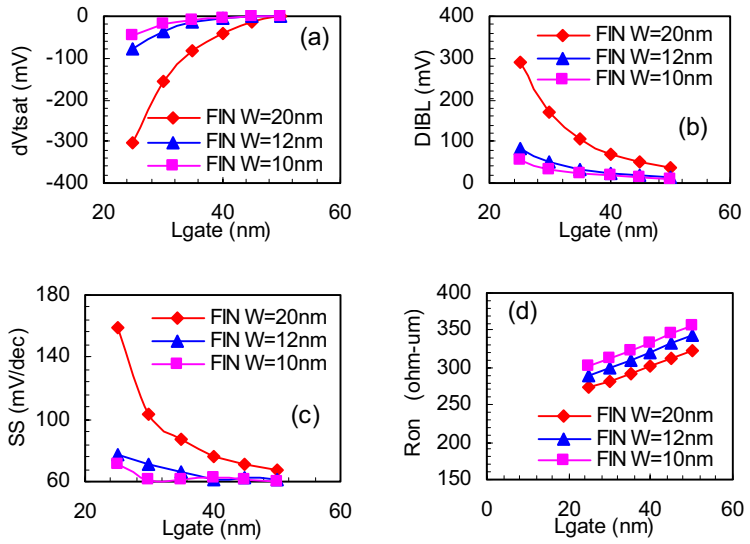


Fig. 2 (a) Vt-roll off (b) DIBL (c) Sub-threshold swing (SS) (d) Ron vs. Lgate for un-doped FinFETs with different FIN width (W).

However, a thinner FIN increases external resistance (Rext) as shown in Fig. 2d, which degrades drive current. So S/D design is one of the key FinFET device design challenges. Firstly We focus on a merged vs. an unmerged case at 80nm pitch, as illustrated in Fig. 1(a,b). Figs 3 and 4 show the spacer thickness and Epi thickness

impact on Rext and Cov for the silicided unmerged S/D FinFET structure. Reducing the spacer thickness yields a Rext benefit and Cov penalty, but the Rext reduction is limited while Cov continues to increase as spacer thickness decreases below 25nm. A spacer thickness of 25nm appears to be optimal.

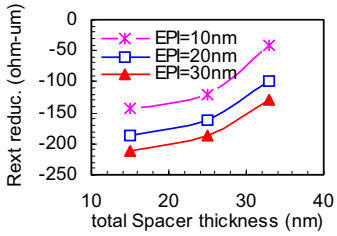


Fig. 3 Rext reduction for un-merged FIN cases.

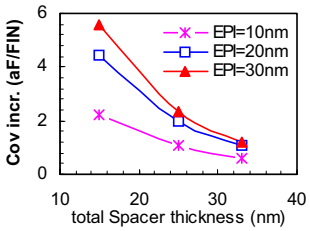


Fig. 4 Cov increase for un-merged FIN cases

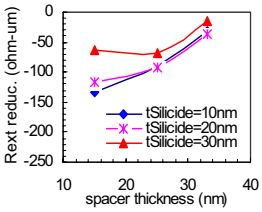


Fig. 5 Rext reduction for merged FIN cases.

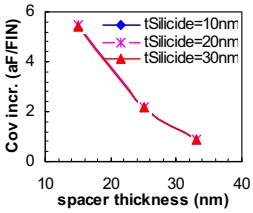


Fig. 6 Cov for merged FIN cases.

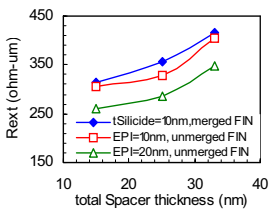


Fig. 7 Rext (merged vs. un-merged FIN cases).

For the merged S/D FinFET case, silicide replaces part of the original Epi surface. Fig. 5 shows that thicker silicide increases Rext. Cov is not affected by silicide thickness as shown in Fig. 6, but it is higher for the merged case due to thicker Epi. Fig. 7 shows that Rext is slightly higher for the merged case. So, un-merged S/D FINs with silicided sidewalls is the optimum case for minimum Rext and Cov but large pitch is required.

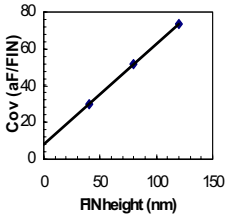


Fig. 8 Cov vs. FIN height. FinFET w=15nm, pitch=80nm, tEpi=20nm, FIN is un-merged. Cfringe=8aF.

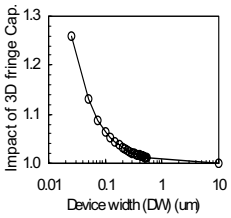
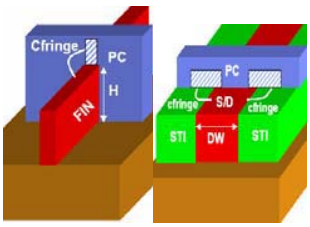


Fig. 9 Impact of 3D fringe Cap calculated as $\frac{C(2D)\times DW + Cfringe(3D)}{C(2D)\times DW}$



(a) FinFET (b) Planar device
Fig. 10 (a) FinFET has top and bottom 3D fringe capacitance. (b) Planar has left and right Cfringe.

In Fig. 8, we extracted the 3-D fringing capacitances at the bottom and top of FINs by plotting Cgs (or Cov) vs. FIN height. We can see that Cgs is proportional to FIN

height. Therefore, the fringe capacitance is the capacitance when the curve is extended back to FIN height=0. The fringe capacitance is close to 1/3 of the total Cgs for a 40nm high FIN at an 80nm pitch. And it becomes more dominant as FIN height is reduced to accommodate tighter pitch.

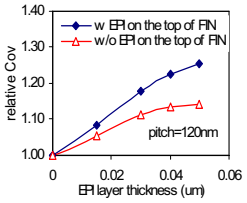


Fig. 11 Cov vs. Epi layer thickness. Pitch=120nm, w=20nm, FIN height=75nm.

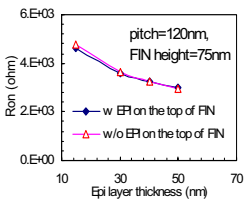


Fig. 12 Ron vs. Epi layer thickness. Growing Epi on the top of FIN does not change Ron.

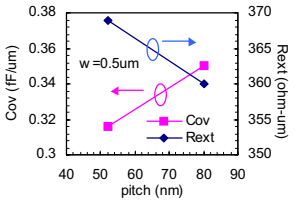


Fig. 13 Cov and Rext vs. Pitch=52nm with 26nm FIN height and pitch=80nm with 40nm FIIN height.

Figs 11 and 12 show that growing Epi on the top of the FIN adds more parasitic capacitance without achieving Rext reduction, which suggests that leaving a mask on the top of the FIN during Epi is preferred to eliminate raised source/drain vertical Epi grow. When the FIN height is scaled proportionally to the pitch scaling, we simulated case with pitch=52nm and FIN height= 26nm, in which only merged FINs fit. Fig. 13 shows that pitch scaling slightly increases Rext, while reducing Cov.

4 Conclusions

Our results show that the primary FinFET advantage is its improved SCE, which provides performance benefit over PDSOI. The Source and Drain structure is a critical aspect of thin-body FinFET design that is impacted by the choice of FIN pitch. Epi is required to reduce Rext, but increases Cov. Unmerged S/D FIN with silicided sidewalls is the optimum case for minimum Rext and Cov, but larger Pitch is required. For the tight pitch, only merged FINs fit, but even with merged Fins, Cgs is reduced at tighter pitches with only a modest increase in Rs.

Acknowledgements

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