Validation of the Effect of Full Stress Tensor in Hole Transport in Strained 65nm-Node pMOSFETs

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Abstract

We have developed a system consisting of a full-3D process simulator for stress calculation and k·p band calculation that takes into account the subband structure. Our simulations are in good agreement with the experimental data of strained Si-pMOSFETs of 65nm technology devices. This system is a powerful tool to optimize device structures with all stress components.

1 Introduction

Process-induced strain has become one of the principal technology boosters for improving MOSFET drivability. In state-of-the-art devices with a stress liner such as Contact Etch Stop Layer (CESL), the stress distribution is nonuniform as shown in Fig. 1. Therefore, it is necessary to optimize the device structure with the support of theoretical analysis.

In this study, we calculated a stress tensor through a full wafer process of strained Si-pMOSFETs of 65nm technology devices using a full-3D process simulator[1]. Looking at Fig. 1, 4, the z-axis stress which is perpendicular to the inversion layer is large, and the mobility enhancement has nonlinearity, so it is difficult to optimize device structures with only the piezo coefficient. Therefore, we need a mobility calculation which is able to take into account all stress components. This system consists of three blocks: at first, it calculates a full stress tensor, and the next block transform it to a strain tensor, finally a hole mobility is obtained with k·p band structure calculation (Fig. 2).

2 Calculation Method

A stress tensor is extracted by full-3D process simulation through the full wafer processes. As the value of a stress tensor strongly depends on film stress, it is important to give the accurate value as much as possible. All extracted stress components are transformed to the strain tensor as an input for k·p band calculation.

Numerical simulation is essential especially for the p-type channel design due to the complicated valence band structure. The subband structures for two dimensional hole states have been obtained by solving the wave equation based on the 6×6 Luttinger-Kohn Hamiltonian. The effect of the strain was taken into account according to the theory of Bir-Pikus[2]. The values for the Luttinger parameters, and Bir-Pikus deformation potentials were taken from the parameters as listed in Table 1[3]. In this study, the mobility has been numerically computed from the realistic subband structure using the following equation:

$$\mu_0 = \frac{\sum_{n\boldsymbol{k}} e\tau(n,\boldsymbol{k}) v_\theta^2(n,\boldsymbol{k})\left(-\frac{\partial f_0}{\partial E}\right)}{\sum_{n\boldsymbol{k}} f_0(E)} \tag{1}$$

where $\tau(n,\boldsymbol{k})$ is the momentum relaxation time for the hole with the in-plane wave vector $\boldsymbol{k}$ in the subband index n, $v_\theta^2(n,\boldsymbol{k})$ is the group velocity component along the θ-direction, and $f_0(E)$ is the equilibrium Fermi function for the hole of energy $E(n\boldsymbol{k})$[4][5].

3 Discussion

The results of the comparison between our simulations and the 4-point-bending method measurements for the <110> and <100> are shown in Fig. 3. Our simulation is an excellent match for the experimental data for both the longitudinal and transverse bending direction. Fig. 4 shows the strain dependence of the mobility enhancement in a large strain range for the <110> and <100>. Observed large nonlinearity infers the significance of the accuracy of the stress calculation because the stress distribution of the real device structure is quite nonuniform. Therefore, we have calculated all the stress components using the full-3D process simulator and compared it with experimental data.

Fig. 5 shows the tensile stress liner thickness dependence of the mobility enhancement of the short channel transistor (Lg=50nm). Tensile stress liner degrades the mobility of <110>, while the mobility of <100> is enhanced with a high tensile stress over a few 100MPa. Since it is well known that the tensile stress liner works well for nMOS drivability improvement, the dual stress liner to boost the mobility of both the electron and the hole is not necessary in <100>. However, the effect of the compressive stress liner looks attractive in both channel directions, especially in <110> (Fig. 6).

Fig. 7 shows the gate length dependence of the hole mobility with a compressive and tensile stress liner. The mobility increases with a shorter gate length in reflection with the increasing stress in the channel. On the other hand, the gate length dependence of the mobility enhancement, which is defined as the ratio of mobility with the compressive liner to that with the tensile one, shows a peak around Lg=50nm as shown in Fig. 8. The simple calculation using the bulk piezo coefficient indicates a tendency to be saturated but does not show any peak. Furthermore, it underestimates the enhancement magnitude over the entire gate length. The calculation based on k·p band structure is in good agreement with the experimental data, although it fails to reproduce the decline of the mobility enhancement below Lg=50nm. A short gate transistor has a high concentration of impurity in the channel, and the channel resistance is lower. Therefore, it is concluded that gate length dependent stress distribution affects the mobility enhancement characteristics of a short channel transistor, in addition to the stress independent impurity scattering limited mobility and the external resistance[6].

4 Conclusion

We have developed a powerful system which is able to optimize real device structures. Our simulations have been in good agreement with the experimental data and have been able to predict the transistor performance. Stress calculation plays an important role and full-3D stress calculation is necessary for the accuracy of performance prediction.

Acknowledgements

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References

[1] T. Uchida et al., SISPAD , 199, (2005).
[2] C. Y.-P. Wang, S. L. Chuang, Phys. Rev. B **46**, 4110 (1992).
[3] E. X. Wang, et al., IEEE Trans. ED. **53**, 1840 (2006).
[4] M. V. Fischetti, et al., J. Appl. Phys. **94**, 1079 (2003).
[5] M. Uchida, et al., SISPAD , 315 (2005).
[6] S. Suthram, et al., IEEE EDL , **28**, 58 (2007).

Table 1: Luttinger Parameters γ_1, γ_2, γ_3, and Bir-Pikus Parameter A, B, and D for silicon hole bands.

	Symbol	Value
Luttinger Parameter	γ_1	4.31
	γ_2	0.345
	γ_3	1.427
Bir-Pikus Parameter	A	2.1
	B	-1.6
	D	-2.7

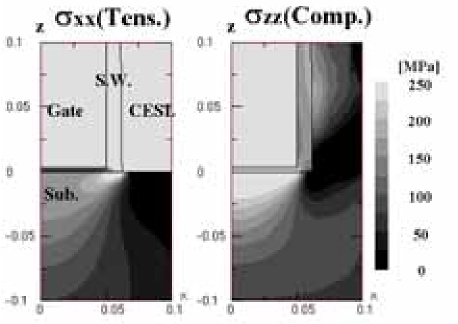

Figure 1: The stress distribution of nMOSFET with CESL. σ_{xx} (left figure) and σ_{zz} (right figure) have nonuniform distribution.

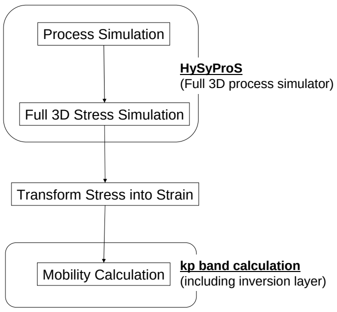

Figure 2: System flow from process simulation to mobility simulation.

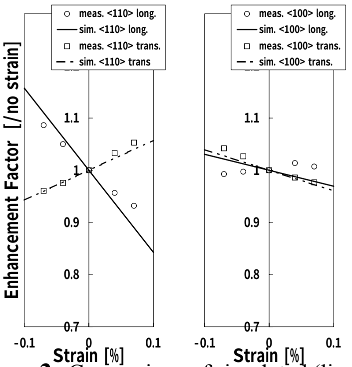

Figure 3: Comparison of simulated (lines) and 4-point bending measured (symbols) <110> and <100> strain dependence of hole mobility.

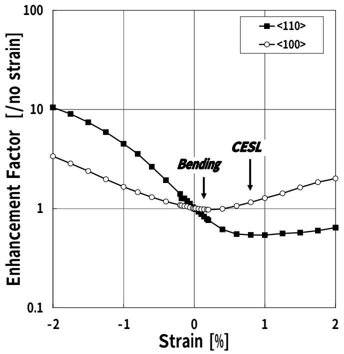

Figure 4: Enhancement of hole mobilities in <100> and <110> as a function of strain. The strain is along the channel direction.

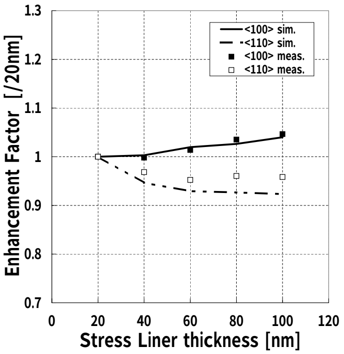

Figure 5: Tensile Stress Liner thickness dependence of mobility enhancement. The enhancement of the measured data is the transconductance in the linear region.

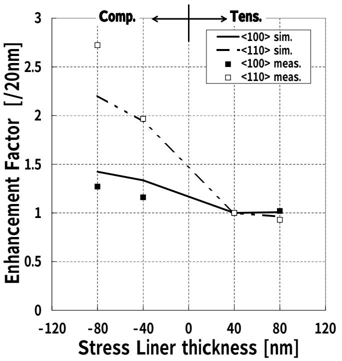

Figure 6: Stress Liner thickness dependence of mobility enhancement. The negative thickness represents compressive stress and the positive thickness represents tensile stress.

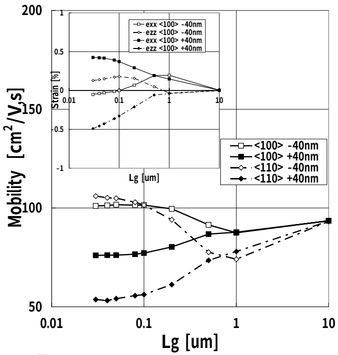

Figure 7: The gate length dependence of hole mobility and strain in <110> and <100> for compressive Stress Liner thickness 40nm versus tensile Stress Liner thickness 40nm.

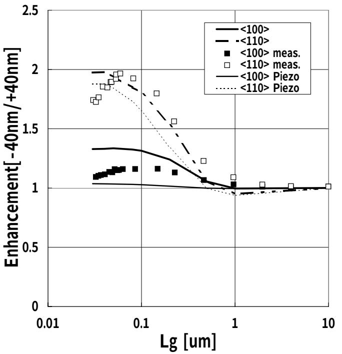

Figure 8: The gate length dependence of enhancement of hole mobility. The dashed lines show calculated enhancements with the bulk piezo coefficient