Modeling of the Leakage Current Distribution of 16M Stacked Single Crystal (SC)-like SOI pMOSFETs using Green's function method

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***Abstract*—An analytical leakage current model is proposed to explain the large magnitude and the broad variation of the leakage current found in the 16M stacked single crystal (SC)-like SOI transistors which have the re-crystallized amorphous-silicon body. This model shows that the parasitic BJT amplification effect should be considered in addition to the trap-assisted tunneling mechanism caused by a randomly located grain boundary and interface traps. Also, the leakage current distribution of the 16M stacked SC-like SOI transistors is analyzed and simulated by utilizing Green's function method.**

Keywords-component; stacked; single crystal(SC)-like; BJT-amplification; green's function)

I. INTRODUCTION

A novel inverter structure that has a stacked pMOSFET over an nMOSFET was recently proposed to reduce the cell area of the high density SRAM as shown in Figure 1 [1]. The pull-up pMOSFET is realized in the single crystal (SC)-like silicon region over the pull-down nMOSFET, where the inter layer dielectric (ILD) vertically separates the two devices from each other. As a result, the pMOSFET has similar electrical characteristics with the SOI devices that have the highly doped ($>10^{18}/cm^3$) floating silicon body. Although the proposed inverter structure has an advantage in the cell size, the magnitude and variation of the off-state current of the SC-like SOI pMOSFET are larger than those of the conventional bulk-silicon device due to the grain boundary (GB) and interface traps. Therefore, it is necessary to understand and model the leakage current mechanism of the proposed inverter to use it as a memory cell in the SRAM chip, where the noise margin is strongly dependent on the leakage current of the cell transistors.

II. MODELS AND DISCUSSION

At first, the trap-assisted tunneling (TAT) mechanism [2] is considered to be the main cause of the large leakage current in the SC-like SOI pMOSFET, since there are many interfacial traps between the SC-like silicon body and ILD. The GB in the SC-like silicon region makes the problem even more complicated. The GB is inevitable and its location in the silicon body is hard to control [1] when the amorphous-silicon film on the ILD is being crystallized. Therefore, the interface between the silicon body and ILD has many dangling bonds, which become the interface traps as depicted in Figure 2. In addition to the TAT, a current enhancement caused by the floating body effect [3][4] and parasitic bipolar junction transistor (BJT) is no more negligible [5][6]. As shown in Figure 2(a), the total off-current can be written as

$$I_{off} = I_{surf} + I_{GEN},$$

$$I_{GEN} = (I_{TAT} + I_{BBT})(1+\beta) \quad (1)$$

where I_{TAT} and I_{BBT} are the generation currents due to the TAT and the band to band tunneling (BBT), respectively ($I_{TAT} \gg I_{BBT}$). I_{GEN} is the total generation current including the BJT amplification effect, I_{surf} is the surface leakage current, and β is the bipolar current gain [8]. I_{TAT} +I_{BBT} in (1) is like I_{CBO} (the common base output current) in case of the base-opened BJT. Fig 3 shows the overall simulation procedure to obtain the leakage current distribution of 16M SRAM cells. Figure 4 shows that the total leakage current obtained from (1) and (4) with and without considering β. After obtaining a DC solution and then, we use the Green's functions $G_n(r)$ and $G_p(r)$, which are frequently used in the noise analysis, to obtain the generation current due to the TAT and BBT mechanisms as [7]

$$I_{GEN} = -\int_{\Omega} dr[R_{TAT}(r) + R_{BBT}(r)][G_n(r) + G_p(r)] \quad (2)$$

where Ω is the simulation domain, -$R_{TAT}(r)$ and -$R_{BBT}(r)$ are the net generation rates due to TAT and BBT, respectively.

Comparing (1) and (2), we can relate $I_{TAT}+I_{BBT}$ and $1+\beta$ with the net generation rates and Green's functions as

$$I_{TAT}+I_{BBT}=-\int_{\Omega} dr\left[R_{TAT}(r)+R_{BBT}(r)\right]\cdot q \qquad (3)$$

$$1+\beta=\left(G_n+G_p\right)/q \qquad (4)$$

By calculating $R_{TAT}(r)+R_{BBT}(r)$, we can extract the relation between the trap location and the magnitude of the leakage current. In particular, the magnitude of $R_{TAT}+R_{BBT}$ is largest when the trap locates at the depletion region of the drain terminal as shown in Figure 5(a). Figure 5(b) shows the response of the drain current due to the impulse noise source with a charge of $1.6\text{x}10^{-19}$C (q), which shows that the bipolar amplification effect is significant, and the corresponding amplification factor is uniform when the leakage source is located in the Si-body region under the channel. Figure 6(a) shows the calculated leakage current distribution of the 16M SRAM cell with the SC-like transistors and conventional bulk Si transistors together with the measured distribution of the 16M SC-like SRAM chip. Figure 6(b) shows the effect of trap density (N_t) on the leakage current distribution.

III. Conclusion

The stacked single crystal (SC)-like SOI load pMOS transistor on the ILD has been developed to reduce the cell area, and an analytic model to explain the leakage mechanism of the SC–like SOI pMOSFET is presented. From the comparison with the experiments, it has been shown that the amplification of the TAT generation current due to the parasitic BJT is the main cause of the large leakage current. The statistical distribution of the leakage current for 16M transistors caused by the random GB and interface traps is predicted by the Green's function method.

Acknowledgment

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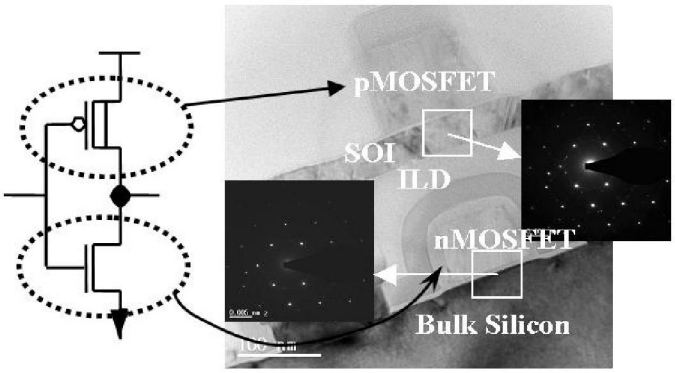

Figure 1. Electron diffraction patterns and TEM image of inverter with stacked SC-like SOI pMOSFET : L_{GATE} is 80nm and the SC-like Si-body thickness is 25nm.

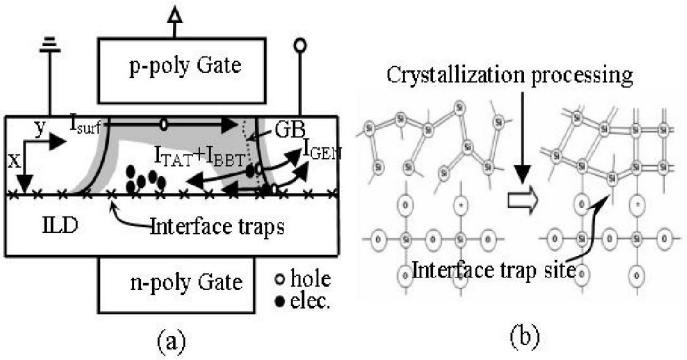

Figure 2. (a) Structure of SC-like SOI pMOSFET on ILD and components of leakage current, (b) Si-O bond structure between SC-like silicon body and ILD before and after crystallization.

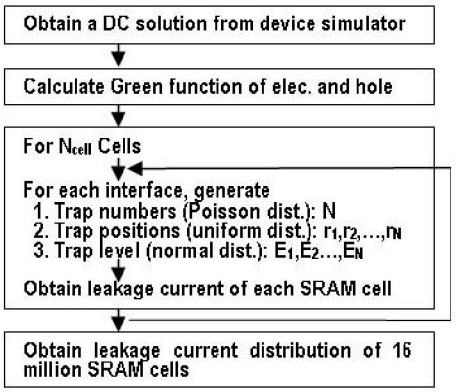

Figure 3. Overall simuation procedure. Trap number obeys the Poisson ditribution. their positions are uniformly distributed in the STI-silicon interface and silicon body-ILD interface and thier energy levels are normally distributed.

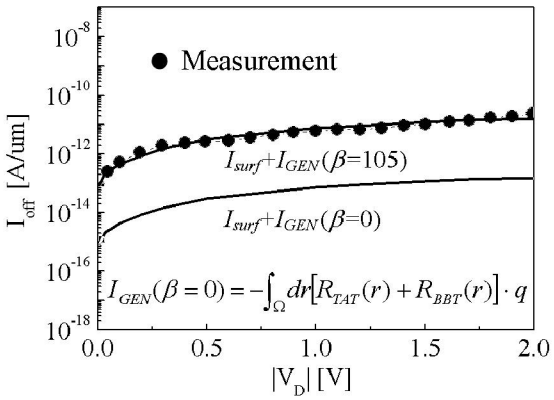

Figure 4. V_{Drain}-I_{off} curve of the SC-like SOI transistors obtained from the simulation data and measurement. Total leakage current is obtained by generation current (I_{GEN}) using the Green's function for β=0 and β=105.

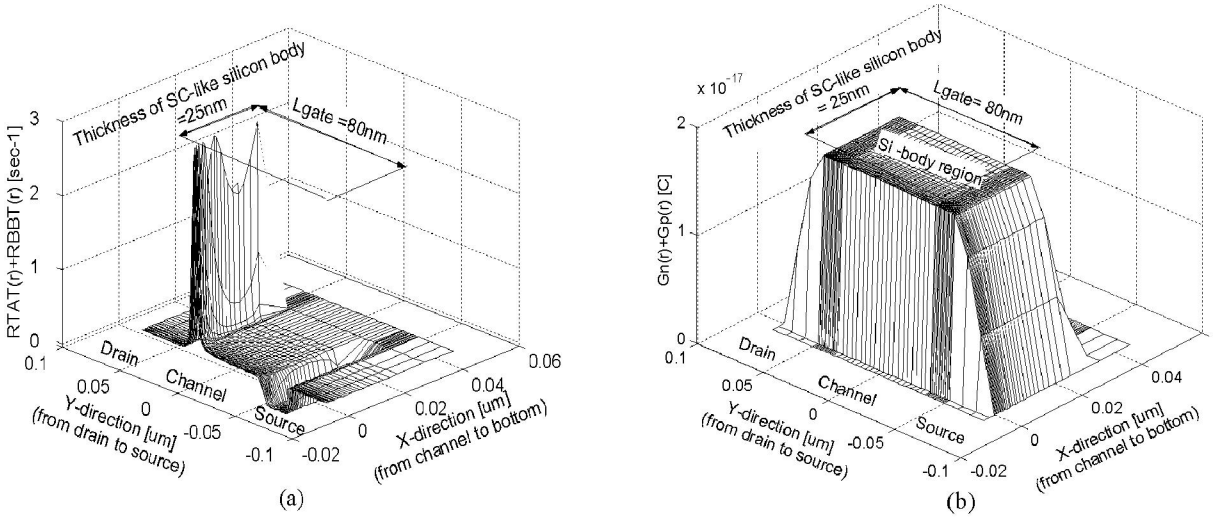

Figure. 5. (a) $-\{R_{TAT}(r)+R_{BBT}(r)\}$ (net generation rate) for V_{Drain}=-2.0V in Si-body. $-(R_{TAT}+R_{BBT})$ has the largest value at the depletion region of the drain terminal. (b) $G_n(r)+G_p(r)$ (sum of the electron and hole Green's function) for V_{Drain}=-2.0V in Si-body, when the impulse noise with a charge of 1.6×10^{-19}C locates in the Si-body. The sum of the electron and hole Green's function is uniform regardless of the location of impulse noise in the Si-body.

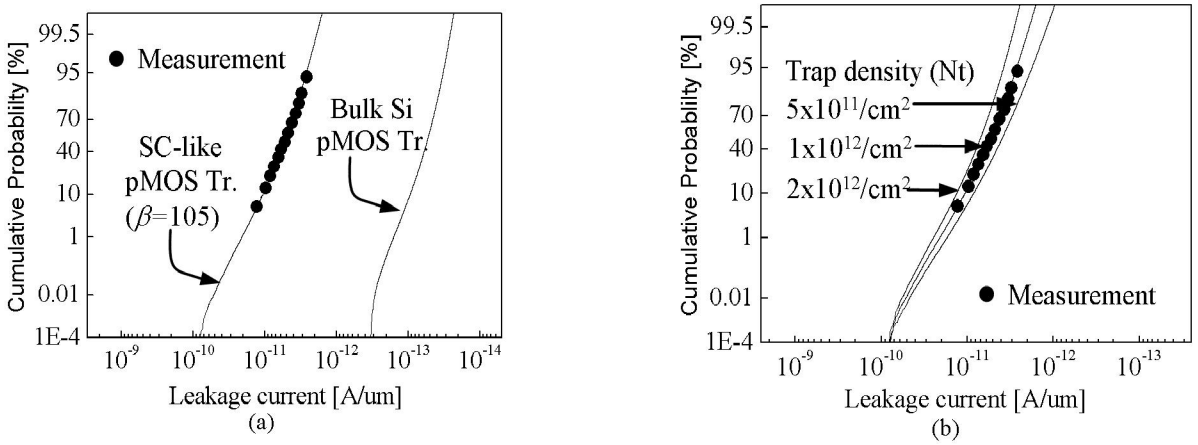

Figure 6. (a) Comparison of the leakage current distribution of SC-like SOI transistor and Bulk-Si transistor. Distribution of SC-like SOI transistor is larger and worse than that of bulk-Si transistor and (b) Effect of trap density (N_t) on the leakage current distribution of SC-like SOI transistor. Increase in the trap density reduces the variation of the leakage current distribution, but the magnitude of the leakage current is increased.