Optimization of Halo Implant Using 3D TCAD for Nanoscale MuGFETs

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Abstract— **This work presents a theoretical design analysis of halo implants for n-MuGFETs using commercial three-dimensional (3D) TCAD simulation tool. The main objective was to show feasibility of a three-dimensional (3D) process simulation within the context of optimization of the device design and the underlying fabrication processes. The 3D simulation process flow is based on the development of the SOI based FinFET devices. Process and device simulations of halo implants have been performed with different nitride spacer, fin thicknesses and gate lengths. We see that thick nitride spacers (50nm) and thinner fins (30nm) are beneficial for 80 nm doped channel n-MuGFETs. Similarly, the role of halo implant is critical to suppress the short channel effects for small gate lengths (65, 50nm etc) devices. Although, the halo implant is beneficial to adjust the threshold voltage to a required value, its presence is counter productive from the point of view of degradation in ION particularly for long channel devices. Using pre-development process results of our MuGFETs, good agreement was obtained with simulations and experimental data in terms of threshold voltage roll-off, ION/IOFF and short channel effects.**

Keywords; FinFETs, Multigate FETs, MuGFETs

I. INTRODUCTION

Despite the added process complexity, double (*FinFET*) or triple (Tri-Gate) gate Multi-Gate FET (*MuGFET*) devices are emerging as strong candidates for low power or high performance application in the future. One of the main advantages of *MuGFETs* is that they offer superior scalability with manufacturability of conventional planar transistors. Devices with gate lengths below 20 nm and acceptable turn-off characteristics have already been demonstrated. Previous studies of double (*FinFETs*) and triple gate (*MuGFETs*) devices based on conventional *Si* or strained *Si-SiGe* channel mainly focused on fabrication and general device design aspects such as corner effects, short channel effects, *S/D* doping gradient and mostly relied on simplified models using 2D or 3D device simulation. Since real devices go through many processing steps, reliable evaluation or design optimization of final devices depend on the optimized unit process development. *TCAD* or Technology *CAD* process simulation is therefore prerequisite to device optimization or device design through device simulation.

This work presents a first theoretical design analysis of halo implants for *MuGFETs* using commercial three-dimensional (*3D*) *TCAD* simulation tool. Process and device simulations of halo implants have been performed with different nitride spacer, fin thicknesses and gate lengths. Using pre-development process results of our *MuGFETs,* good agreement was obtained with simulations and experimental data in terms of threshold voltage roll-off, I_{ON}/I_{OFF} and short channel effects.

II. PROCESS AND DEVICE SIMULATIONS

Critical process steps for tri-gate *MuGFETs* on standard SOI are channel implant, fin formation (*Fin* width=30/50 *nm* and *Fin* height=*88 nm*), gate oxide growth (2 nm), extension implant (*LDD*), halo implant, spacer formation (25, 50 *nm*), and finally S/D implant before RTA. All necessary thermal steps have been included in the process simulation. Well-known Equilibrium diffusion model (*PD* Fermi) and dual Pearson implantation model was included in the process simulation using default model parameters. Only quarter of the device was used in the process simulation flow, and the device was then reflected at the end of the process flow to get half of the device for device simulation. The grid accuracy at the Si/SiO_2 interface was 0.1 *nm* and in the *Si* channel region was 1 - 2 *nm*. The total number of mesh points for the half-device was approximately 180,000, while the processing time was 10-12 hours using 3D *TCAD*. Device simulations have been performed using drift diffusion model taking into account quantum confinement effects (*MLDA* model), bandgap narrowing effects, low field (doping and temperature dependence) and high field (Caughey Thomas) mobility models including Lombardi surface scattering mobility model. Other physical effects such as *SRH* recombination and auger recombination were also included in the device simulation. We neglected the gate depletion effects. The threshold voltage was defined at drain current of 1.0E-7 A, while I_{OFF} was defined at V_{GS}=0V, and V_{DS}=1.2V. Similarly, I_{ON} was defined at $V_{GS}=V_{DS}$=1.2V.

III. RESULTS AND DISCUSSION

A simulated structure and corresponding boron doping profile of left half of 100 *nm MuGFET* device is shown in figure 1. A maximum amount of active boron at the gate edges with 3 x 10^{18} cm^{-3} (with halo: yellow lobes) and 3 x 10^{17} cm^{-3} (no halo: light green) is visible in the structures. No significant difference in the arsenic concentration was obtained as expected and the junction abruptness also remains the same for both types of structures. A 3D view of net doping profile in the *Si Fin* region with cut along x and z axis is shown in Fig.2 and

3 for structures with halo energy of 6 *keV* and total dose of 3 x 10^{12} cm^{-2}.

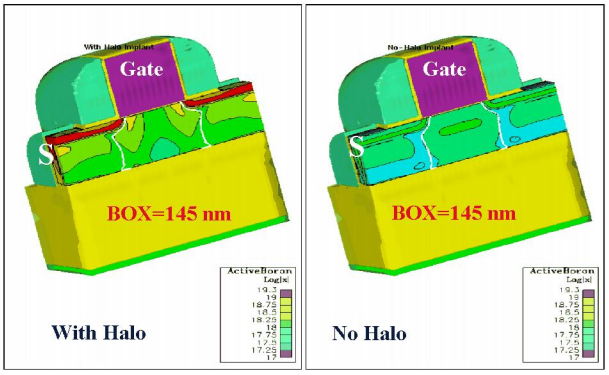

Figure 1. An example of left half of a 100 nm *MuGFET* device with and without halo implant.

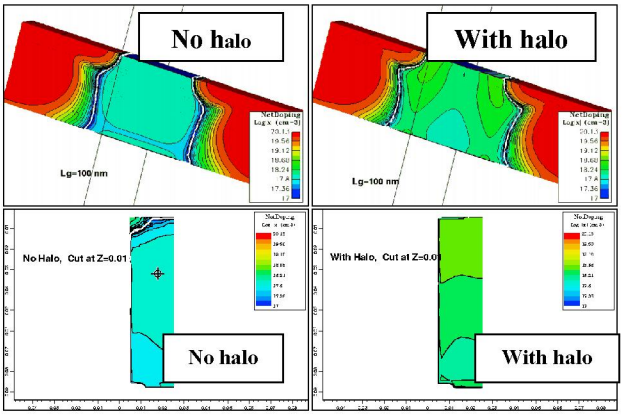

Figure 2. Net doping profile in the *Si Fin* region and cut along x-axis at z=0.01 μm of a *MuGFET* device.

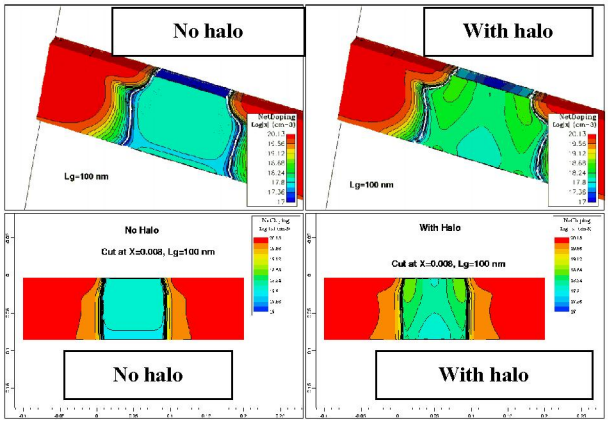

Figure 3. Net doping profile in the *Si Fin* region and cut along z-axis at x=8 nm from the gate surface.

A threshold voltage and *DIBL* (drain induced barrier lowering) as a function of dose at constant halo energy of 6 keV for 50 *nm Fin* thickness is shown in figure 4. Threshold voltage increases with the increase of halo implant dose and energy. A threshold voltage tunability was 289 *meV* with varying dose from 0 (i.e., no halo) to 5 x 10^{13} cm^{-2} at constant energy of 6 *keV* for 80 nm gate device. Similarly, the threshold voltage tunability of 196 *meV* was obtained with varying halo energy from 0 to 8 *keV* at fixed dose of 2 x 10^{13} cm^{-2}. Increasing the halo implant dose at constant halo energy, I_{ON} (one decade) and I_{OFF} (three decades) current decreases in general (Fig. 5) because of reduction in the electron mobility. The same qualitative trend was obtained at constant dose with varying halo implant energy.

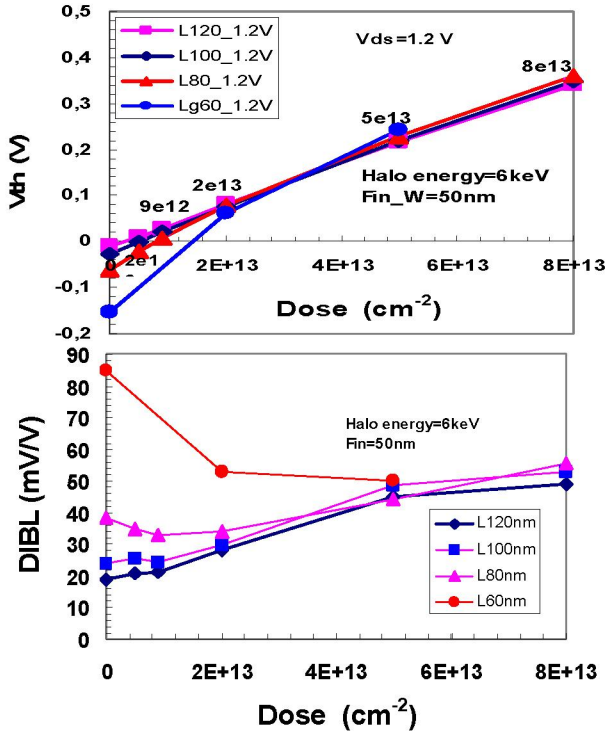

Figure 4. A threshold voltage (top) and *DIBL* (bottom) versus dose of *MuGFET* device at *6 keV* halo energy with 50 *nm Fin* width.

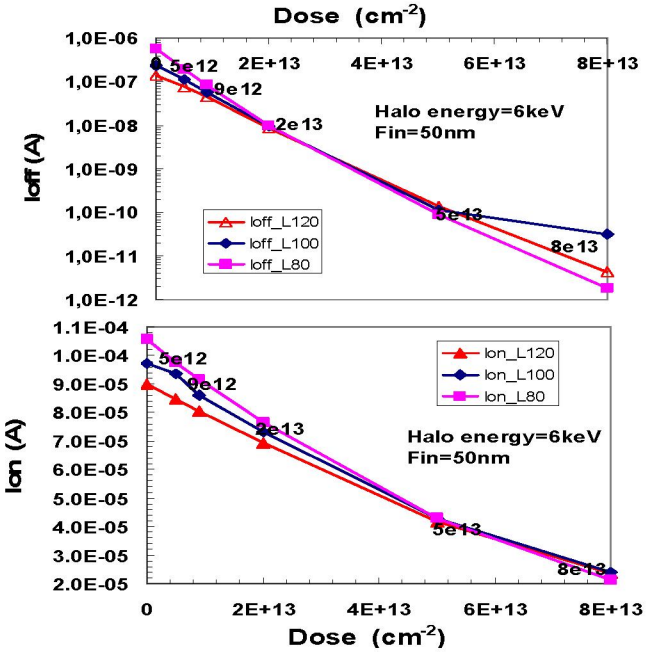

Figure 5. Off (top) and On (bottom) current versus dose at constant halo energy of 6 *keV* of a *MuGFET* device.

For a *Fin* thickness of 50 *nm*, gate oxide of 2 *nm*, and spacer thickness of 50 nm, I_{OFF} decreases to 44 and 24 % with a dose variation from 4 x 12 to 2 x 13 cm^{-2} at halo energies of 6 and 4 *keV*, respectively. Similarly, I_{ON} decreases to only 5 and 2 % with a dose variation from 4 x 12 to 2 x 13 cm^{-2} at halo energies of 6 and 4 *keV*, respectively. A slight decrease (4 -5 %) in *DIBL* was observed with a dose variation from 4 x 12 to 2 x 13 cm^{-2}, while *S* (Subthreshold slope) remains approximately constant.

For undoped channel *MuGFETs*, I_{OFF} decreases to 35 and 19 % with dose variation from 4 x 12 to 2 x 13 cm^{-2} at halo energies of 6 and 4 *keV*, respectively. I_{ON} decreases to only 3.8 and 1.6 % with a dose variation from 4 x 12 to 2 x 13 cm^{-2} at halo energies of 6 and 4 *keV*, respectively. Compared to doped channel, undoped channel 80 nm *MuGFET* devices show 30 % higher *DIBL*, and 10 % higher subthreshold slope *S* as shown in figure 6 with *Fin* thickness of 50 *nm* and gate oxide of 2 *nm*.

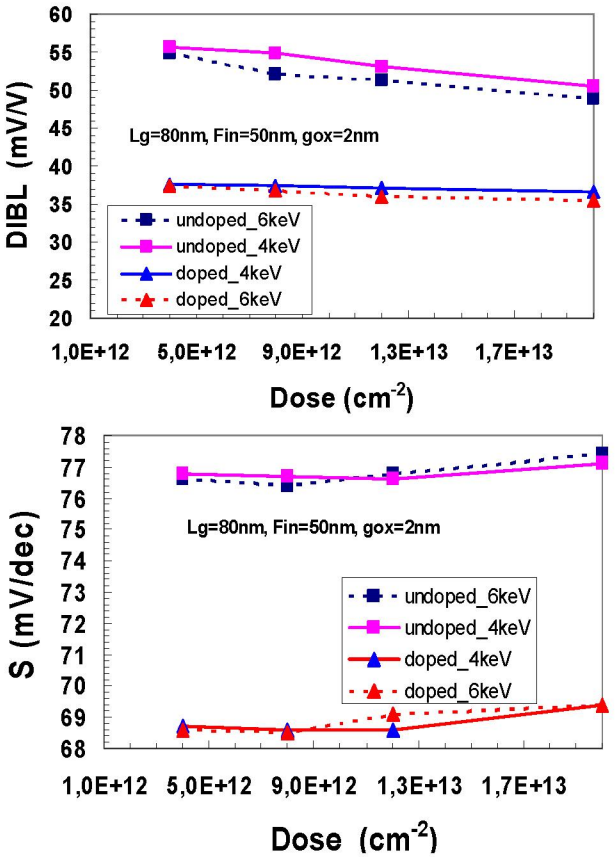

Figure 6. *DIBL* (top) and *S* (bottom) versus dose of 80 nm *MuGFET* device with doped and undoped channel.

Influence of different nitride spacer thickness on electrical performance of a *MuGFET* device is reported in figure 7 at 4 and *6 keV* halo implant energy. For a given halo implant dose and energy, *DIBL* and *S* are 26 and 7 % higher for a 25 nm nitride spacer than that of 50 nm spacers. Similarly, reduction in I_{OFF} and I_{ON} are 10 and 2 %, respectively, less for a 25 nm nitride spacer than the 50 nm spacer.

The effect of variation in *Fin* thickness at constant halo energy and with different halo dose is shown in figure . 8. Compared to a thicker *Fin* (50 *nm*), a thinner *Fin* (30 *nm*) device produces approximately 50 % less degradation in I_{ON} and I_{OFF} with variations of halo implant dose from 4 x 12 to 20 x 12 cm^{-2}. Similarly, we obtained 45 and 4 % less *DIBL* and *S* respectively, with thinner *MuGFET* (i.e., *Fin* width=30 *nm*) than thicker *MuGFET* (i.e., *Fin* width=50 *nm*) devices.

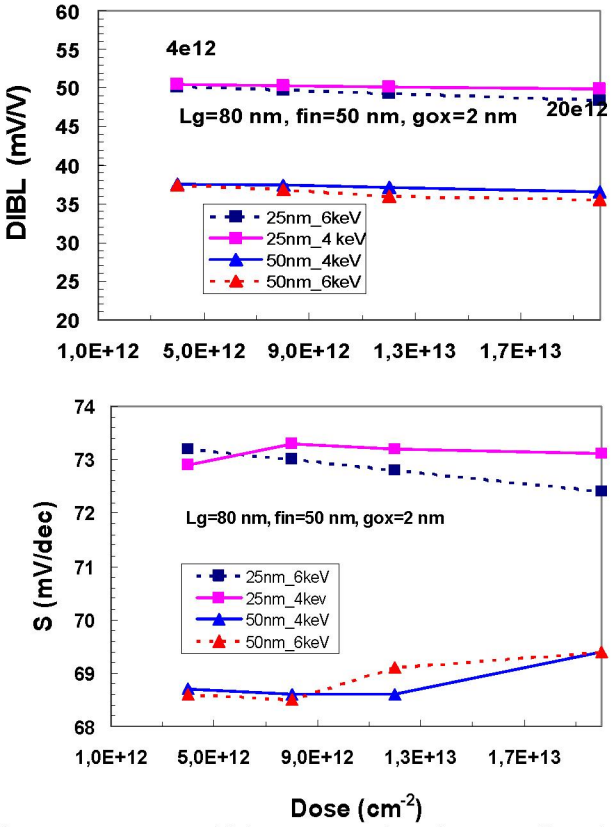

Figure 7. *DIBL* (top) and *S* (bottom) versus dose of 80 nm *MuGFET* device with different nitride spacer thicknesses.

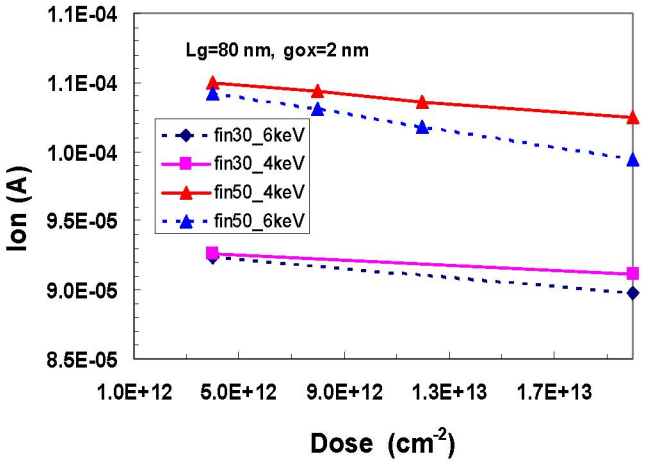

Figure 8. I_{ON} as a function of halo dose for different Fin thickness and halo energy.

Threshold voltage roll-off, *DIBL* and I_{ON} versus I_{OFF} behavior for different gate length devices is shown in figure 9. The on and off current data was extracted with varying gate lengths at constant halo dose and energy.

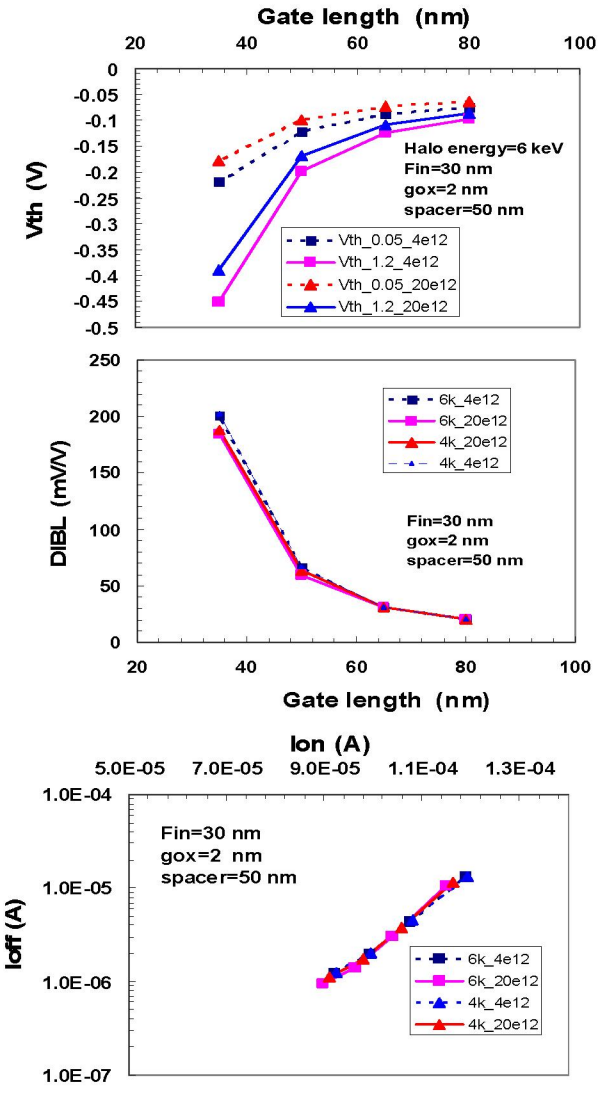

Figure 9. Threshold voltage roll-off (top), *DIBL* (middle) and on/off current (bottom) behavior of *MuGFETs* at different halo dose and halo energy.

Finally, simulation results have been compared with experimental data from different devices picked randomly from different dies on the same wafer. Comparison of simulation was performed using our real process flow of manufactured devices with identical set of geometrical (*Fin* width of 30 nm, *Fin* height of 88 nm and nitride spacer of 20 nm) and implant parameters and using *TiN* metal gate for device simulation with a work function of 4.45 eV. A fairly good agreement has been obtained for different *MuGFETs* in terms of threshold voltage (Fig. 10a), I_{ON}/I_{OFF} (Fig. 10c,and Fig. 10d) current and short channel effects (Fig. 10b).

IV. CONCLUSIONS

In summary, we see that a thick nitride spacers (50nm) and thinner fins (30nm) are beneficial for 80nm doped channel n-FETs. Similarly, the role of halo implant is critical to suppress the short channel effects for small gate lengths (65, 50nm etc) devices. Although, the halo implant is beneficial to adjust the threshold voltage to a required value, its presence is counter productive from the point of view of degradation in I_{ON} particularly for long channel devices.

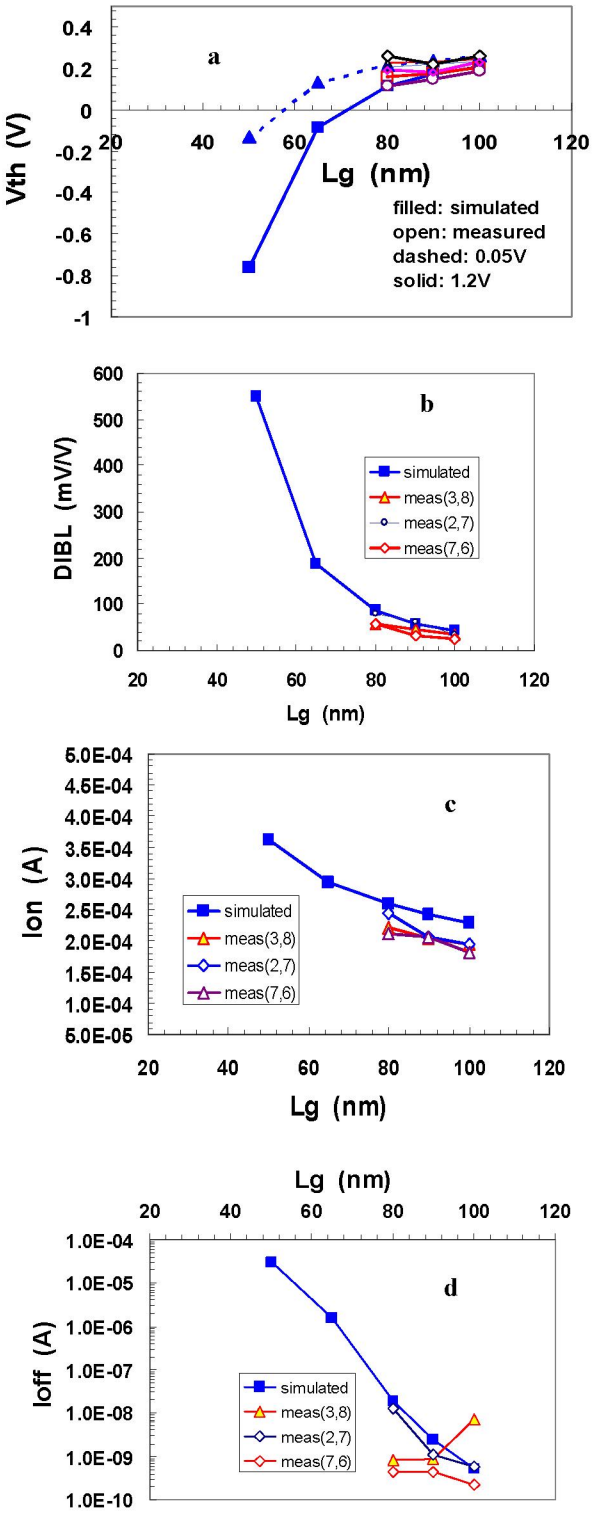

Figure 10. Threshold voltage roll-off (top: a), *DIBL* (middle: b) and on/off current (bottom: c, d) behavior of *MuGFETs* at different halo dose and energy.

V. ACKNOWLEDGEMENT

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