Analysis and Compact Modeling of MOSFET High-Frequency Noise

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***Abstract*— We have developed a high-frequency noise model for short channel MOSFETs by considering the position dependent surface potential which results in a non-uniform mobility distribution along the channel. The chosen approach successfully reproduces the induced-gate noise and the cross-correlation noise between drain and gate for short channel MOSFETs without additional model parameters. In particular, the gate noise characteristics at GHz frequencies are accurately captured. The newly developed high-frequency noise model is implemented in the complete surface-potential based MOSFET model HiSIM (Hiroshima-university STARC IGFET Model) for circuit simulation.**

I. Introduction

The technology development for scaling the gate length ($L_{\rm g}$) down to the sub-100nm regime promises to accomplish RF applications based on MOSFET technology. Therefore, the impotance of analyzing and predicting the noise characteristics in MOSFETs is increasing in particular for RF analog design [11]. Figure 1 shows schematically the current noise characteristic of MOSFETs as a function of frequency f. At low frequency the $1/f$ noise dominates, while at higher frequencies ($>$ 10KHz) the thermal noise and the induced-gate noise become obvious, inducing also the cross-correlation noise. It has been demonstrated that the thermal noise characteristic of short-channel MOSFETs is determined by the surface-potential distribution along the channel [9]. In the GHz frequency range the high frequency carrier dynamics has to be considered explicitly.

Previous modeling of the high-frequency noise has been done either based on an admittance matrix [1, 2] or a transmission line [3] description. However, explicit analysis of calculated results is still not sufficient. Especially no explicit modeling of these noise characteristics for the short-channel case is given. Here we aim at providing compact models for high-frequency noise types based on their physical origin and valid for any gate lengths. The findings of our analysis suggest that excess noise must be expected under the saturation condition for all kinds of the high-frequency noise in short-channel MOSFETs of which the physical origin is the surface-potential distribution along the channel.

II. High Frequency Noise Modeling

Noise modeling for short channel MOSFETs ($L_{\rm g}$ down to 100nm or less) requires the consideration of the position dependent surface potential along the channel, because for 100nm size devices the electric force lines from the drain region penetrate through the channel, and modulate electronic states of the channel even in the vicinity the source region. This potential distribution causes all possible device specific properties, such as the inversion carrier distribution as well as the mobility distribution. We carried out an analysis of the channel mobility for MOSFETs with various channel lengths by using a 2-D device simulation. The channel mobility is almost constant over the channel for long channel devices ($L_{\rm g} \gtrapprox 0.5\mu$m) as shown in Fig. 2. For a short channel device with $L_{\rm g} = 0.11\mu$m, on the contrary, the position dependence of the channel mobility becomes prominent.

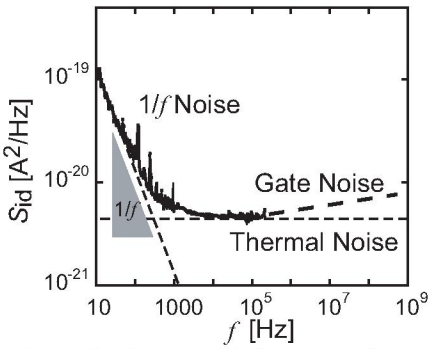

Fig. 1. Typical example of measured drain current noise spectral intensity $S_{\rm id}$ as function of frequency f. Three different noise mechanisms are depicted. The $1/f$ noise is dominant at low frequency. The thermal noise and the induced-gate noise become obvious at higher frequency.

This demonstrates the necessity of considering this distribution in the noise modeling. We have previously reported a circuit simulation model for the thermal noise of a drain current $S_{\rm i_d}$ by considering the surface-potential distribution along the channel explicitly [9]

$$S_{\rm i_d} = 4kTg_{\rm ds0}\gamma,\ \gamma = \frac{1}{L_{\rm eff}^2 I_{\rm ds} g_{\rm ds0}} \int \{g_{\rm ds}(\phi)\}^2\, d\phi \qquad (1)$$
$$g_{\rm ds0} = g_{\rm ds}(V_{\rm ds} = 0).$$

Here $L_{\rm eff}$ and $g_{\rm ds}$ are the effective channel length and the channel conductance, respectively. Figure 3 shows the comparison of calculated results with measurements for the thermal noise coefficient γ, which is equal to one at $V_{\rm ds} = 0$ and reduces to $2/3$ under the saturation condition for long $L_{\rm g}$ MOSFETs. However, γ increases under the saturation condition for reduced gate lengths. This feature was reproduced

automatically without any additional model parameter. The reason for the γ increase under the saturation condition is the enhanced scattering along the channel, originated by the steeper potential increase.

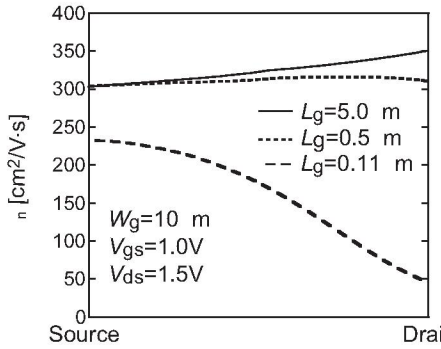

Fig. 2. Simulation results of the mobility along the MOSFET channel for $L_{\rm g} = 5.0\mu$m (solid line), 0.5μm (dotted line) and 0.11μm (dashed line). The lateral axis is normalized by the gate length. A position dependence of the mobility is clearly seen for the $L_{\rm g} = 0.11\mu$m device.

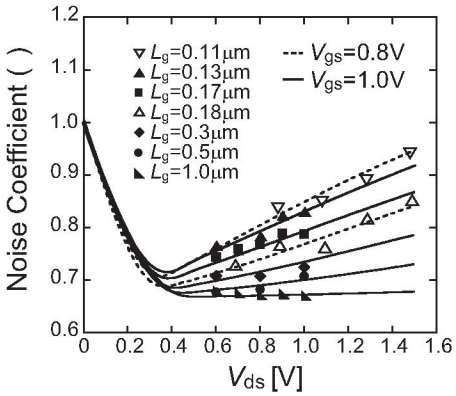

Fig. 3. Calculated (lines) thermal noise coefficient γ as a function of drain voltage $V_{\rm ds}$ together with measurements (symbols). Two different technologies are compared (open symbols and solid symbols). For the calculation the circuit simulation model HiSIM including the developed noise model was applied.

The physical origin of the induced-gate noise ($S_{\rm i_g}$) is the capacitive coupling of the channel conductance to the gate conductance as schematically shown in Fig. 4. Based on the assumption that the gate noise is induced by the thermal noise in the channel through the capacitive coupling, van der Ziel derived a simple description [1]

$$S_{\rm i_g} = 4kTg_{\rm g}\beta,\ g_{\rm g} = \frac{(\omega C_{\rm gs})^2}{5g_{\rm ds0}};\ \ (\omega = 2\pi f) \tag{2}$$

where $C_{\rm gs}$ is the gate-source capacitance. The expression is valid in the saturation region for frequencies f below $1/3$ of the cut-off frequency $f_{\rm T}$ and this frequency range is sufficient for most real applications of the device. Both the $1/f$ noise and the thermal noise increase with reduced device size. On the contrary, the induced noise intensity reduces with reducing the device size. This can be understood from the fact that the induced-gate noise is directly related to the gate capacitance, which is proportional to the device size. In addition, the induced-gate is proportional to f^2, which makes the gate noise a serious problem under the high-frequency operation. Although it is valid only under the saturation condition, van der Ziel's equation is simple and describes the main cause of the induced-gate noise clearly.

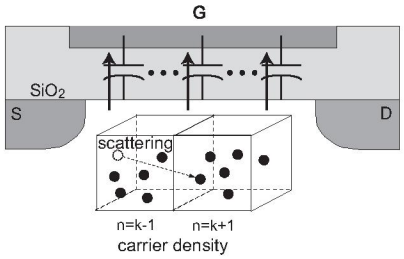

Fig. 4. Schematic of the physical origin of the induced gate noise. The thermal noise generated in the channel causes the induced-gate noise because of the capacitive coupling.

We have derived an improved description, valid for any bias conditions, by solving the continuity equation [4]

$$V(x)\frac{\partial V(x)}{\partial x} = -\frac{d}{W\epsilon\mu}I(x) \tag{3}$$

together with the current density equation

$$\frac{d\{i(x)\}}{dx} = -j\omega\frac{\epsilon W}{d}v(x) \tag{4}$$

$$V(x) = V_0(x) - v(x),\quad I(x) = I_0 - i(x) \tag{5}$$

where $V_0(x)$ and I_0 are the quiescent potential and current, respectively. $v(x)$ and $i(x)$ are the incremental variables of potential and current, respectively. If we assume a constant channel mobility, these equations can be solved analytically in a Bessel function form. To obtain a closed form, only the low-order term of the Bessel function is considered [10].

For the detailed derivation a small section Δx in the channel with a voltage fluctuation of Δv is considered. This Δv is exactly corresponding to the noise source. Furthermore, two transmission lines, from Δx to the source side and to the drain side, are considered to derive the description of the gate current noise with the Bessel function [3]. The potential distribution is included with the help of the mobility distribution and the charge distribution which are treated separately. The description is further simplified to obtain a closed form by truncating higher-order terms of the integration along the channel. The final equation is

$$S_{\rm i_g} = S_{\rm i_g,0}\cdot\frac{1}{\xi_{00}-\xi_{\rm L}}\int_{\xi_{\rm L}}^{\xi_{00}}\left(\frac{\mu}{\mu_0}\right)^{-1}d\xi \tag{6}$$

$$\xi_{00} = \left(\frac{Q_{\rm n0}}{C_{\rm ox}}\right)^2,\quad \xi_{\rm L} = \left(\frac{Q_{\rm n0}}{C_{\rm ox}}\right)^2 - \frac{2IDD}{\beta C_{\rm ox}} \tag{7}$$

$$IDD = \frac{L_{\rm eff}}{W_{\rm eff}}\cdot\frac{\beta}{\mu}\cdot I_{\rm ds} \tag{8}$$

where

$$S_{\rm i_g,0} = \frac{16}{135}\omega^2 kT\frac{C_{\rm gs}^2}{g_{\rm ds0}} \cdot \frac{\xi_{00}^{1/2}\left(4\xi_{00}^2 + 20\xi_{00}^{3/2}\xi_{\rm L}^{1/2} + 42\xi_{00}\xi_{\rm L} + 20\xi_{00}^{1/2}\xi_{\rm L}^{3/2} + 4\xi_{\rm L}^2\right)}{\left(\xi_{00}{}^{1/2} + \xi_{\rm L}^{1/2}\right)^5}. \tag{9}$$

The derived gate noise model is implemented in the surface-potential-based MOSFET model HiSIM. The integration in Eq. (6) is carried out analytically by using the mobility model implemented in HiSIM, and thus the computation penalty of the high frequency noise is negligible.

Cross-correlation noise is derived as

$$S_{\mathrm{i_g i_d}} = j\frac{4}{9}\omega kTC_{\mathrm{gs}} \cdot \frac{(\xi_{00}-\xi_{\mathrm{L}})\left(\xi_{00}+4{\xi_{00}}^{1/2}{\xi_{\mathrm{L}}}^{1/2}+\xi_{\mathrm{L}}\right)}{\left({\xi_{00}}^{1/2}+{\xi_{\mathrm{L}}}^{1/2}\right)^4}, \tag{10}$$

and the correlation factor is written as

$$\begin{aligned} c &= \frac{S_{\mathrm{i_g i_d}}}{\sqrt{S_{\mathrm{i_g}} \cdot S_{\mathrm{i_d}}}} \\ &= j\frac{\sqrt{15}}{6\sqrt{\gamma}} \cdot \frac{(\xi_{00}-\xi_{\mathrm{L}})}{\left({\xi_{00}}^{1/2}+{\xi_{\mathrm{L}}}^{1/2}\right)^{3/2} \cdot \xi_{00}^{1/4}} \\ &\cdot \frac{\xi_{00}+4{\xi_{00}}^{1/2}{\xi_{\mathrm{L}}}^{1/2}+\xi_{\mathrm{L}}}{\left(4{\xi_{00}}^2+20\xi_{00}^{3/2}\xi_{\mathrm{L}}^{1/2}+42\xi_{00}\xi_{\mathrm{L}}+20\xi_{00}^{1/2}\xi_{\mathrm{L}}^{3/2}+4\xi_{\mathrm{L}}^2\right)^{1/2}}. \end{aligned} \tag{11}$$

III. Results and Discussion

Figure 5 compares calculation results by the developed model with the van der Ziel model for a long-channel transistor as a function of drain-source voltage V_{ds}. For the van der Ziel model, C_{gs} and g_{ds0} are taken from HiSIM results. Therefore, the results of the two cases are quite similar for the long-channel case in the saturation region. For the linear region, deviations are seen because the van der Ziel model is only valid for the saturation condition. Figure 6 shows

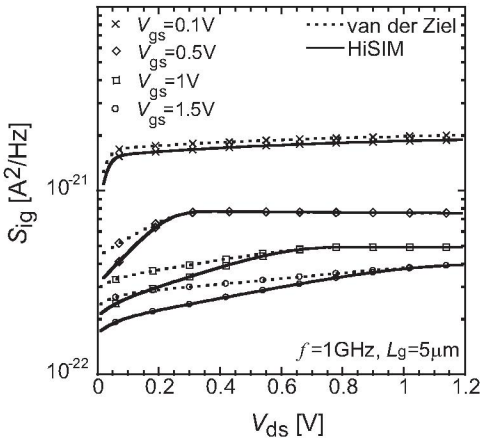

Fig. 5. Comparison of calculated induced-gate noise $S_{\mathrm{i_g}}$ with HiSIM (solid lines) and the van der Ziel model (dotted lines). Symbols indicate the gate-source voltage biases. The plot is given as a function of drain-source voltage V_{ds} for different gate-source voltage values. Deviations are seen outside of the saturation region, where the van der Ziel model is no more valid.

the calculated induced-gate noise for different gate lengths at $V_{\mathrm{gs}} = 1$V. Under the saturation condition our model and the simple van der Ziel model shows the same results. However, a deviation becomes clear for the short-channel case. The HiSIM result for the short-channel MOSFET shows enhanced induced-gate noise under the saturation condition, as also observed for the thermal noise.

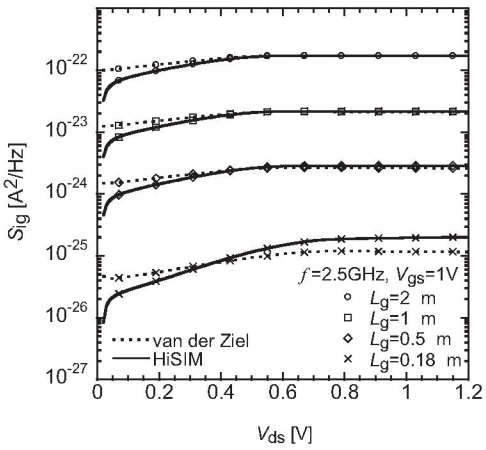

Fig. 6. $S_{\mathrm{i_g}}$ as a function of the drain voltage for various gate lengths.

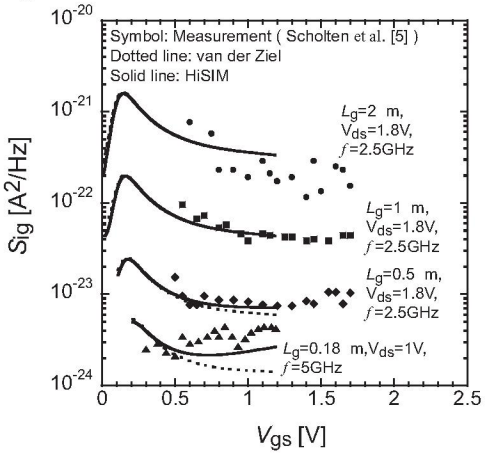

Fig. 7. Comparison of calculated induced-gate noise S_{ig} for different gate lengths (L_{g}) as a function of gate-source voltage V_{gs}. Solid and dotted lines are the simulation results obtained from the developed model and the van der Ziel model, respectively. Symbols are the measurement results. The noise increase for short channel devices is well reproduced with HiSIM.

Figure 7 shows the calculated noise intensity S_{ig} as a function of V_{gs} in comparison to measurements [5]. For this comparison, calculated S_{ig} for $L = 2\mu$m is fitted to the measurement by adjusting the device width. Both models coincide with each other for long-channel cases. This is because the simulation is done under the saturation condition, whereas deviation of the van der Ziel model from measurements becomes obvious with reduced MOSFET length. The simple van der Ziel model underestimate the induced-gate noise. On the contrary the HiSIM results with the developed model reproduce the measurement features. The measured S_{ig} for $L_{\mathrm{g}} = 0.18\mu$m includes a noise enhancement as seen Fig. 6, which the van der Ziel model misses. Figure. 8 compares calculated S_{ig} with and without the short-channel effect together with the simulated threshold voltage V_{th}. It is seen that the maximum of the induced-gate noise occurs around V_{th}.

The correlation factor (Eq. (11)), which is usually a measure for the cross-correlation noise, is shown in Figs. 9(a) and

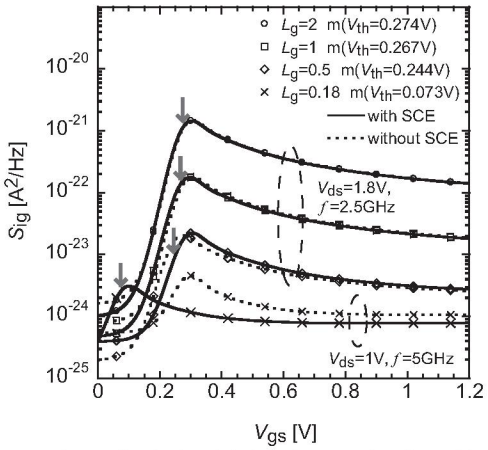

Fig. 8. Comparison of calculated induced-gate noise $S_{\rm ig}$ with the short-channel effect and without. The $V_{\rm th}$ is depicted by arrows.

(b) as a function of $V_{\rm ds}$ and $V_{\rm gs}$, respectively. The value of about 0.4V is predicted by van der Ziel under the saturation condition. Our simulation results are slightly smaller than the value, and reduce to zero at $V_{\rm ds}$=0.

The developed model is applied to estimate the induced-gate noise intensity with respect to the drain current noise as shown in Fig. 10 for $L_{\rm g} = 5\mu$m. In the low-frequency region ($f \lessapprox$ 100MHz), the drain current noise dominates over the gate noise. For the frequency around 1GHz, the model predicts that the induced-gate noise become comparable in intensity to the drain current noise, and beyond 1GHz frequency the induced-gate noise dominates. Therefore, the induced-gate noise becomes a primary concern for RF applications.

IV. Conclusion

We have developed a compact model for the induced-gate noise and the cross-correlation noise between drain and gate noises. The model reproduces measured characteristics for any gate lengths and at any bias conditions without additional model parameters specific to these noise features. An excess noise of the induced-gate noise has been found for reduced gate lengths as also observed for the thermal noise. The potential distribution and the related mobility distribution along the channel are responsible for this excess noise.

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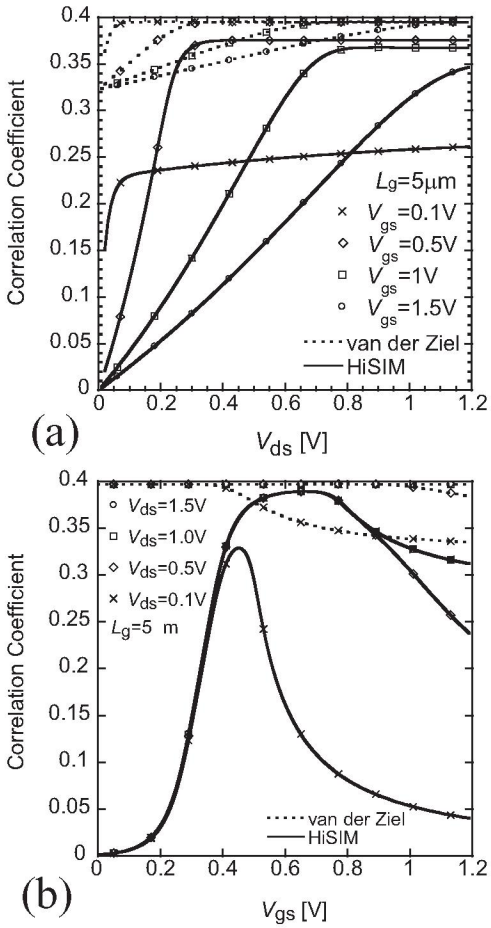

Fig. 9. Calculated correlation coefficient between the thermal noise and the induced-gate noise obtained by HiSIM (solid lines) and van der Ziel model (dotted lines). Symbols indicate the gate-source voltages. (a) and (b) depict correlation coefficients as a function of drain voltage and of gate voltage, respectively. Again the deficit of the van der Ziel model in the linear region is improved by the developed model.

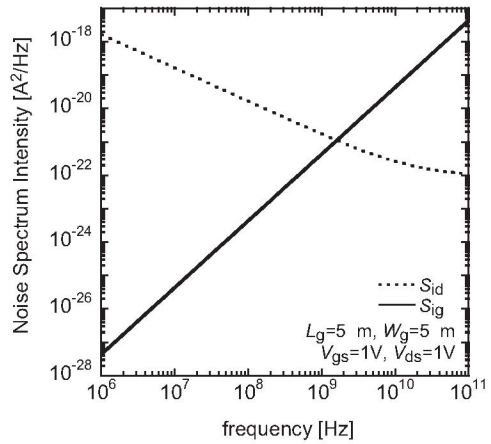

Fig. 10. Simulation results of the drain current noise $S_{\rm i_d}$ (solid line) and the induced-gate current noise $S_{\rm i_g}$ (dotted line) as a function of frequency. The induced-gate noise becomes larger than the drain current noise for the high-frequency region ($f \gtrapprox$ 1GHz).

