Improvement of Drive Current in Bulk-FinFET using Full 3D Process/Device Simulations

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***Abstract*—We discussed the optimization of structure and doping profile of bulk-FinFETs by using 3D process and device simulations. The channel profile was determined so as to realize higher drive current as well as lower punch-through current. The analysis of stress field for bulk-FinFETs and SOI-FinFETs revealed that the channel stress induced by a stress liner (SL) in the bulk-FinFET is larger than that for the SOI-FinFET. In addition, we applied a raised source/drain (RSD) structure to the bulk-FinFETs and optimized doping profile in the RSD region. The combination of stress liner and RSD structure is found to be efficient for improving drive current of a bulk-FinFET.**

Keywords-component; FinFET; drive current; punch-through current; raised source/drain; mobility enhancement; optimization; 3-D process simulation; 3-D device simulation; TCAD

I. INTRODUCTION

FinFET is one of the promising candidates for device structure in 32 nm technology node and beyond, because of its good cut-off characteristics due to double gate mode operation. Two kinds of FinFET structure have been proposed, namely a bulk-FinFET fabricated on a bulk Si substrate and SOI-FinFET on an SOI substrate (Fig.1). The bulk-FinFET is superior to the SOI-FinFET in terms of wafer cost, process compatibility and extendibility of conventional planar CMOS technologies. However, a serious issue arises in the bulk-FinFET, since weak gate controllability beneath the gate region induces large punch-through current as depicted in Fig.2. In order to reduce the punch-through current, an appropriate design of channel profile is required. We have proposed a novel punch-through stopper (PTS) formation technique [2], making use of the lateral scattering of the implanted ions in shallow trench isolation (STI) regions (Fig 3). In the present paper, firstly, we discuss the channel profile optimization of the bulk-FinFET to realize high drive current with low leakage current.

On the other hand, improvement of drive current is one of the most important issues in the FinFET design. Recently, it has been found experimentally that the drive current of SOI-FinFETs is efficiently improved by mobility enhancement with the stress liner (SL) technique [3] and by reduction of parasitic resistance using a raised source/drain (RSD) with selective epitaxial growth (SEG) technique [4]. In the present paper, secondly, we investigate stress field effect induced by the SL deposited on the FinFET, focusing on the structural difference between bulk-FinFET and SOI-FinFET. Thirdly, we briefly discuss the optimization of doping in the RSD region. And finally, we describe the result of total optimization by taking into consideration of channel profile, SL effect, and RSD structure.

II. CHANNEL PROFILE OPTIMIZATION

We investigated the impact of PTS and channel ion implant dose on subthreshold swing (S-swing) and drain current (I_{on}) at constant gate overdrive. In the following discussion, we use 3-dimensional process/device simulators HySyProS and HyDeLEOS [5]. In Table 1, the structural parameters of FinFETs used in the simulations are shown. In Fig.1, the bulk-FinFET and the SOI-FinFET are compared. In the bulk-FinFET, large punch-through current flows beneath the channel region (Fig.2), and therefore, the punch-through stopper (PTS) region should be formed. The PTS implant gives rise to higher dopant concentration in the PTS region than that in the channel region. It is difficult to realize an appropriate dopant distribution throughout channel to PTS regions by the single PTS implant. Therefore, we combined the channel implant (CI) with tilted angle for the doping in the channel region (Fig.3) and the PTS implant with zero tilt-angle to obtain the optimum dopant profile (Fig.4). Figures 5 and 6 show the response surfaces of S-swing and I_{on} as functions of CI dose and PTS dose, respectively. We have found that the S-swing is monotonously reduced by the increase of both CI dose and PTS dose. However, the I_{on} shows the maximum value at CI dose of 1×10^{12}cm^{-2} and PTS dose of 1×10^{13}cm^{-2} (Fig.6). The increase of the CI dose causes the high dopant concentration in the channel, and results in the degradation of carrier mobility. The increase of the PTS dose also leads to the narrowing of the effective channel width in fin height direction due to the widening of the PTS region, and causes the decrease of the I_{on}. On the other hand, lower dose implant both in PTS and channel region enhances SCE, which also results in the smaller drive current. We found that the optimum dose condition (CI: 1×10^{12}cm^{-2}, PTS: 1×10^{13}cm^{-2}) realizes maximum I_{on} (796 μA/μm @ Vd = 0.8V) with S-swing of 64

mV/dec. In addition, we evaluated the effect of fin width (Wfin) fluctuation on the threshold voltage (Vt) of the bulk-FinFET. Fig.7 shows the simulation results of the Vt difference (ΔVt = Vt (Wfin = 10nm) -Vt (Wfin = 15nm)) in each implant condition. The previously obtained optimum dose condition corresponds to ΔVt=153mV.

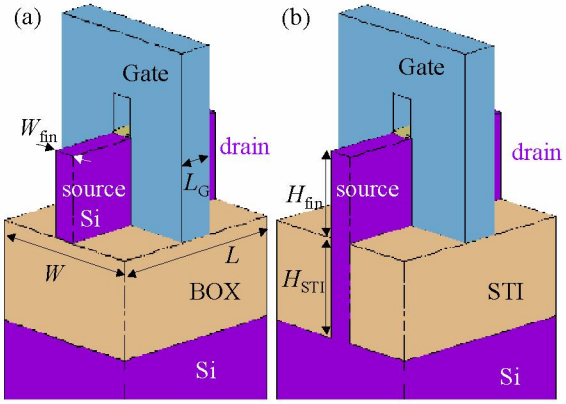

Figure 1. Bird's-eye view of SOI-FinFET (a) and Bulk-FinFET (b)

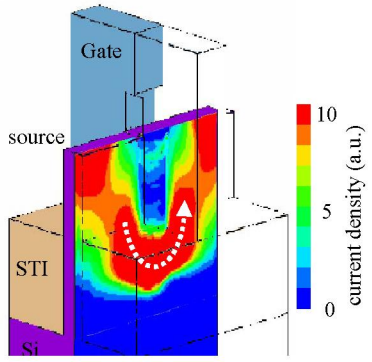

Figure 2. Cross-sectional view of current density distribution at the middle of the fin. Boron concentrartion in the fin is uniform (1×10^{17}cm^{-3}), and punch-through stopper is not formed. Drain (source) bias is 0.8V (0V), gate bias equals threthold voltage. The white arrow indicates the flow of punch-through current.

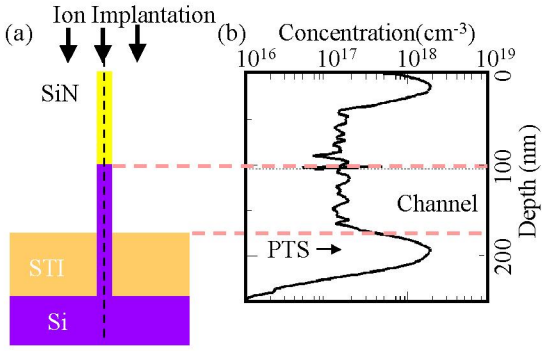

Figure 3. (a) cross-sectional view of zero tilt-angle ion implantation for punch-through stopper (PTS) formation, (b) simulated boron distribution at the dashed line in Fig. 3a.

TABLE I. SIZE OF SIMULATED FINFET.

L_G	W_{fin}	H_{fin}	L	W	H_{STI}
30nm	10nm	50nm	300nm	100nm+Wfin	70nm

NOTATIONS ARE DESCRIBED IN FIG. 1.

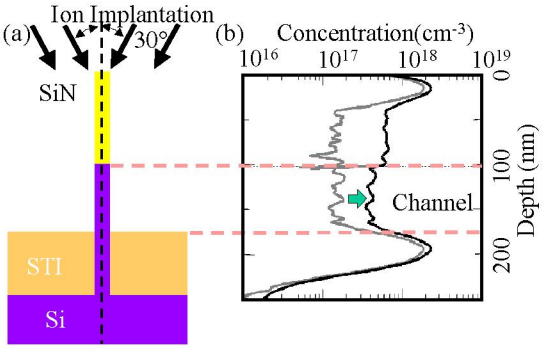

Figure 4. (a) cross-sectional view of tilt angled ion implantation for channel doping. (b) simulated boron distribution, after zero tilt-angle implantation (gray line, same to Fig. 3b) and followed by the implantation for channel doping (black line).

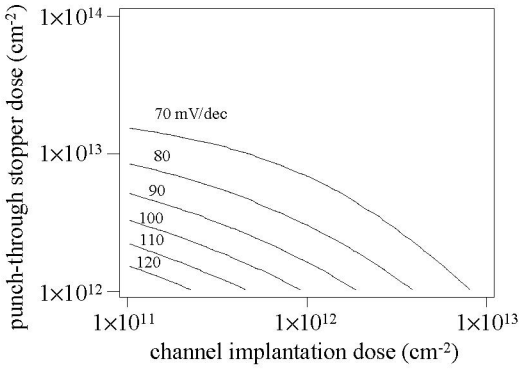

Figure 5. *S*-swing contour plot in bulk-FinFET as function of punch-through stopper dose and channel implantation dose

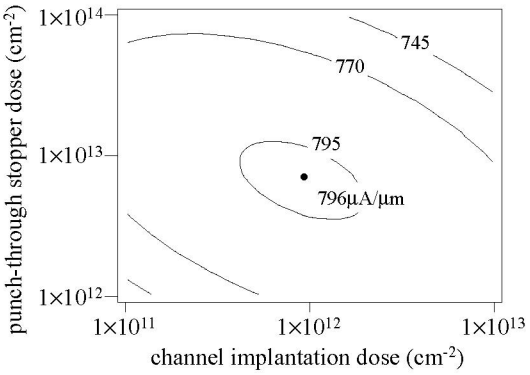

Figure 6. I_{on} contour plot in bulk-FinFET as function of punch-through stopper dose and channel implantation dose

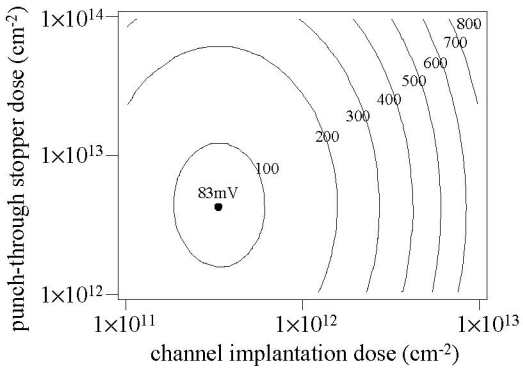

Figure 7. Contour plot of Vt difference between bulk-FinFET with Wfin=10nm and bulk-FinFET with Wfin=15nm as function of punch-through stopper dose and channel implantation dose. Gate length of each FinFET is 30nm.

III. Stress Liner and Raised Source/Drain Impact on Bulk-FinFET Structure

Next, the impact of process induced stress by a stress liner (SL) on the bulk-FinFET and SOI-FinFET is investigated (Fig 8). Fig.9 indicates the I_{on} enhancement factors both in the bulk-FinFET and the SOI-FinFET with tensile SL deposition (thickness 25nm). It is found that the SL effect on the bulk-FinFET is larger than that on the SOI-FinFET. In order to clarify the SL effect, we have investigated the stress distribution in the fin regions. Fig.10 shows the strength of stress at the bottom of channel regions in the FinFETs. S_{xx} is stress component parallel to current flow (source-drain direction), S_{yy} shows the stress component perpendicular to the side plane of the fin region, and S_{zz} indicates the stress component of depth direction. The simulation results show that the induced stress in the bulk-FinFET is stronger than that in the SOI-FinFET. The reason is ascribed to the decrease of relaxation effect of the stress in the bulk-FinFET, because the fin is connected to the Si substrate. The SL thickness dependence of the I_{on} enhancement is shown in Fig. 11, which shows saturation nature of drive current as the increase of the SL thickness.

The raised source/drain (RSD) regions are experimentally formed by selective-epitaxial growth (SEG) of Si films onto the source/drain (SD) regions (Fig.12). This figure shows that facets at the edges of the SEG region are formed [6]. In the following simulations, we use the realistic configuration of the SEG regions. Fig.13 shows an example of simulation result. In order to avoid ion penetration into the channel region through the facets in the RSD, the implantation energy, tilt angle, and twist angle as well as implant dose were carefully determined (Fig.13b). We adopted multiple tilted implantations for the RSD regions. Fig. 14 shows the implanted arsenic distribution in the cross-section at the middle of the fin after optimization. From this result, few arsenic atoms are observed in the channel region, although arsenic atoms are highly doped both in the RSD and deep source/drain (outside of the sidewalls) regions.

Finally, we investigate the effect of combination of SL effect and the RSD in bulk-FinFET. Fig.15 shows the simulation results of I_{on} as functions of the RSD thickness and the SL thickness. From this figure, we see that the dependence of RSD thickness on the I_{on} improvement is larger than that of SL thickness. In the present case, the fin width (Wfin=10nm) is very narrow, which causes large resistance in the SD region. Therefore the reduction of SD resistance by the RSD region gives rise to dominant contribution to the improvement of drive current. Fig.16 indicates Id-Vg characteristics of the bulk-FinFETs. This figure shows that the combination of RSD and SL improves the I_{on} by 22.5% at V_G-V_t= 0.6V.

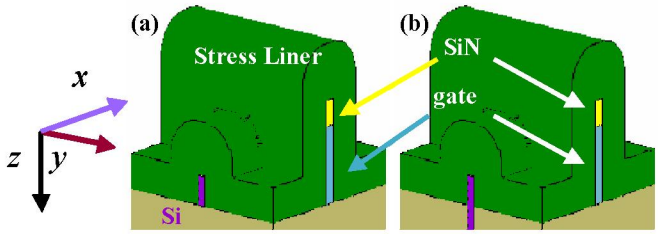

Figure 8. Bird's-eye view of SOI-FinFET (a) and bulk-FinFET (b) with stress liner

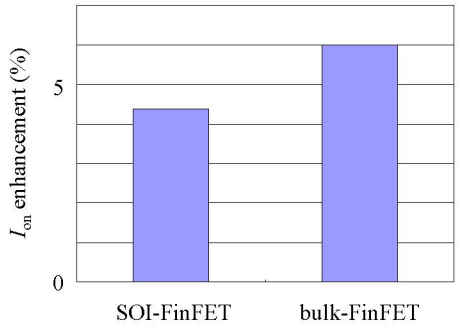

Figure 9. Comparison of I_{on} enhancement by the stress liner which is 25nm in thickness and 1.5GPa in intrinsic stress.

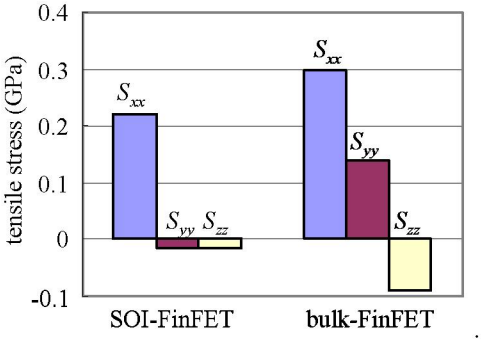

Figure 10. Comparison of three components of stress induced by stress liner. S_{xx} is stress in the current flow direction. S_{xx}, S_{yy} and S_{zz} are stress in the x, y and z direction shown in Fig. 8, respectively.

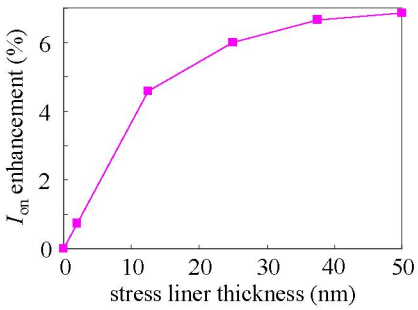

Figure 11. I_{on} enhancement dependence on stress liner thickness

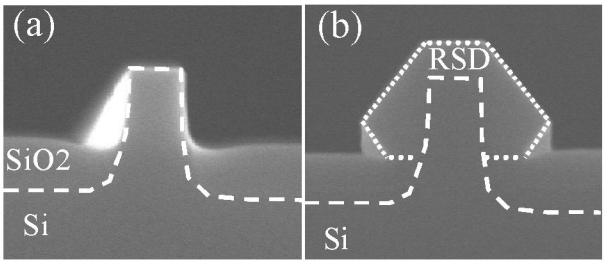

Figure 12. SEM image of source/drain region before (a) and after (b) raised source/drain process

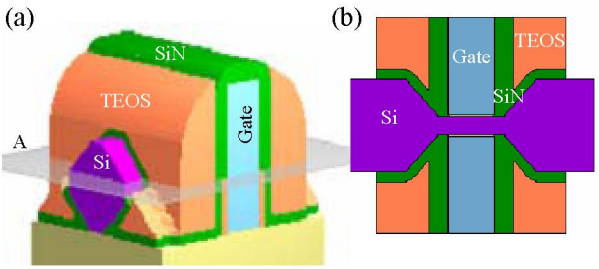

Figure 13. Simulated FinFET with raised source/drain. (a) bird's eye view; (b) cross-sectional view at plane A in (a).

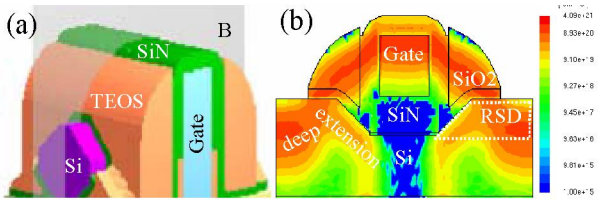

Figure 14. Simulated FinFET with raised source/drain. (a) bird's eye view; (b) arsenic distribution in cross-section at plane B in (a).

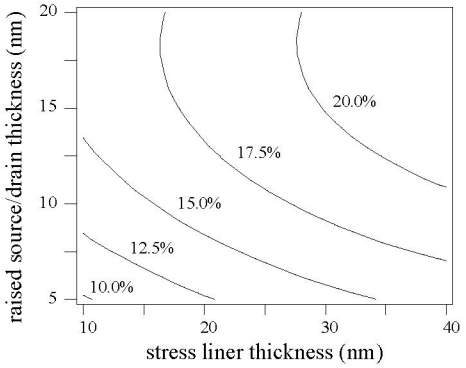

Figure 15. I_{on} contour plot as function of stress liner thickness and raised source/drain thickness

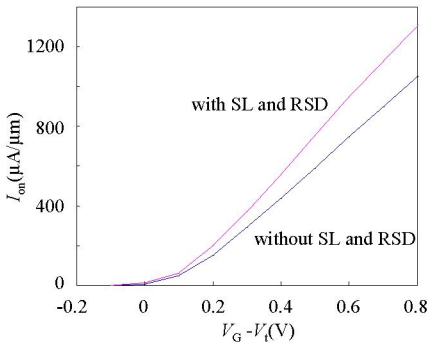

Figure 16. I_{on} as function of gate overdrive (V_G-V_t). The thickness of stress liner (SL) (raised source/drain (RSD)) is 42.7nm (21.3nm). The combination of SL and RSD improves I_{on} by 22.5% at V_G-V_t = 0.6V.

IV. Conclusion

In order to improve drive current of the bulk-FinFET, 3-D simulations were applied to optimize the channel profile and to evaluate the mobility enhancement by the SL effect, and to analyze the impact of the raised SD structure. We found that the dual channel implantation (CI and PTS) technique is efficient to control both *S*-swing and drive current. It is also found that the SL effect on the bulk-FinFET is larger than that on the SOI-FinFET. Furthermore, we found that the RSD structure largely improved drive current, although careful optimization of SD implantations is required. Therefore, the 3-D simulations are powerful tools for realizing high performance bulk-FinFET.

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