Comparison of device performance and scaling properties of cylindrical-nanowire (CNW) and carbon-nanotube (CNT) transistors

E. Gnani, A. Marchi, S. Reggiani, M. Rudan, and G. Baccarani
Advanced Research Center on Electronic Systems (ARCES), and Department of Electronics (DEIS)
University of Bologna, viale Risorgimento 2, 40136 Bologna, Italy
Email: egnani@arces.unibo.it

***Abstract*— In this work we investigate the performance of cylindrical nanowire (CNW) and carbon-nanotube (CNT) FETs at their extreme miniaturization limits. The model self-consistently solves the Poisson and the quantum transport equations using the formalism of the Quantum Transmitting Boundary Method (QTBM). The performance comparison between CNW- and CNT-FETs with the same diameter demonstrates that the CNW-FET provides a better scaling trend at very low sizes.**

I. Introduction

In the past decades, improvements in circuit performance and cost per function have been pursued by shrinking transistor geometries. Further scaling will not be as straightforward in the future as it has been in the past, because fundamental material and device limits are rapidly being approached by the bulk CMOS technology. For this reason, technology boosters and innovative structures are needed to improve the achievable device performance. New MOSFET architectures, such as ultrathin-body single- or multi-gate FETs, can in fact be scaled down more aggressively than the bulk-CMOS ones, and may become good candidates for future technology nodes. According to the ITRS 2005 [1], ultra-thin silicon devices are gaining an increasing consensus and are likely to become one of primary architectures for the 32-nm CMOS technology node. On the other hand, when the gate length of ultra-thin body (UTB) SOI-FETs is scaled down to extreme miniaturization limits, they still suffer short-channel effects (SCE) caused by the penetration into the thick buried oxide of lateral field lines originating from the drain and ending onto the source-side of the channel [2], [3]. As the channel lengths of FETs enter the deca-nanometer regime, various nonplanar, multigate (i.e., tri-gate and gate-all-around) structures have been proposed to obtain effective gate control. According to the long-term provisions of the ITRS 2005 [1], sub-10-nm channel-length FETs will be manufactured in the year 2016 for the HP22 technology node, and 5-nm channel lengths will be required for the HP14 node in the year 2020. At such scaling limits, the size of the cross section of the multigate structures must shrink to the sub-10-nm regime to maintain good electrostatic control, leading to the design of devices that become nanowire transistors. Moreover, the silicon-based technology will eventually reach its limits, and alternative concepts will become necessary in order to continue improving the density and performance of electronic devices. Among the new materials under investigation, carbon nanotubes (CNTs) have emerged as promising candidates for nanoscale electronics [4]. CNTs exhibit in fact unique electrical properties, such as large carrier mobility due to the weak electron-phonon interaction, as well as high mechanical and thermal stability; furthermore, their chemical structure and small dimensions potentially allow for a large packing density and for the fabrication of non-planar structures. Thus, the technological evolution of devices ultimately leads to cylindrical nanowire (CNW) FETs [5] and to carbon-nanotube (CNT) FETs [4].

In this work we investigate the performance of cylindrical nanowire (CNW) and carbon-nanotube (CNT) FETs at their extreme miniaturization limits. To this purpose, a home-made simulation tool has been used to carry out the analysis which fully accounts for quantum-mechanical effects on the device electrostatics and transport. The model self-consistently solves the Poisson and the quantum transport equations using the formalism of the Quantum Transmitting Boundary Method (QTBM). Previous investigations, based on the non-equilibrium Green's Function (NEGF) approach [6], have shown that quantum simulation captures the essential physical effects of these device structures (see, e.g., [7]). A high number of simulations has been run to provide an extensive performance analysis of such devices. The latter investigation has been carried out for both CNW- and CNT-FETs with the same diameter in order to compare the numerical predictions and show how such novel devices answer to the performance requirements of the ultimate scaling limits.

II. Device Simulation

A full-quantum transport simulator is used to provide some insight on the upper-limit performance of the devices investigated in this work, whose schematic structures are shown in Fig. 1. Due to the cylindrical symmetry in CNTs and to the structural quantum confinement in the radial and angular directions in the CNWs, the conduction band is split into energy subbands along the transport direction for both devices. In the CNT device, the intervals between the energy levels are fixed by the geometry only, because the charge is fully localized at the surface of the nanotube [8]. At each point along the channel the energy reference is prescribed

 1-4244-0404-5/06/$20.00

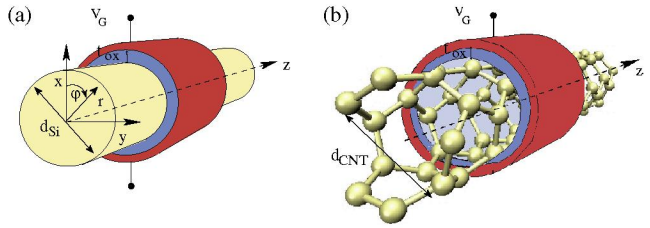

Fig. 1. The analyzed structures: CNW-FET (left), CNT-FET (right).

by the electric potential. In contrast, in the CNW structure the intervals between the energy levels are influenced also by the shape of the electric potential over the cross section. As a consequence, the transport problem must be tackled by coupling the solution of the Schrödinger equation over each cross section with that of the 1D transport problem. In the transport direction the Schrödinger equation is solved using the QTBM method. The latter is used with traveling waves at the boundary points of the simulation region in order to obtain open boundary conditions [9]. Within the solution procedure it is necessary to take into account narrow resonances at some energies for the calculation of the electron charge density. To achieve the desired accuracy an adaptive procedure based on the Simpson quadrature [10] has been implemented during the scanning of the energy interval. The Schrödinger equation is solved within the effective-mass m^* approach, which proves to be valid for structures with thicknesses down to 1 nm [11]. The analysis of the change in m^* with diameter is beyond the scope of this work and is not addressed here. For the CNT-FET the mass value has been chosen so as to obtain the same equilibrium inversion charge as that given by the universal density of states of [12]. Consequently, the material properties are fully accounted for. Finally, the Schrödinger solution is self-consistently coupled with the Poisson equation using a Newton-Raphson scheme. The Jacobian matrix is computed at each iteration by numerically differentiating the space charge.

III. Results and Discussion

The numerical analysis is carried out on devices with geometrical and electrical requirements that follow those provided by the ITRS 2005 [1]. We examine devices with channel lengths and diameters varying from 1 to 5 nm. An intrinsic material is assumed within the channel; heavily-doped source and drain regions are used with ohmic contacts at the ends. Abrupt junctions are taken into account in both devices to provide a clear definition of the channel length. The metal work function is chosen so that $I_{\text{off}} = 108$ nA/μm as indicated by the ITRS. The most important parameters of the investigated devices are reported in Table I along with some key material properties. We assume $V_{DD} = 0.8$ V and fix the oxide thickness at 0.5 nm.

A preliminary analysis is carried out by comparing the full-quantum with the quantum drift-diffusion (QDD) solution (see Figs. 2, 3 and 4). The quantum drift-diffusion transport model is based on an improved drift-diffusion approach, supporting both planar and cylindrical structures, which takes advantage

TABLE I

Main technological parameters for the simulated devices

	CNW	CNT	CNT	CNT
Diameter (nm)	1, 2, 5	1	2	5
L_g (nm)	1, 2, 5	1, 2, 5	1, 2, 5	2, 5
EOT (nm)	0.5	0.5	0.5	0.5
E_G (eV)	1.12	0.720	0.360	0.144

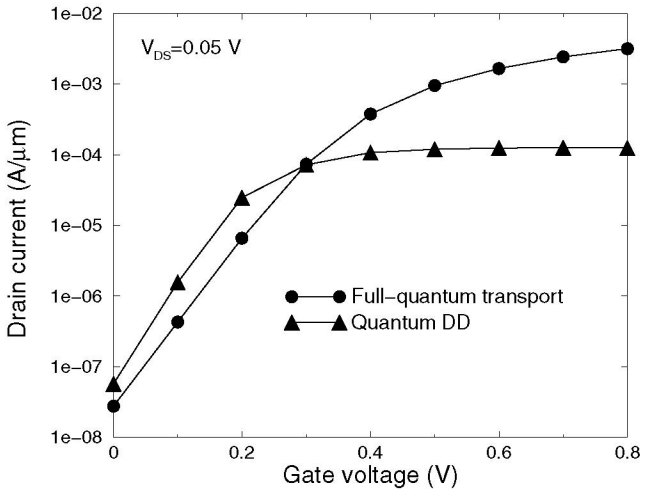

Fig. 2. Turn-on characteristics at $V_{ds} = 0.05$ V of a CNW-FET with a 2-nm-diameter silicon body and a 5-nm gate length, using the full quantum-transport solution and the quantum drift-diffusion one. The former is not affected by the strong reduction in the drain current due to mobility degradation that occurs at very thin silicon diameters. The subthreshold slope is higher for the quantum model due to source-to-drain tunnelling.

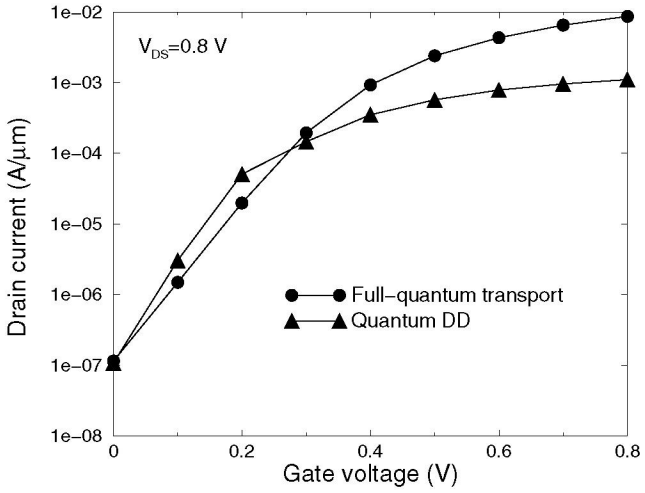

Fig. 3. Turn-on characteristics at $V_{ds} = 0.8$ V of a CNW-FET with a 2-nm-diameter silicon body and a 5-nm gate length, using the full quantum-transport solution and the quantum drift-diffusion one. The same considerations given for Fig. 2 are also valid for this comparison.

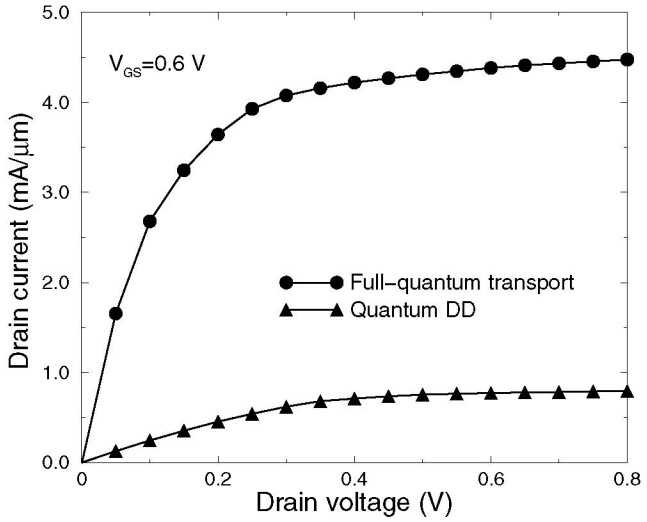

Fig. 4. Output characteristics of a CNW-FET with a 2-nm-diameter silicon body and a 5-nm gate length, using the full quantum-transport solutions and the quantum drift-diffusion one at $V_{GS} = 0.6$ V. Due to the low mobility values, the quantum DD solution provides a much lower current and a larger saturation voltage. Hence, the discrepancy between the two solutions is substantial.

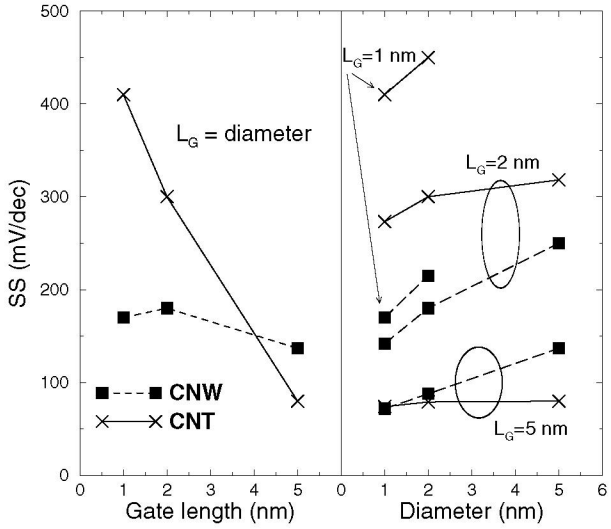

Fig. 5. Left: subthreshold slope vs L_g for CNW- and CNT-FETs. In this plot, the device diameter is kept equal to the gate length. Right: SS vs diameter for different gate lengths. The CNW-FET provides a better scaling trend at the extreme miniaturization limits.

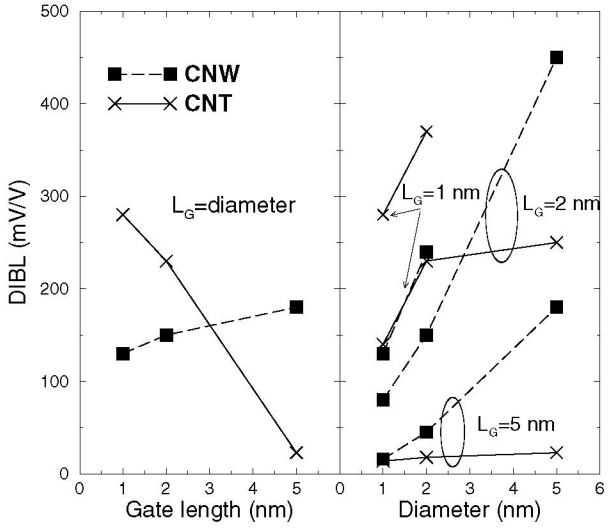

Fig. 6. Left: DIBL vs L_g for CNW- and CNT-FETs with the gate length equal to the device diameter. Right: DIBL vs diameter for different gate lengths. The CNW-FET provides a better DIBL at the extreme miniaturization limits.

from the exact computation of the carrier density and, thus, does not rely on the density-gradient approximation. More specifically, we solve a 2D Poisson equation coupled with as many 1D (normal to the channel) Schrödinger equations as the number of mesh points along the channel. We integrate the non-linear Poisson equation by the Newton-Raphson method, and compute the Jacobian matrix at each iteration by numerically differentiating the space charge. A more detailed description of this method can be found in [8]. The Schrödinger-Poisson solution is then coupled with a 2D quantum drift-diffusion solver, which allows us to determine the electron quasi-Fermi potential within the device. The knowledge of the electron concentration n and of the potential ϕ leads to the "quantum potential" Λ, which is computed from the standard relationship $n = n_i \exp[q(\phi - \phi_n - \Lambda)/k_B T]$. This term is then added to the potential ϕ within the Bernoulli function of the discretized drift-diffusion equations. The QDD approach avails itself of a new compact carrier mobility model, which has been worked out along the lines indicated by [13] for SiO_2 insulated-gate SOI-FETs, and which has been compared with experiments for different silicon thicknesses down to t_{Si} = 2.48 nm.

As shown by Figs. 2 and 3, the main discepancies are given by a different subthreshold slope and a substantially-different on-current. In the subthreshold regime, the quantum mechanical (QM) tunnelling through the source-channel barrier gives an additional contribution to the current, increasing the carrier density in the channel and degrading the subthreshold slope (SS). As far as the on regime is concerned, the large discrepancies are due to the strong mobility degradation occurring in the Quantum DD case at very thin silicon diameters. This is also shown by the output characteristics in Fig. 4, where the predictions given by the QDD model show a much lower current and a larger saturation voltage. This preliminary comparison quantifies the importance of quantum physical effects to asses the device performances with respect to the typical metrics.

To provide a first comparison between CNW- and CNT-FETs, we plot the SS in Fig. 5 and the DIBL in Fig. 6. A preliminary work was carried out to find out the best aspect ratio (gate length over diameter) for the investigated devices: we found that $L_g/d \approx 1$ gives acceptable values of subthreshold slope (SS) and drain-induced barrier lowering (DIBL) for both devices with gate lengths down to 5 nm. By further scaling

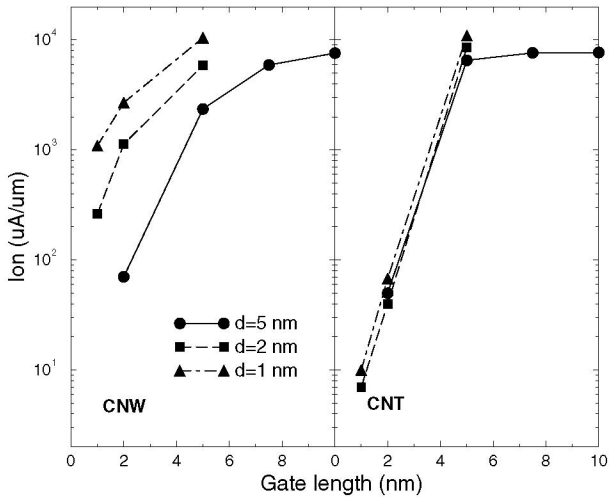

Fig. 7. $I_{\rm on}$ current for the CNW- (left) and CNT- (right). For small gate lengths the CNT-FET provides low on-currents because the high SS prevents the device from turning on. A similar trend is obtained for all diameters.

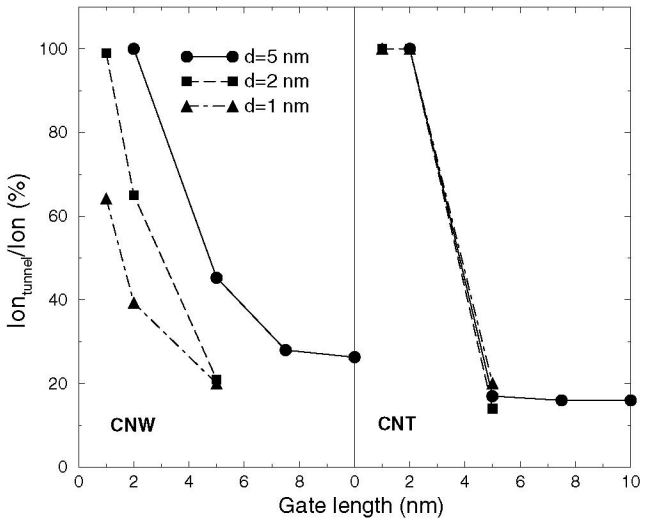

Fig. 8. Tunnelling and total current ratio in the on-state for the CNW- (left) and CNT-FETs (right). For small gate lengths, the reduced SS prevents the device from turning on: therefore, the fraction of tunnelling current increases.

down the devices using the same aspect ratio we found that the CNT device is more affected by short-channel effects that the CNW one (see Figs. 5 and 6, left). This can be ascribed to the intrinsic material differences, which become relevant when a strong splitting of the energy levels is present, due to the strong structural quantum confinement. The better scaling trend at the extreme miniaturization limits is provided by the CNW also when a higher aspect ratio is used: to see this, we plotted the SS and DIBL as a function of the diameter for different gate lengths in Figs. 5 and 6, right.

The $I_{\rm on}$ results are compared in figure 7 for different diameters as a function of the gate length. $I_{\rm on}$ is computed as $I(V_{gs} = V_{ds} = 0.8V)$. For small gate lengths the CNT-FET provides lower on-currents because the poor SS prevents the device from turning on. In figure 8, the ratio between the tunnelling and total on-current is shown as a function of the gate length. The tunneling contribution increases with decreasing gate length for both devices at any diameter, showing an abrupt behavior for the CNT-FET at gate lengths lower than 5 nm.

IV. Conclusion

A full-quantum-transport simulation approach is developed to investigate emerging devices indicated as candidates by the ITRS for future technology nodes. By investigating the overall performance of CNW- and CNT-FETs, it turns out that the former provides a better scaling trend for very low sizes.

Acknowledgment

This work has been partially supported by the EU IST Network SINANO (contract n. 506844).

References

[1] "International technology roadmap for semiconductors 2005 edition," http://public.itrs.net.

[2] B. Doris, M. Ieong, T. Kanarsky, Y. Zhang, R. Roy, O. Dokumaci, Z. Ren, F. Jamin, L. Shi, W. Natzle, H. Huang, J. Mezzapelle, A. Mocuta, S. Womack, M. Gribelyuk, E. Jones, R. Miller, H.-S. Wong, and W. Haensch, "Extreme scaling with ultra-thin Si channel MOSFETs," in *International Electron Devices Meeting, 2002. IEDM '02. Digest.*, 8-11 Dec. 2002, pp. 267–270.

[3] B. Doris, M. Ieong, H. Zhu, Y. Zhang, M. Steen, W. Natzle, S. Callegari, V. Narayanan, J. Cai, S. Ku, P. Jamison, Y. Li, Z. Ren, V. Ku, D. Boyd, T. Kanarsky, C. D'Emic, M. Newport, D. Dobuzinsky, S. Deshpande, J. Petrus, R. Jammy, and W. Haensch, "Device Design Considerations for Ultra-Thin SOI MOSFETs," in *International Electron Devices Meeting, 2003. IEDM '03. Digest.*, 8-11 Dec. 2003, pp. 631–634.

[4] P. Avouris, J. Appenzeller, R. Martel, and S. J. Wind, "Carbon nanotube electronics," *Proc. IEEE*, vol. 91, no. 11, pp. 1772–1784, 2003.

[5] F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu, C.-C. Huang, T.-X. Chung, H.-W. Chen, C.-C. Huang, Y.-H. Liu, C.-C. Wu, C.-C. Cheng, S.-C. Chen, Y.-T. Chen, Y.-H. Chen, C.-J. Chen, B.-W. Chan, P.-F. Hsu, J.-H. Shieh, H.-J. Tao, Y.-C. Yeo, Y. Li, J.-W. Lee, P. Chen, M.-S. Liang, and C. Hu, "5nm-gate nanowire FinFET," in *2004 Symposium on VLSI Technology, 2004. Digest of Technical Papers.*, 15-17 June 2004, pp. 196–197.

[6] J. Wang, E. Polizzi, and M. Lundstrom, "A Computational Study of Ballistic Silicon Nanowire Transistors," in *International Electron Devices Meeting, 2003. IEDM '03. Digest.*, 2003, pp. 695–698.

[7] J. Guo, A. Javey, H. Dai, and M. Lundstrom, "Performance Analysis and Design Optimization of Near Ballistic Carbon Nanotube Field-Effect Transistors," in *International Electron Devices Meeting, 2004. IEDM '04. Digest.*, 2004, pp. 703–706.

[8] A. Marchi, E. Gnani, S. Reggiani, M. Rudan, and G. Baccarani, "Investigating the performance limits of silicon-nanowire and carbon-nanotube FETs," *Solid State Electronics*, vol. 50, pp. 78–85, 2006.

[9] C. Lent and D. Kirkner, "The quantum transmitting boundary method," *J. Appl. Phys.*, vol. 67, no. 10, pp. 6353–6359, 1990.

[10] "Numerical Recipes," http://www.nr.com.

[11] S. Horiguchi, "Validity of effective mass theory for energy levels in Si quantum wires," *Physica B*, vol. 227, pp. 336–338, 1996.

[12] J. W. Mintmire and C. T. White, "Universal Density of States for Carbon Nanotubes," *Phys. Rev. Lett.*, vol. 81, no. 12, pp. 2506–2509, 1998.

[13] K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata, and S. Takagi, "Experimental study on carrier transport mechanism in ultrathin-body SOI nand p-MOSFETs with SOI thickness less than 5 nm," in *International Electron Devices Meeting, 2002. IEDM '02. Digest.*, 8-11 Dec. 2002, pp. 47–50.