TCAD as an integral part of the semiconductor manufacturing environment

(Invited Paper)

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***Abstract*— This work shows a new methodology which automates the necessary links between technology computer aided design (TCAD) and the semiconductor manufacturing environment to a high extent. Initially a short overview of a typical chain of processes during the fabrication of an integrated circuit is given. Furthermore an overview on the relations to the respective simulator tools is given.**

The interfaces between the fabrication process and simulation are identified and the detailed structure of the interfaces is outlined. A comprehensive overview over the interactions in this integrated system is given as well.

Finally the strengths of such a structured and integrated approach are demonstrated with a case in a real semiconductor fabrication environment.

I. Introduction

This work concentrates on technology computer aided design (TCAD) [1] and its integration into the semiconductor fabrication process flow. The use of TCAD is twofold: Firstly it models the complex flow of semiconductor fabrication steps ending up with detailed information on geometric shape and doping profile distribution of a semiconductor device in scope (like CMOS- or Bipolar-Transistors). Secondly it uses the information of the first step to predict the device characteristics of semiconductor devices leading to circuit simulation models as implemented in any circuit simulator like PSPICE [2], ELDO [3], SPECTRE [4] etc. The setup of such a simulation methodology requires an almost completely documented semiconductor fabrication process flow including such fabrication details like angle of incidence of ions implanted in ion implantation process steps, or etch rate distribution as a function of the local angle of the etched layer surface. Any modern semiconductor fabrication facility maintains such documentation to an extremely high detail level, but commercial TCAD simulation software like Synopsys [5] or Silvaco [6] tools need this information in a very specialized format [7] which cannot be directly deduced from the standard process flow documentation. The traditional way of setting up the process- and to some extent also the device TCAD-simulation framework is, entering it by hand, which is of course a source of numerous errors. This work shows a new methodology with the main target to automate the necessary links to the manufacturing environment to a high extent. After outlining the two "worlds" of TCAD and manufacturing in Section II and Section III and showing the concept used for connecting them both together in Section IV an example of a successful implementation of the proposed methodology is given in Section V

II. The Processing Chain in Semiconductor Manufacturing

A. Overview

The semiconductor industry is starting from the product idea the following sequential steps occur in a standard integrated circuit development and production flow [8].

1) Development: Starting from the product idea, the electronic contents of the overall system are developed, leading into a schematic of the electronic circuitry. For digital circuitry this development process is similar to writing a software program by using *Very High Speed Integrated Hardware Description Language* (VHDL) as a abstract description of the digital block. The development of a digital block starts with the specification (operation and timing) and the subsequent description of this specification via a model in VHDL.
2) Design: The integrated circuit is designed starting from the schematic, and taking into account the special demands of integrated circuits (crosstalk, common substrate, etc.). It is state of the art to use ECAD (electronic computer aided design) tools to simulate the behaviour of a design as an integrated circuit by using detailed circuit simulation models and design rules, which are specific to a process family (technology node) [9].
3) Layout: The resulting integrated circuit is drawn as a layout on the specific layers which are given by the semiconductor process family (technology node). The combination of multiple layers, like implantation masks and etch masks, define the shape and functionality of the electronic devices in the integrated circuit [10].
4) Mask-Shop: The layout is post processed to take into account process induced size variations (layer biasing) and constraints on combination of layers (logical combination). The physical mask layers are written from this data by using laser- [11] or e-beam [12] equipment.
5) The wafer start material is released at the beginning of the process flow into fabrication [13]. In the following

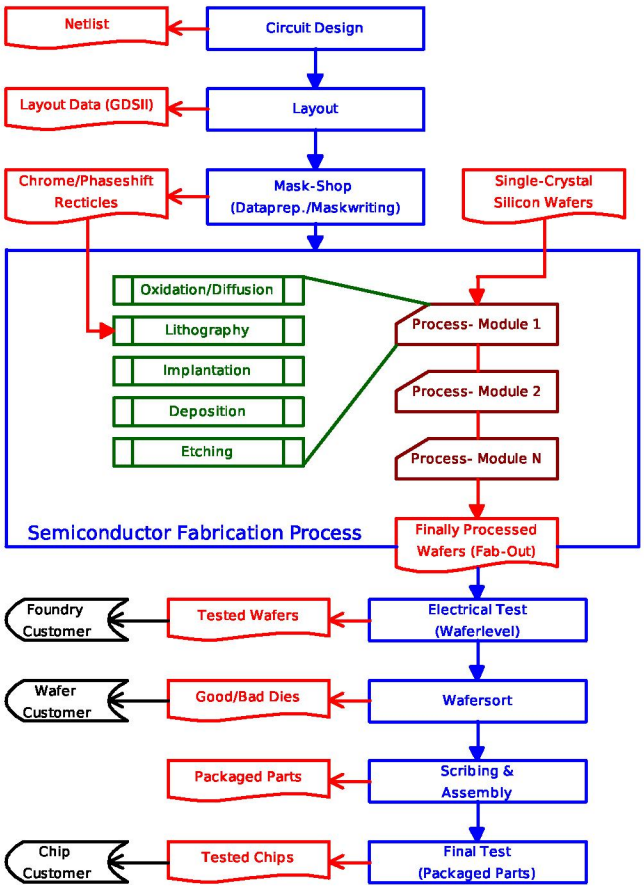

Fig. 1. Processing chain of integrated circuit production

these wafers are subject to numerous single process steps like ion-implantation, deposition and etching of semiconductor, dielectric, and metallic materials, furthermore diffusion of dopants, and oxidation and lithography to structure deposited layers using the previously fabricated mask reticles.

6) After leaving the fabrication the now functional integrated circuits are tested electrically. Firstly on single device level on process control monitors (PCM's), secondly on full device level (wafer sort). These tests select the functioning parts for further processing.
7) Scribing into pieces and packaging of the single circuits.
8) Electrical functionality test of the packaged pieces.

The overall processing chain is shown in Figure 1 .

The ECAD simulation tools in Subject 1 , Subject 2 , and Subject 3 are already closely integrated into the development chain [14] and are therefore very efficient.

Packaging simulation is not subject to this work, however, tools [15] are used to analyse new packages with respect to electromagnetic field, stress, and self heating.

For Subject 4 to Subject 6 good simulation solutions exist for the single process step e.g. SIGMA-C or PROLITH [16] for lithography and mask fabrication step simulation, TCAD Tools from Synopsys and Silvaco for the process- and device-simulation steps), which are sufficient for most of the two-dimensional process- and device-simulation applications.

However, the set-up of these TCAD-simulators is highly complicated and time consuming. Changes in fabrication procedures like parameter optimization of process conditions are not reflected in simulation with the traditional way of defining this set-up by hand. Therefore the simulation flow definitions become asynchronous to the semiconductor fabrication very quickly.

The main concept to be considered is to match the simulation methodology as closely as possible to the fabrication methodology in an automatic (or at least semi-automatic) way. The resulting work flow and the main application areas for TCAD integration into fabrication can be seen in Figure 2 .

B. Description of Semiconductor Manufacturing Processes

A semiconductor manufacturing process differs markedly from other processes. In many other types of processing plants, the material being processed moves through the plant in a fairly simple, straightforward, and well-integrated manner. Despite the fact that the processing flow of this material is straightforward and linear, a flow chart depicting the process will usually be quite complicated. Contrast this with a semiconductor manufacturing process, which can be described very easily with a linear processing flow chart, but whose work-in-process (WIP) moving through the plant will follow very complex paths. During wafer processing - i.e. in the semiconductor fabrication clean-room - the integrated circuitry is formed at the surface of the single crystal silicon wafer by numerous repetitive micro-lithographic, deposition, diffusion, and etching steps, until it is finished. During this processing, depending on the complexity of the technology, a set of about fifteen up to more than thirty-five separate wafer processing cycles (which form modules like gate module, lightly doped drain (LDD) module, metal module and so on), including the associated lithography step, were performed. An expanded flow chart of one of these cycles appears as shown in Figure 3 .

Here it can be seen that the wafer will iterate through this inner circle as many times as there are masks(alignments)[1] for adding new circuitry.

III. TCAD Concept Overview

The different levels of functionality of the TCAD system are shown in Figure 4 .

The purpose of the process simulation is to provide the structural information of the device under scope, consisting of the boundary including the composition of the different materials involved (e.g. polycrystalline silicon, single crystalline silicon, silicon dioxide, metals etc.). In addition, the doping concentration inside the silicon has to be available. The process simulation takes the photo mask information and the process flow to model the evolution of above mentioned

[1]One has to carefully distinguish between the terms "mask" and "alignment". A mask is the physical reticle for the illumination process. An alignment is the group of steps performed in a lithography track as shown in Figure 3 in the box. The number of masks and alignments is normally not equal, because certain reticles may be used for more than one alignment.

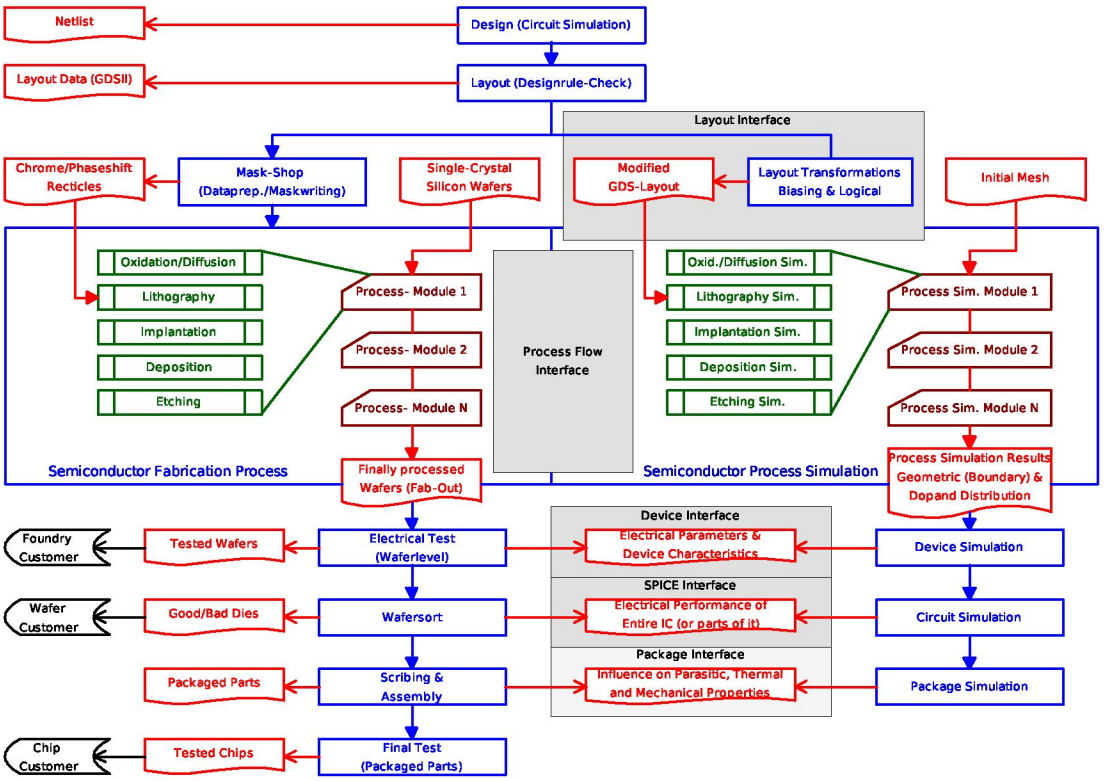

Fig. 2. Structure of the semiconductor process flow and its mirror image the TCAD simulation flow. The interfaces between TCAD and semiconductor fabrication are identified as well.

information (boundary and dopant) over the multiple steps of the process.

The mesh for solving the partial-differential equations (PDEs) typical for the physical and chemical processes occurring during processing is normally of unstructured type, to model the steep gradients of the doping distributions with good accuracy, but with a low number of mesh points where the physical fields (doping concentration, point defect concentrations etc.) are not varying much. A detailed description of a process simulator can be found in, e.g., [17]

The boundary and dopant information is then used as an input to describe the electrical behaviour of the device under scope by calculating the potential distribution and the carrier transport phenomena (current concentrations etc.) via solving the PDEs describing their physics. A detailed description of the underlying principles of a device simulator can be found in, e.g., [18]

Since the requirements on meshes for process and device simulations, respectively, are very different, a re-meshing step is necessary to minimize the numerical error, and the number of mesh points necessary for a certain accuracy of the solution. This re-meshing is normally based on the gradient or difference refinement criteria. In some cases this approach is not sufficient to get a good mesh. The inversion region of a MOSFET channel is a good example for the problems gradient refinement criteria are facing. However in recent investigation approaches are outlined to overcome or, at least, to tackle these limitations [19].

IV. Integration between Semiconductor Fabrication and TCAD

The shaded areas in Figure 2 indicate the different interfaces identified between "reality" and "simulation".

A. Between Design/Layout as Process Simulation Input

According to the work flow outlined in Section III , the layout of the masks is one of the two main inputs for process simulation.

Normally this layout is available in GDSII-binary format which can be read by any of the above mentioned commercially available TCAD tools. To mirror the activities carried out in the mask shop this data must undergo the same transformations as in reality listed in Subject 4 of Subsection II-A. The "Mask Generation Instructions" define special boolean operations to modify the mask data in a way that certain effects of wafer processing are cancelled out. Examples for possible corrections like simple mask biasing or proximity corrections.

Figure 5 shows the detailed structure of the identified interface as motivated by the real mask generation and lithography process. The GDSII data is converted into the ASCII formatted CIF format (for easier processing) This data is then subject to boolean and biasing operations as defined by the mask generation instructions. To emulate the real shape of the photoresist a proximity correction is applied and the resulting contours are written back to a CIF format serving as mask information input during the process simulation.

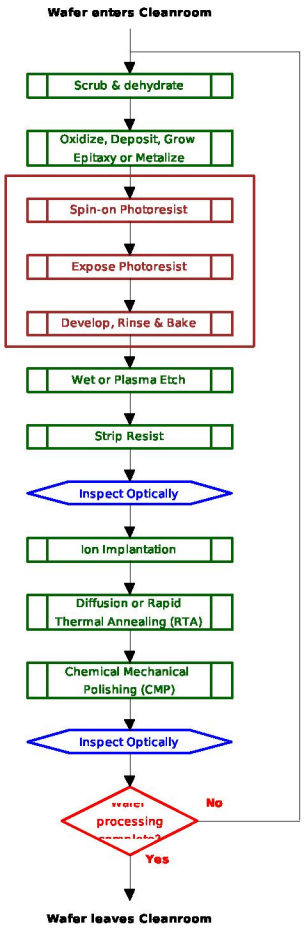

Fig. 3. Expanded flow chart of the wafer fabrication cycle comprising one alignment step and the associated processing

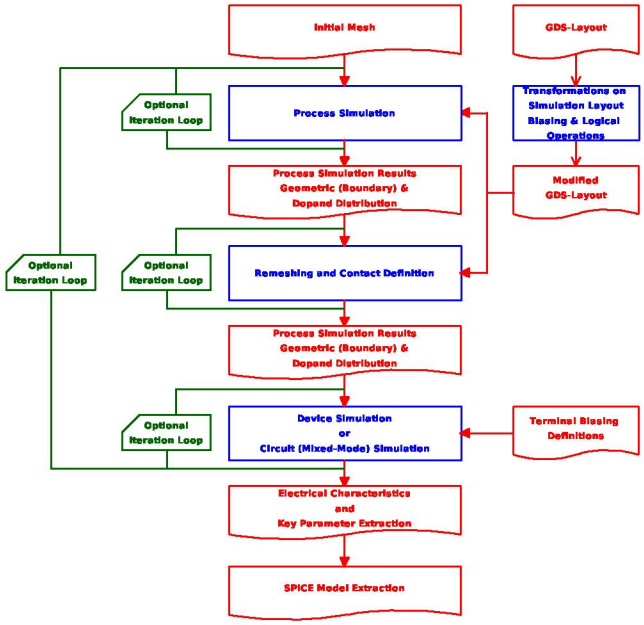

Fig. 4. TCAD work flow scheme showing possible iteration loops

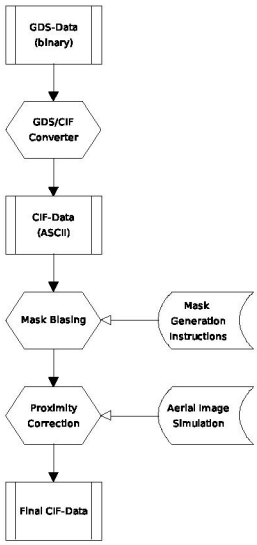

Fig. 5. Interface of layout-data to simulation mask-data

B. Between Process Flow Description and Process Simulation Command File

The overall process flow information is typically documented in the database of a manufacturing execution system like PROMIS from Brooks-PRI, SiView from IBM, or WorkStream from AppliedMaterials. The information relevant for process simulation inside this database is numerous, depending on the detailed level of the simulation models. Normally the following datasets are needed for process simulation:

1) Sequence of process steps representing the semiconductor process flow (oxidation ⇒ layer thickness measurement ⇒ implantation ⇒ diffusion ⇒ material deposition ⇒ lithography etc.)
2) Blocks of process sequences which are carried out on the same semiconductor fabrication equipment and are normally organized as program sequences like oxidation/diffusion programs which can consist of up to dozens of single process steps with different temperatures (temperature ramps) and gas ambients (gas steps or ramps).
3) The detailed process parameter set of one single process step (e.g. ion species and composition, ion dose and energy, angle of incidence and rotational orientation of ion beam with respect to wafer, ion beam divergence, etc., for ion implantation)
4) Positions in the full semiconductor process flow where selected physical characteristics like layer thickness or sheet resistances are measured by using metrology tools on wafer level.

Subject 1 through Subject 3 represent the hierarchy levels from highest to lowest. It is advisable to use an abstract representation of data as an intermediate format between the process step information and the simulation command file. Since commercial simulators and simulators from university are still under heavy development, syntax changes of the

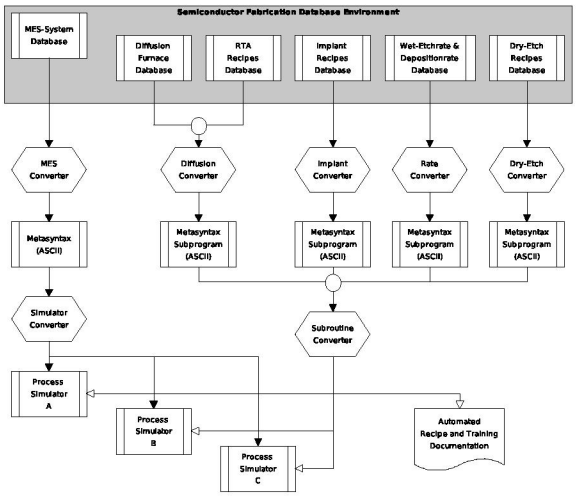

Fig. 6. Interface of process flow information to process simulation command files

simulator command files are happening frequently. Therefore a direct translator between process flow information and simulation is inflexible and difficult to extend. With an intermediate abstract format different types of simulators can be supported by a single source of data (see Figure 6).

Typically the Manufacturing Execution System (MES) is not storing the full details of the diffusion and oxidation recipes, the plasma etch programs or the etch and deposition rates of the wet chemistry used during semiconductor processing. This information is stored in separate databases as outlined in Figure 6 . Normally there is only a reference to a machine recipe or a etch sink given in the MES flow. Again the strategy of exactly mirroring the real situation was chosen to set up the interfaces. The recipes are transferred by a converter into the meta-syntax and are then converted into the simulator syntax of the process simulator chosen. This procedure is shown on the left hand side of Figure 6 . The converted recipes are then transferred into a subroutine format, provided by every commercial or university simulator available. Thus this approach can be used for every TCAD environment available. Furthermore, through the use of a meta-syntax the interpretation of the data formats inside the manufacturing system (MES and recipe databases) and the conversion into the different simulator syntaxes can be treated in a more systematic way, since both tasks cannot interfere in a single program but are performed in a modular way. Last but not least the meta-syntax enables a very compact and concise overview about the details of the semiconductor process flow. Thus, this syntax can be used as a source for a very sophisticated process flow description for documentation and training (see [20]).

C. Between Electrical Test and Device Simulation

After finished processing of the silicon wafers the first electrical test is the measurement of simple test structures and devices organized in Process Control Monitors (PCM) in the

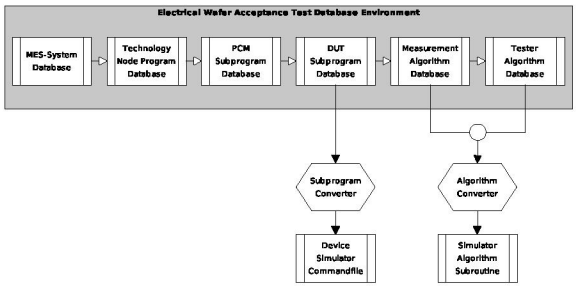

Fig. 7. Interface of electrical wafer acceptance test information to device simulation command files

scribe-lines of the wafer. These measurements are carried out on automated tester systems on wafer level. The measurement procedures are again hierarchically oriented in the following way:

1) Measurement program set up for actual technology node.
2) Subprogram defined for actual PCM (normally several PCMs are inserted in the scribe-lines).
3) Module for device under test (DUT) consisting of single program statements measuring relevant electrical parameters.
4) Single measurement algorithms for e.g. CMOS threshold voltage, or diffusion sheet-resistance.
5) Single steps of carrying out the measurement algorithm for e.g. CMOS threshold voltage in saturation. These steps define how the device terminals are connected to the voltage and current sources of the automated tester and how the currents and voltages of the DUT are measured.

Subject 3 to Subject 5 are mirrored on the device simulation side to provide comparable electrical data of measurements and simulation.
Since the algorithms under Subject 4 and Subject 5 are not changing frequently (the algorithms under Subject 5 are fixed[2] with the hardware of the automated tester used and measurement algorithms defined under Subject 4 are only changing, if a completely new device type is introduced) these algorithms are not converted on a daily basis. The structure of the interface is shown in Figure 7 . The subprogram conversion of the DUT modules is carried out much more frequently on a daily basis.

There are two main application areas existing for converting electrical test programs. First, this conversion is used for the automated generation of big device test-chips during process development including new device architectures. Second, the standard PCM structure measurement algorithms have to be converted to match the simulation results with the PCM measurements.

[2]these algorithms are typically provided by the tester vendor in the form of test libraries

D. Between Device Characterization and Device Modeling (SPICE)

This interface deals with the generation of reliable device models for circuit modeling (e.g. SPICE). The main devices (NMOS/PMOS transistors for standard CMOS processes and, in addition, bipolar transistors for BiCMOS processes) of any new process fabrication must be characterized completely in terms of output characteristics, transfer characteristics, amplification, etc. This task results in scalable electrical models (BSIM3 for CMOS, VBIC for Bipolar transistors) or compact models for circuit simulation. In the TCAD fabrication integration scheme the source for this fitting procedure can be twofold: First, the usual way of measuring the characteristics on semiconductor wafer material and second, by simulating these characteristics with device simulation. The second approach has the enormous advantage of getting worst case predictions [21], [22], which are directly related to process parameter changes by applying statistical variations on selected semiconductor process step parameters (e.g. selected implantation doses). Furthermore, combined process and device simulations without the existence of any semiconductor material can generate preliminary models very early in the process development stage. Unfortunately the generation of SPICE models (e.g. BSIM3.3 or BSIM4 with hundreds of free parameters) is not an automated straightforward task. The process characterization engineers have to set up many initial values for starting the optimization of actual SPICE models and have to follow a complicated iterative strategy to get a good model with reasonable accuracy. Therefore an automated global optimizer for generating a good SPICE model is not available. Currently the only way to get so called "TCAD based models" is to generate characteristics with device simulation as they were measured on a real device and submit this information to process characterization engineers for the generation of SPICE models. Nevertheless, this approach enables the generation of a design environment of a new technology in a very early stage of a process development. The time to market for new process technologies is thus significantly reduced.

E. Package Modeling Interface

Since package modeling does not have a key focus in this work, the corresponding interface is not discussed in detail. However it would be beneficial to implement such a conversion into the overall TCAD flow. Since commercial package simulators provide a compact model (sub-circuit) of the parasitic elements introduced by the package, especially for RF and power applications this additional input could be very helpful. Currently this conversion is performed by hand or, more typically, not considered at all in the design process.

V. Using TCAD with SPC

A. Introduction

A semiconductor fabrication process consists of several hundred unit process steps, each of which is subject to potential misprocessing. Such misprocessing typically occurs when wrong tool recipes are loaded and executed, or process steps are accidentally left out or performed twice. Although many of these issues are immediately detected at the next process step because of the physical deviation of the wafers from their usual appearance, some of these misprocessed wafers make their way through the whole production line and the failure is only detected at electrical parameter test. In such cases it is paramount that the cause of the failure is identified as quickly as possible to prevent other wafers in the fabrication line from being misprocessed the same way.

One special group of unit processes that is of particular interest in this context is the group of implant steps. Advanced semiconductor process flows contain several dozens of different implant steps, and since the implants do only affect the electrical, but not the mechanical or optical properties of the semiconductor wafers, a missing or double implant will typically be detected only at electrical test. Although large efforts have been made to prevent implant accidents, a certain risk remains in every not fully automated semiconductor fabrication facility.

Unfortunately, the relationship between the implants performed and the electrical behavior of the semiconductor devices is of high complexity, and the inference from the electrical data obtained at test to what actually happened during production requires the judgment and experience from device engineering experts.

In the following an approach is shown, how this inference can be made by a broader range of personnel with an even higher level of certainty.

During recent years, simulation techniques for semiconductor processing have been developed at a breathtaking speed. It is therefore feasible today, to feed a process flow, including all relevant process parameters, into a TCAD simulation, thereby creating a virtual semiconductor device such as a typical transistor, and extract the electrical properties of this simulated device. Parameters such as thresholds, saturation currents, sheet resistances or similar can thus be calculated for almost any given process flow.

So far, TCAD simulation has been extensively used for process development, but its application for manufacturing control and corrective action was very limited, which is partly due to the fact that its application needs skilled specialists. The advantages, of running a complete set of TCAD simulations of a transistor device for the process of record (POR), and for all process flows that result from both, an accidental missing and double implant (for each implant step), are described in the following.

B. Computational Effort

The current work is based on the analysis of austriamicrosystems' $0.35\mu m$ CMOS-mixed-signal process licensed from TSMC. This industry standard process offers two different gate oxide options (3.3V and 5V) resulting in 4 basic CMOS devices.

Performing a full factorial simulation of only 3 parameters

(p-well, n-well and PMOS threshold adjust implant) with parameter values 0,1,2 (corresponding missing, correct and double implants) takes $3^3 = 27$ different simulation runs. Because of speed and memory constraints only one CMOS-transistor can be simulated per run, 108 different runs have to be executed to get the full information for these three implants on four transistors. This took a full weekend on a cluster of four 2GHz Linux computers, but having these data calculated up front, enables an engineer to identify very quickly the step where misprocessing occurred, in case a lot fails at electrical parameter test. Furthermore, this information has to be calculated only once, since these data reflect the situation in a frozen process flow.

C. Selecting a Set of Parameters

Since this $0.35\mu m$ process contains 16 implants in total, it is obvious that a full factorial computation is not feasible as the number 4096 of required simulation runs for a full factorial design exceeds all reasonable computation efforts.
However, it is neither necessary nor sensible to do a full factorial design, because, as the probability for a process incident is rather small, the probability that multiple implant steps have been misprocessed is vanishing. However, it is not sufficient to calculate only the 32 situations for each single implant step being skipped or doubly processed, because scenarios where a wrong implant recipe is used lead to situations where one implant is missing and another one doubled. Hence, the possible combinations of missed and double implants have to be selected carefully. So, as can be seen from Table I , out of the possible 27 combinations only 1 (process of record) + 3 times 2 (missing and double implant each) + 2 (swapped P- and N-Well implants) = 9 combinations remain that make sense.
Furthermore, one can distinguish between different implant "classes" which affect only certain electrical parameters. E.g., incidents related to the standard polysilicon resistor implant (poly 2 implant) can be easily detected by measurement of the polysilicon resistance. Hence, only three TCAD calculations need to be performed to cover possible incidents at this particular implant step.
This leads to the general requirement that some efforts are needed to identify an appropriate set of electrical parameters which will give an unambiguous indication of the "culprit" implant.

D. Simulation Results

The parameter values were extracted from combined process- and device simulations with the Synopsys software suite. Each step of the process flow relevant for the device structures was taken into account for the process simulation. A device simulation of the NMOS and PMOS transistor types was performed to obtain device characteristics like saturation current or NMOS threshold. The identical parameter extraction algorithms as in actual electrical tests were applied to enable a comparison to measured values for calibration of the simulation. Finally, the relative deviation of the nominal electrical parameters was calculated the results of which are shown in Table I . These results show clearly the power of the proposed method for identifying root causes for wafer misprocessing. By choosing the driving capability and the threshold voltage of two different types of NMOS and the driving capability of two different types of PMOS transistors an unabigous set of electrical parameters was obtained. The percentage values in the table are relative changes of the parameters compared to the typical situation indicated in the first line of the table. Before the implementation of this method, it took valuable time of PCM data analysis by an experienced device engineer to find switched PLDD and NLDD reticles as the root cause for a misprocessed lot.
As these kinds of implant misprocessing incidents are rare, the system has to be understood as a preventive method to react to such problems as quickly as possible. It can save both, expensive engineering resources and additional measurements. Furthermore, the system can be used to rule out a number of speculations by simply trying them out with simulation and compare the "fingerprint" of their results.

VI. Conclusions and Outlook

Implementing a framework for the integration of TCAD with the actual fabrication process results in multiple impacts on the strategic position of TCAD in a semiconductor fabrication environment.
Historically TCAD was only applied on single device structures and only during process development to gain better insight into the physics behind devices [23]. Additionally, information on physical quantities which are difficult to obtain experimentally was gained. By automated integration of the TCAD framework over the whole work flow of semiconductor circuit fabrication many additional application fields can be addressed, as shown by this work. The setup of new processes (or the transfer of existing technologies) is speeded up dramatically. The human induced errors are consecutely reduced. The number of, at least passive, users of TCAD in a semiconductor company grows from a handful engineers to the entire engineering and production team. This results also in a much better utilization of the resources spent in TCAD (software license costs, work efficiency of TCAD engineers, computer hardware etc.). The gap in technical information between the top management and the "engineer in the production line" is made smaller. This aspect should not be underestimated in the field of semiconductor industry because due to the high complexity of integrated circuit fabrication, any closed documentation of the processes is of inevitable value.
However some open questions remain. The integration of etching and deposition recipies via automatic conversion is still on the level of transferring etch and deposition rates. The lack of generic equipment simulators for etching and deposition leads to additional effort in calibrating these steps in the TCAD simulation. Furthermore, there is still no fully automated approach to generate SPICE models from measurement or simulation data without user interaction. This leads to a significant amount of resource allocation at every additional

Implant			NMOS3V		PMOS3V	NMOS5V		PMOS5V
N-Well	P-Well	V_{TH}	I_{DS}	V_{TH}	I_{DS}	I_{DS}	V_{TH}	I_{DS}
1	**1**	**1**	*0%*	*0%*	*0%*	*0%*	*0%*	*0%*
1	**1**	**0**	*0%*	*0%*	**-52%**	*0%*	*0%*	**-61%**
1	**1**	**2**	*0%*	*0%*	**66%**	*0%*	*0%*	**110%**
1	**0**	**1**	**6%**	**-9%**	*0%*	**12%**	**-20%**	*0%*
1	**2**	**1**	**-2%**	**9%**	*0%*	**-11%**	**24%**	*0%*
0	**1**	**1**	*0%*	*0%*	**15%**	*0%*	*0%*	**39%**
0	**2**	**1**	**-2%**	**9%**	**15%**	**-11%**	**24%**	**39%**
2	**1**	**1**	*0%*	*0%*	**-17%**	*0%*	*0%*	**-17%**
2	**0**	**1**	**6%**	**-9%**	**-17%**	**12%**	**-20%**	**-17%**

TABLE I

CALCULATED DIFFERENCES OF THE SELECTED PARAMETERS TO THE NOMINAL IMPLANT SET (1,1,1) IN PERCENT

model interaction. Finally, package related effects (thermal and electromagnetical) are not included on a routine basis yet.
Since there exists a strong trend to convergence of different technologies (RF, MEMS, sensors, optical etc.), system on a chip (SOC) solutions will play a sigificant role in the future. Therefore not only the small silicon die, but the overall system consisting of die, bond wires, lead frame, and package body has to be taken into account as a whole. The implementation of multy-physics multi-purpose simulators (integrated or as a framework of stand-alone tools) together with the automated recipe aquisition system interfaces to the manufacturing environment will be the challenge for the forthcoming years.

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