FinFET Source/Drain Profile Optimization Considering GIDL for Low Power Applications

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***Abstract*— We have investigated sub-50nm FinFET design to be used in low power applications, through 3D device simulations considering gate-induced drain leakage (GIDL). It is found that the body-tied structure is necessary for doped-channel FinFET to reduce off-state current ($I_{\rm off}$). For further reduction of $I_{\rm off}$ including GIDL, optimization of source/drain (S/D) profile characterized by lateral spread σ and lateral offset δ is effective, and feasibility of S/D profile depends on channel doping concentration. By adjusting the concentration properly, $I_{\rm off}$ can be reduced for (σ, δ) points in a wide range. In addition, sensitivity of drive current upon σ and δ is found to be small.**

I. Introduction

FinFET is a promising device structure to produce multi-gate devices such as double-gate and triple-gate MOSFETs because of their high compatibility with conventional CMOS manufacturing processes. Since FinFETs are expected to exhibit good subthreshold characteristics, they have potential use in low power applications. However, it has been reported that the source/drain (S/D) lateral doping profile has to be carefully designed to achieve sufficiently low off-state current ($I_{\rm off}$) for double-gate MOSFETs [1]. Moreover, it has also been pointed out that gate-induced drain leakage (GIDL) can limit $I_{\rm off}$ in ultra-thin-body silicon-on-insulator (UTB-SOI) MOSFETs [2], which should also apply to FinFETs. We have investigated a method for designing the S/D profile of FinFETs that takes into account the GIDL through 3D device simulation.

II. Evaluation of GIDL Using Device Simulation

Fig. 1 shows GIDL current observed in FinFETs fabricated on a SOI substrate (SOI FinFET). GIDL increases as the gate length ($L_{\rm g}$) decreases due to floating body effect [3], showing the importance of taking GIDL into account, especially in short-channel FinFET design. To estimate the leakage current, including GIDL, for various FinFET structures, 3D device simulations were carried out using DESSIS [4] with conventional drift-diffusion model. Prior to the 3D simulations, the band-to-band tunneling model parameters were adjusted so that the GIDL current measured in a bulk nMOSFET was reproduced (Fig. 2). In this work, lateral decay of the FinFET S/D profiles was represented by the Gaussian distributions. To start with, lateral spread (standard deviation) σ and lateral offset δ were set to 5nm and 4nm, respectively, which corresponds to the implanted arsenic profile tilted 45 degrees and parallel to xz plane (Fig. 3). Polysilicon gate and relatively thick 1.9nm gate oxide (2.7nm inversion thickness) for achieving sufficiently low gate leakage, were assumed.

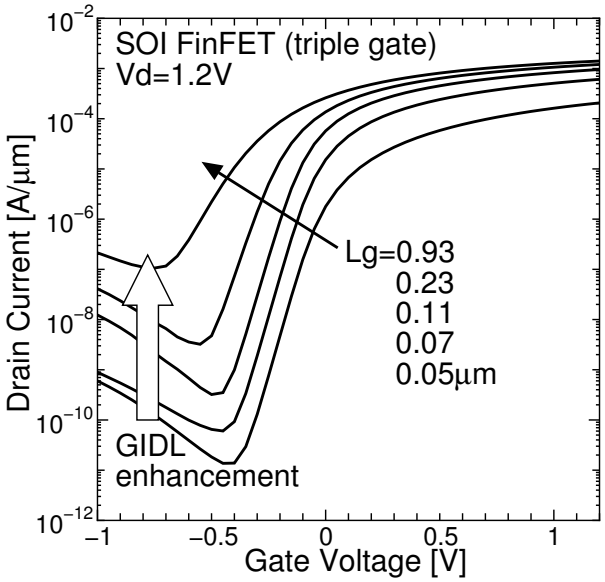

Fig. 1: Measured $I_{\rm d}$-$V_{\rm g}$ characteristics of SOI FinFETs with various $L_{\rm g}$.

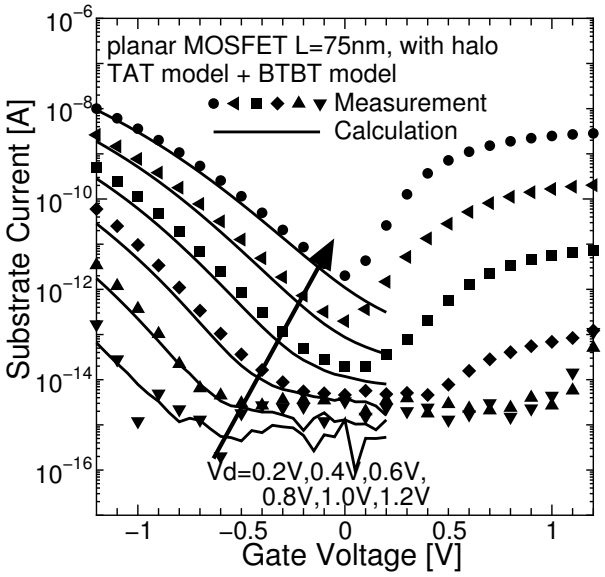

Fig. 2: Measured and simulated substrate current $I_{\rm sub}$ for bulk nMOSFET.

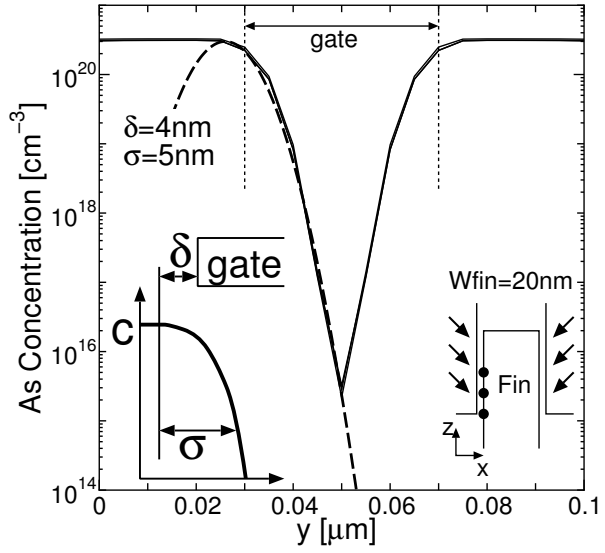

Fig. 3: Arsenic profile along the channel obtained from 3D Monte Carlo simulation.

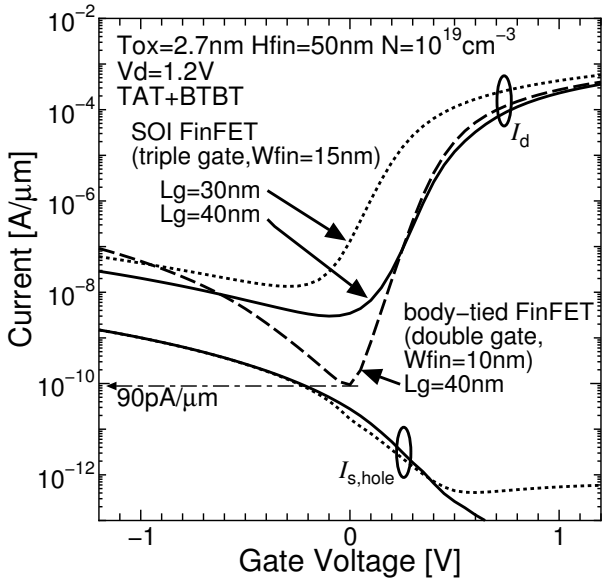

Fig. 4: Drain current ($I_{\rm d}$) and hole component of source current ($I_{\rm s,hole}$) for triple-gate SOI FinFETs (solid and dotted lines) and drain current for double-gate body-tied FinFET (broken line).

In Fig. 4, solid and dotted lines represent the drain current ($I_{\rm d}$) and the hole component of the source current ($I_{\rm s,hole}$) for two different gate lengths simulated for a n-type triple-gate SOI FinFET with a heavily doped channel. $I_{\rm s,hole}$ is the GIDL current due to the carriers generated by band-to-band tunneling, and is not affected by $L_{\rm g}$. However, the GIDL current observed in the drain current was more than 10 times greater than that because of the amplification due to the parasitic bipolar transistor, and worsened for the shorter $L_{\rm g}$. Since the $I_{\rm off}$ is substantially large, improvements of

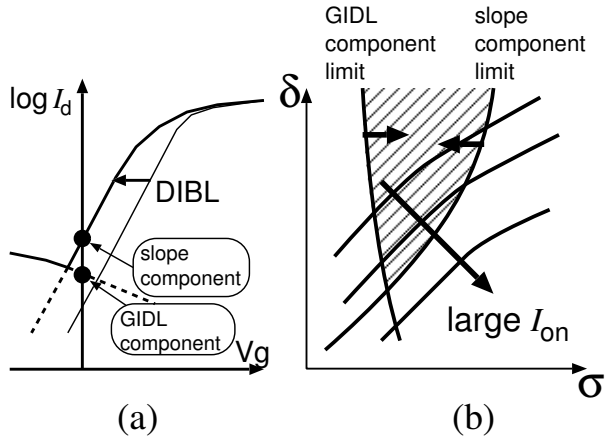

Fig. 5: (a) Two components of $I_{\rm off}$. (b) Feasible region where $I_{\rm off}$ specification is fulfilled, bounded by upper limits of each component.

the FinFET structure other than the S/D profile were made first. Firstly, a body-tied FinFET structure [5] is adopted to avoid the GIDL enhancement. Secondly, triple-gate structure is changed to double-gate, in which the electric field in the upper region of the fin is relaxed and GIDL current is reduced. Thirdly, the fin width $W_{\rm fin}$ is decreased to improve the subthreshold characteristics. As a result, the $I_{\rm off}$ was reduced to approximately 90pA/μm as indicated by the broken line in Fig. 4. However, this $I_{\rm off}$ is still larger than ITRS 2004 specifications where an $I_{\rm off}$ of 25pA/μm is predicted for the hp65 ($L_{\rm g}$=37nm) of the LSTP devices. Therefore, further $I_{\rm off}$ reduction is required, and S/D profile optimization is examined to achieve this.

III. Optimization of Source/Drain Doping Profile

The S/D profile is characterized by the parameters σ and δ, as depicted in the inset of Fig. 3, and determining the appropriate values for σ and δ to reduce $I_{\rm off}$ is of interest. For sub-50nm FinFETs, the $I_{\rm off}$ is determined by two major components, the GIDL component and the slope component (Fig. 5 (a)). Since the slope component is affected by the short channel effects (SCEs), a S/D profile with a small σ and a large δ is preferred for reducing this component. As for the GIDL component, a gradual S/D profile reduces this component and hence a profile with a large σ is preferred. Therefore, the feasible region where the $I_{\rm off}$ is below a certain critical value looks like hatched area depicted in Fig. 5 (b). This is the case when an undoped channel is used and the gate workfunction is fixed as was assumed in [1,2]. However, if the gate workfunction or channel doping concentration N is assumed to be tunable, the optimization results become completely different.

To determine (σ, δ) points that satisfy a certain $I_{\rm off}$ criteria allowing N to vary, a concentration, N^*, which gives the minimum $I_{\rm off}$ for each (σ, δ), was considered (Fig. 6). Figs. 7 and 8 show the $I_{\rm off}$ distributions of double-gate body-tied FinFETs ($L_{\rm g}$=40nm) for constant N and N=N^*, respectively.

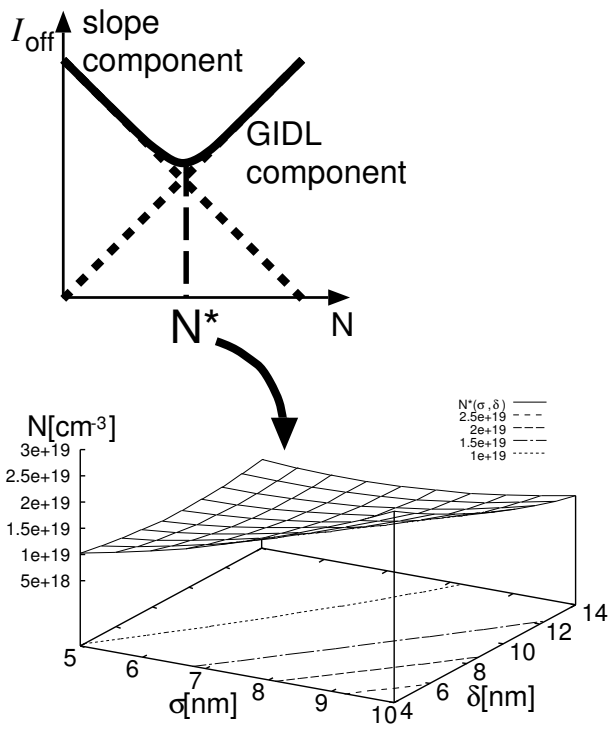

Fig. 6: N^* definition and N^* surface calculated for FinFET with L_g =40nm.

In Fig. 7, contour lines of I_{off} resemble the boundary line of the feasible region depicted in Fig. 5 (b) as expected. I_{off} increases rapidly in lower right direction because of SCEs. In Fig. 8, however, the I_{off} variation in this region was much smaller since SCEs are suppressed by higher channel doping concentration N^* as shown in Fig. 6. The I_{off} plotted in Fig. 8 is the lowest possible one and parameter points in a wider range compared with Fig. 7, could fulfill the specification. The dependence of I_{off} on σ was small within the range shown in Fig. 8 since larger σ leads to smaller GIDL because of more gradual junction, while GIDL is enhanced at the same time because of higher N^*.

The I_{on} is also plotted in Fig. 8. When I_{off} =20pA/μm at N =N^*, the maximum I_{on} was approximately 360μA/μm at the point indicated by a big dot. However, this may not be the optimal I_{on} value. Once the feasible region where the I_{off} is below a certain upper limit is defined, the I_{on} must be recalculated within the region by changing N as there is still room for I_{on} improvement until the I_{off} reaches its upper limit. When an I_{off} of 20pA/μm was attained, it was found that the recalculated I_{on} values are almost constant within the hatched region in Fig. 8 including the point indicated by the big dot. Therefore, the maximum I_{on} estimated for N =N^* shown in Fig. 8 was close to the maximum value in the 3D parameter space spanned by σ, δ and N, although the parameter points within the wide area could offer the maximum I_{on}. The area where I_{on} variation is within 2% from the maximum value is depicted in Fig. 9. In the lower right region of this area,

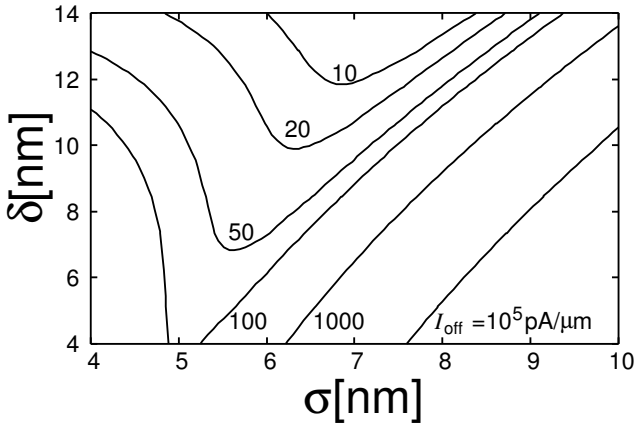

Fig. 7: Contour plot of I_{off} when N is constant (10^{19}cm^{-3}) calculated for double-gate body-tied FinFET with L_g =40nm.

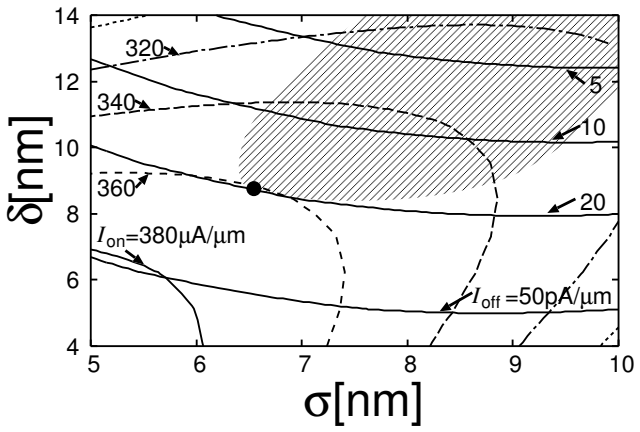

Fig. 8: Contour plot of I_{off} and I_{on} when N =N^*, calculated for same device structure in Fig. 7.

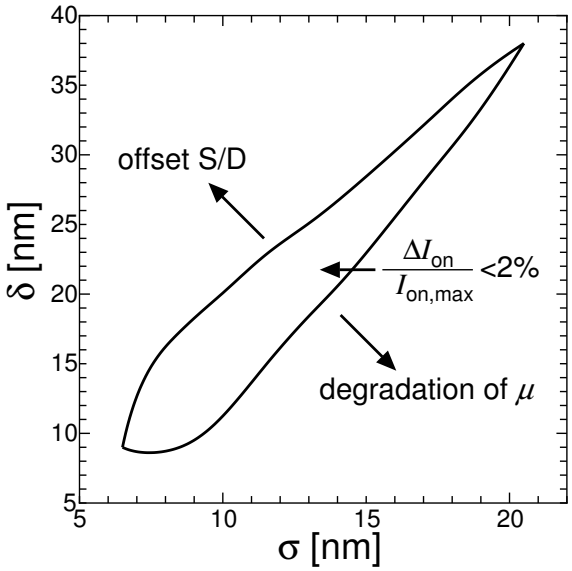

Fig. 9: The area where I_{on} variation is within 2% from the maximum value.

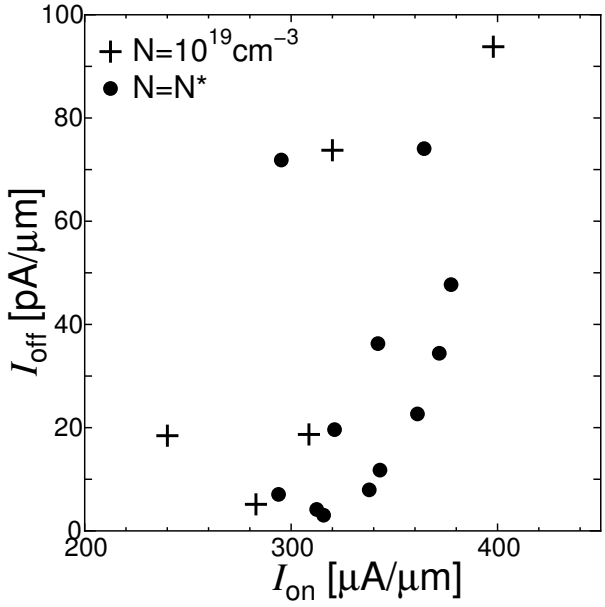

Fig. 10: $I_{\rm on}$-$I_{\rm off}$ plot for various (σ, δ) points.

$I_{\rm on}$ decreases due to degradation of carrier mobility resulting from high channel doping concentration. On the other hand, in the upper left region of the area, S/D region is likely to offset from the gate edge, and hence $I_{\rm on}$ decreases due to increase in series resistance.

Fig. 10 shows the $I_{\rm on}$-$I_{\rm off}$ plot obtained for various (σ, δ) points. A more favorable $I_{\rm off}$ and $I_{\rm on}$ profile can be obtained by adjusting the channel impurity concentration, thereby allowing the design window to be enlarged.

IV. Summary

We evaluated $I_{\rm off}$ by using device simulation that took the effects of GIDL into consideration, and showed that a body-tied structure is needed for sub-50nm FinFETs with a heavily doped channel, that are to be used in low power applications. For further $I_{\rm off}$ reduction, we investigated the S/D profile optimization and found that taking the gate workfunction or the channel doping concentration into account influences FinFET design greatly, which was demonstrated for a doped-channel FinFET with $L_{\rm g}$ =40nm. By adjusting the channel doping concentration, $I_{\rm off}$ can be reduced for (σ, δ) points in a wide range. In addition, sensitivity of $I_{\rm on}$ upon the parameters σ and δ is small. Similar optimizations will be possible for FinFET with an undoped channel by adjusting the gate workfunction.

Acknowledgment

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