Study of RF Performance for Graded-Channel SOI MOSFETs

Wei Ma and Savas Kaya
SEECS, Ohio University, Athens, OH 45701, USA,
e-mail: kaya@ohio.edu, Tel: (740)-597-1633

***Abstract*—The RF performance of Graded-Channel (GC) SOI MOSFET is investigated using accurate 2D TCAD simulations. Intrinsic-gain, cut-off frequency, distortion/linearity and g_m/I_d performance were compared for GC SOI MOSFETs at various channel geometry and doping considerations. We outline how RF characteristics may be optimized in GC SOI MOSFETs. It is shown that GC devices provide a superior RF performance in all figures of merit except for distortion/linearity characteristics. However, they are as susceptible to short channel effects (SCE) as undoped counterparts. In particular, the performance gain obtained by tailoring doping level and position in the graded channel may be ultimately offset by SCE if SOI-layer thickness and gate length are not set appropriately.**

I. INTRODUCTION

Silicon-on-insulator (SOI) substrate technology has emerged as the leading candidate for CMOS applications below 100nm scale [1]. Not only does SOI allow aggressive digital CMOS scaling based on multi-gate architectures, but also it provides a unique platform for RF integration due to its impressive isolation, noise and high-frequency performance inherent to its low-parasitic architecture [2,3]. In particular, the graded or asymmetric-doped channel SOI MOSFET is proposed as suitable candidate for optimizing both RF and DC performance without additional mask levels or complicated fabrication requirements [4,5]. Graded-channel (GC) devices (see Fig.1) have higher doping density at one side of the channel near source and lower doping density at the drain end. This graded channel doping stragety increases the electric field on the source end of the channel, providing a better injection condition for the source while also reducing the electric-field on the drain side, thus leading to larger depletion regions, lower capacitive parasitics and weakened hot-carrier injection. However, so far demonstrations of these devices have been limited mainly to long gate lengths, where integral doping dose is significant and short-channel performance is not obvious. Furthermore, a study of RF performance of GC SOI devices has not been attempted before either. In this work, we investigagte the RF performance of GC SOI MOSFETs by comparing the RF figure of merits including distrotion characteristics, g_m/I_d, cutoff frequency and intrinsic gain. The impact of short-channel effects associated with gate length scaling is also considered in the following RF analysis.

II. DEVICE SIMULATIONS FOR RF ANALYSIS

The generic GC SOI MOSFET structure studied in this work is shown in Fig. 1. The nominal GC device has 200nm gate length, 3nm gate oxide thickness, 50nm SOI layer and 100nm BOX layer. Higher doping region of the channel has L_D=100nm and a uniform density of $N_a=10^{17}cm^{-3}$. The 2D

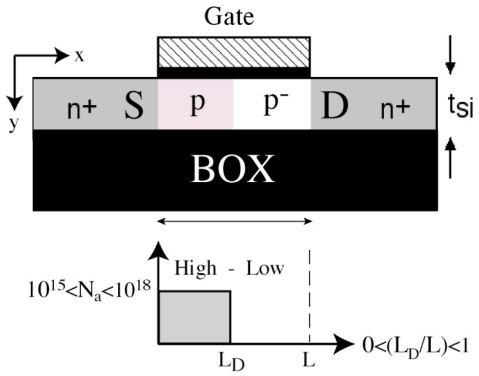


FIGURE 1: Generic GC SOI MOSFET structure used in our simulations. L_D marks the boundary between the high-low doping regions along the channel. Unless otherwise noted, L=200nm, L_D=100nm, t_{BOX}=100nm, t_{Si}=50nm, t_{Oxide}=3nm, $N_a=10^{17}cm^{-3}$

simulations employed in this work were carried out using ISE TCAD 8.0 suite [6], with sufficiently large mesh points to resolve rapidly changing fields also along the channel. Moreover, the quantum mechanical effects are taken into account using density-gradient corrections and hydrodynamic transport model is included to allow accurate simulations. Using both DC and transient (AC) simulations, we investigate the RF performance of GC SOI MOSFETs as a function of device geometry and channel doping strategies. In addition to common g_m/I_d plots, we extract the input-referred linearity figures (third-order intercept power, P_{IP3}) from g_m derivatives using high-order polynomial fits [7], while the third-order harmonic distortion (HD3) is obtained using the new integral approach [8]. Intrinsic gain (g_m/g_d) and cut-off frequency (f_T) are extracted from AC simulations for the same operation condition throughout (I_{DS}=100μA/μm), which allow a fair comparison between MOSFETs of different thresholds. Above figures of merits are sufficient to asses performance in most applications given RF design octagon [9].

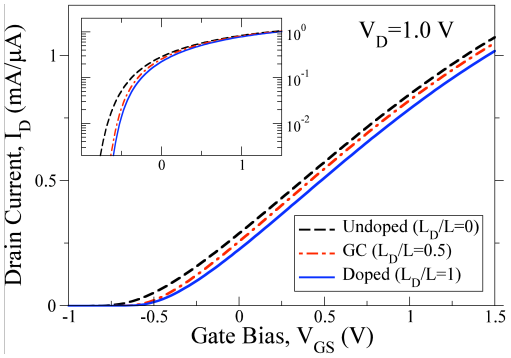


FIGURE 2: I_d-V_g characteristics of Undoped, GC and fully doped otherwise identical MOSFETs. GC curve falls in the middle as expected

III. ANALYSIS AND RESULTS

We start the analysis by comparing I_D-V_{GS} characteristics (Fig.2) of GC SOI MOSFET with undoped and fully-doped device. At all gate biases, I_D-V_{GS} curve of GC SOI MOSFET (L_D/L=0.5) is higher than that of fully doped MOSFET (L_D/L=1) and lower than that of undoped MOSFET (L_D/L=0), which is intuitively expected. The inset of Fig.1 gives a clearer picture of I_D-V_{GS} curves at lower gate bias, i.e. illustrates performance under weak inversion.

Given in Fig.3 are the g_m/I_d curves for all three devices. A high g_m/I_d is crucial to RF devices design. Compared to a comparable undoped device, g_m/I_d performance of GC SOI MOSFET is higher in all operating conditions. In the case of fully doped device, GC-MOSFET has worse g_m/I_d performance in subthreshold-operation but quickly catches up with and eventually slightly exceeds the fully doped device in moderate to strong-inversion conditions under same drain bias (V_D=1.0V). Because moderate to strong-inversion is the area where RF devices are operated mostly, we can see that GC SOI MOSFET can actually outperform even the fully-doped device. Even though a fully-doped SOI device is not preferred due to hot-electron-related noise and kink-effect [10], our data shows how an asymmetric doping strategy may lead to improvement in MOSFET RF performance. In other words, based on g_m/I_d figures, a GC SOI MOSFET is indeed a more suitable alternative for RF modulation performance than undoped and fully doped device under most useful operation points.

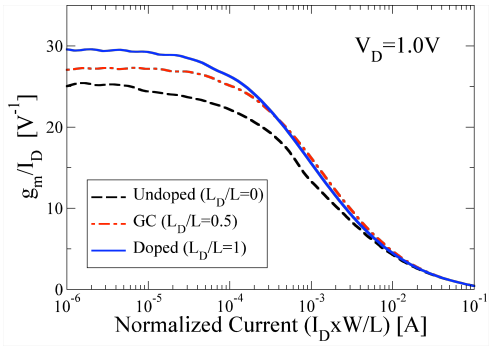


FIGURE 3: Simulated g_m/I_d figures, which relates to f_t and gain, shows that GC device is comparable or better than fully doped device in moderate to strong- inversion conditions.

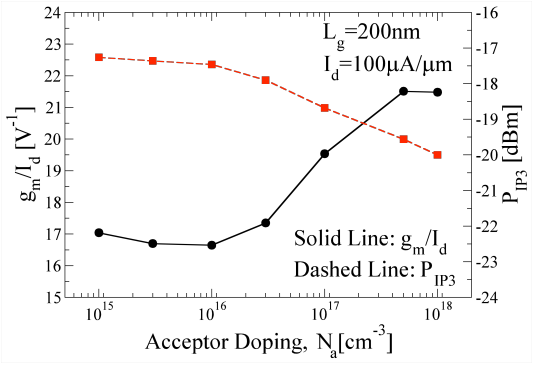


FIGURE 4: GC SOI MOSFET (L_D/L=0.5) suffers from linearity-g_m/I_d trade-offs, which can be controlled by the graded doping.

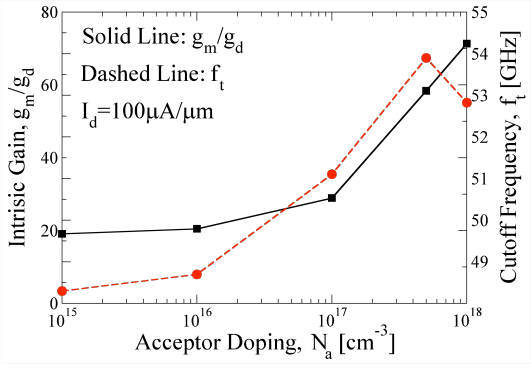
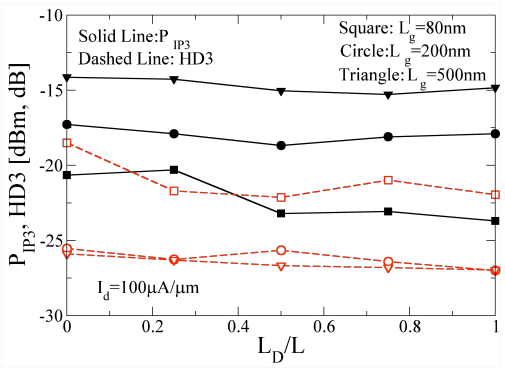


FIGURE 5: Intrinsic gain and cut-off frequency of GC SOI MOSFET can be improved as the level of graded doping increase.

Next we investigate the effect of different channel doping density on GC SOI MOSFET RF performance. As shown in Fig.4, when the channel doping boundary is fixed at L_D/L=0.5, an increase in doping density from $N_a=10^{15}cm^{-3}$ to $N_a=10^{18}cm^{-3}$ leads to an improvement for g_m/I_d of about 5 V^{-1} and a drop for linearity of 3dBm. A similar change in Fig.5 results in a significant increase of 50 in intrinsic gain and an appreciable increase of 6GHz in cut-off frequency. These results indicate that for the RF performance matrix studied here, although increasing the doping density results in a small comprise of device linearity, it leads to higher RF performance in terms of g_m/I_d, intrinsic gain (g_m/g_d) and cut-off frequency (f_T). This is to state that we have a tradeoff between the high gain and better frequency response with linearity. This trade-off is known from bulk MOSFETs [11], which appears to be just as valid in GC SOI MOSFETs.



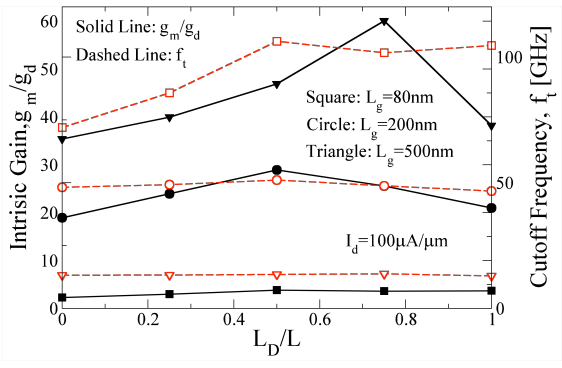


FIGURE 6: a) Distortion characteristic, and b) intrinsic gain and cut-off frequency versus the position of graded channel doping at different gate lengths.

The second aspect of doping strategy studied is the position or high-low doping boundary, as can be seen from Fig.6, where the graded channel doping position varies from $L_D/L=0$ (undoped) to $L_D/L=1$ (fully-doped) case. To include gate length scaling factor, three different gate lengths at 500 nm, 200 nm and 80 nm are selected. As the doping boundary is shifted along the channel, the distortion characteristics (P_{IP3} & HD3) are very slightly reduced as compared to the undoped SOI MOSFET ($L_D/L=0$) case. The channel doping position shift makes small variations for P_{IP3}&HD3 at long gate length (500 and 200 nm) and larger variation at 80 nm. Previous works exist which also illustrate lower P_{IP3} and higher HD3 induced by gate length down scaling [11,12]. For the same scenario in Fig.6, however, the intrinsic gain is maximized at range of $L_D/L=0.5–0.75$ for longer gate lengths and not affected in the shortest device (80 nm). However, f_T is maximized at $L_D/L=0.5$ and saturates when $L_D/L>0.5$ only for the 80 nm GC SOI MOSFET. It is generally clear that the location of doping boundary have more significant impact on frequency and modulation performance than distortion and linearity characteristics. While a universal optimum value is hard to pin down, it is possible to find an optimum location for the doping boundary that maximizes f_T at short gate lengths and intrinsic gain in long gate lengths. In either case, optimum values lie in the range $0.5 \le L_D/L \le 0.75$.

In order to better resolve the impact of device scaling and SCE resistance in GC SOI MOSFETs, we also simulated devices with same doping profiles but with varying channel geometry in terms of gate length and SOI thickness. The impact of Si body scaling on RF performance is shown in Fig.7 for both GC ($L_D/L=0.5$, $N_a=10^{17}cm^{-3}$) and undoped MOSFETs at gate length of 200nm and $I_d=100\mu A/\mu m$. We can see that body thickness scaling does not alter g_m/I_d and linearity significantly for GC-MOSFET, except a slight positive impact on linearity. While body thickness scaling can largely improve the g_m/I_d characteristics of a conventional SOI MOSFET, GC SOI MOSFET is not sensitive to t_{Si}. It seems that the benefits of better gate control from thickness scaling, i.e. less SCE, is already achieved in GC device by virtue of the higher doping in the source end of the channel.

Gate length scaling has the most complicated and the largest impact on the two devices in terms of linearity and g_m/I_d figures as shown in Fig.8. The trend of P_{IP3} (HD3) curve indicates that linearity (distortion) gets worse (larger) as the gate length is scaled down. In the meantime, g_m/I_d increases about $5V^{-1}$ from 1000 nm down to 200 nm but suffers a large reduction at gate length shorter than 200 nm, which suggests that SCE can reduce the RF performance of GC SOI and conventional SOI MOSFETs equally dramatically. This can be better understood if we consider that the generic structure in Fig.1 has a channel thickness of 50 nm, which would be suitable for devices down to 150-200 nm range, and is insufficient to stop SCE for devices any shorter. It is also interesting to note that third-order distortion is also intolerant to SCE, and is not dominated by g_m/I_d at small gate lengths. In the parameter ranges considered here, it is obvious from Fig.9 that GC device has a slight advantage over undoped counterpart in all RF figures of merit except linearity or distortion.

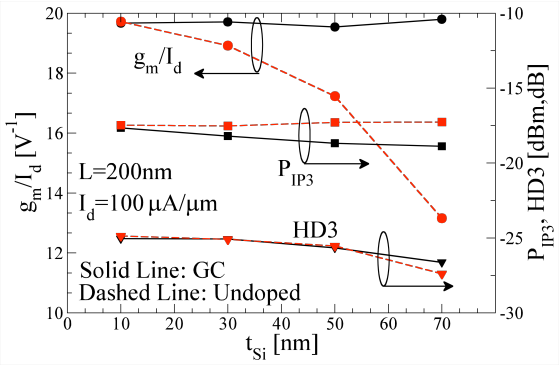


FIGURE 7: Impact of body thickness (t_{si}) on g_m/I_d and linearity (P_{IP3}) of GC ($L_D/L=0.5$) and undoped MOSFETs

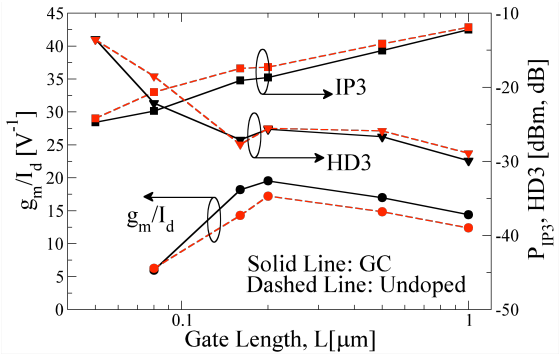


FIGURE 8: Impact of gate length (L) on g_m/I_d and linearity (P_{IP3}) of GC ($L_D/L=0.5$) and undoped MOSFETs

IV. DISCUSSION

The above results show us that it is not possible to opimize the all-around RF performance of SOI MOSFETs solely by the doping or geometry considerations. In the context of GC devices, we specifically show that an asytmmetrical optimization of doping profile in the channel is not sufficient to break the deadlock on gain/linearity or frequency/distortion trade-offs. While optimization of a given RF performance figure via asymetrical doping is possible at a given geometry, SCE can also overwhelm GC devices, distubing the optimization intended. However, as a general rule, we observe that doping level and channel length are more sensitive of all parameters invesitigated, affecting all performsnce metrics equally strongly. On the contrary, the doping boundary position and SOI thickness have weaker impact in RF optimization of GC devices.

We find it interesting that, while the doping location has a minimal impact on linearity/distortion, hence also on g_m/I_d (see Fig.4 and Fig.8), it has a significant impact on intrinsic gain (g_m/g_d) and cut-off frequency (f_T). This points out that it is the output conductance and Miller capacitances that are mainly impacted by the location of doping boundary. The former is reduced as the doping gets closer to drain, while the depletion capacitance get higher as the doping location moves closer to drain. This trade-off is probably responsible for the optimum L_D/L conditions in Fig.6 and may also explain opposite gate length dependence in the same figure. It can also explain the drop in f_T in extreme cases in Fig.5 and 6b, when increase in capacitive elements dominates over high-g_m.

Finally, it is also significant that SCE behavior of GC-MOSFETs in Fig.7 is weakly dependent on SOI thickness, even though conventional SOI MOSFET is strongly dependent. The latter depence gets worse when t_{Si}>40 nm, where SCE becomes significant, which supports the observations on Fig.8 summarized above. Clearly, GC SOI MOSFET is more resilient to SCE than undoped devices as would be expected. Even though this figure does not include information on frequency or gain characteristics of GC-MOSFETs, we can expect in the light of above discussion, as well as of Fig.5 and Fig.6b, that both g_m/g_d and f_T will improve as t_{Si} gets smaller.

V. CONCLUSION

We provide a thorough investigation of RF performance for GC SOI MOSFETs as a function of device geometry as well as doping strategies. To design high RF performance for GC SOI MOSFETs, our work shows that both graded doping density and its position in the channel can be used for RF optimization. Overall, GC SOI MOSFET is less sensitive to changes in body thickness and has better RF performance except linearity as compared to undoped devices. SCE associated with gate length scaling has a dramatic negative impact on both GC and conventional undoped SOI devices.

REFERENCES

[1] G K Celler and S Cristoloveanu, J Appl. Phys., 93(9), p.4955, 2003.

[2] H-S P Wong, IBM J Res & Dev., vol.46, p.133, 2002

[3] T Lee, *Proc. of Symp. on RFIC ,* 3, 1999

[4] B. Cheng *et al*., IEEE SOI Conference, p. 113, 1998.

[5] M A Pavanello *et al*., *Electrochem. and Solid-State Lett.,* 3(1), p.50, 2000.

[6] See for details ISE Inc. web site at http;//www.ise.com

[7] W Ma, S Kaya and A Asenov, *Proc. of EDMO*, p.255, 2003.

[8] A Cerdeira *et al*., *Solid-StateElectronics*, 46 , p.103, 2002

[9] Design of Analog CMOS Integrated circuits, B Razavi, McGraw-Hill, 2001, p.48.

[10] V Kilchytska *et al*., *IEEE Trans. Electron Dev*., 50, p.577, 2003, and references therein.

[11] M Garg, S Suryagandh and J C S Woo, *Proc. of ESSDERC, p.371, 2003.*

[12] T. Soorapanth and T. Lee, in *Proc. 1st Int. Workshop on Design of Mixed-Mode Integrated Circuits and Applications*, Cancun, Mexico, July 1997, pp. 81.