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Forward Body-biased Single Halo MOS Devices for Low Voltage Analog Circuits

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Abstract **- Forward body bias has been shown to be an effective way to improve the digital performance of CMOS circuits. However, as the technologies scale into the sub 100 nm regime, body bias sensitivity degrades, making the application of body bias less attractive for scaled CMOS technologies. In this work, we show for the first time that, Single Halo (SH) MOSFETS exhibit superior body bias sensitivity in the sub 100 nm regime compared to conventional technologies, which can be utilized for improving the performance of forward body-biased MOS devices such as dynamic threshold (DTMOS) and body-driven (BDMOS) transistors for low-voltage (LV) analog designs with the scaled technologies. Our result show that SH doping in these devices results in more than 50 % improvement of intrinsic gain and about a factor of two improvement in transconductance for DTMOS and BDMOS devices respectively, compared to their conventional counterparts.**

I. INTRODUCTION

The continuous scaling of the supply voltage with scaled technologies reduces the circuit headroom and output signal swings available for analog I/O circuits. To increase signal swings, one needs to reduce the saturation drain voltage. This requires the MOS device to be operated at low gate over-drive voltages resulting in reduced transconductance and f_T's. Further at these reduced gate overdrives, the increased short channel effects (SCEs) degrade the performance drastically, in addition to resulting in degraded matching characteristics, making the scaled technologies unsuitable for low voltage analog applications [1] – [2]. Application of forward body in DTMOS devices has been widely studied for logic applications as a way to improve the drive current and SCEs of scaled MOSFETs for low voltage (LV) applications [3] – [4]. In addition to this, forward body bias reduces the threshold voltage and thus increases the input signal swing or common mode range for analog amplifiers [2]. Few researchers looked at BDMOS devices for improving the input dynamic range for low voltage analog amplifiers [5]. However, not much work has been done in understanding the effect of forward body bias on the analog performance characteristics of scaled CMOS technologies. In this work, the effect of forward body bias on the analog performance aspects of scaled CMOS technologies is systematically studied, for the most widely regarded body biased devices, namely the dynamic threshold MOSFETs (DTMOS) and the Body-driven MOSFETs (BDMOS). We show that the performance advantage with these devices can be further optimised with the help of lateral channel engineering [6].

II. SIMULATION DETAILS

The various devices are simulated using 2D DIOS process simulator, available in ISE-TCAD. For both conventional (CON) and SH devices, the process flow is identical except for the threshold adjust implant, which is an angled implantation after gate electrode formation for SH devices [6]. The pocket implant parameters such as dose, energy and angle of implantation are adjusted to maximize the SH device performance and the technology parameters L_G, L_{eff}, t_{ox}, x_j, S/D depth and V_T are adjusted to be identical and are 130 nm, 90 nm, 2 nm, 35 nm, 75 nm and 0.25 V respectively for the two doping schemes. MDRAW tool is used for making simulation grid and DESSIS module is used for device and mixed mode simulations [7]. For SH MOSFETs used in simulations, the pocket has been realized using Boron for n-MOSFETs and Arsenic for p-MOSFETs. The standard threshold adjust implant has been done with BF_2 for CON devices.

III. SINGLE HALO MOSFETS

Fig. 1(a) - (d) show the analog performance parameters g_m/I_D, R_{out} and f_T tradeoff with intrinsic gain and power dissipation for MOS devices with CON and SH doping schemes at a drain voltage of 0.8 V and transistor width of 1 µm. The channel doping profiles for the two devices are shown in the inset. The improvement in analog/RF performance for LAC devices can be directly seen due to reduced DIBL and channel length modulation in SH devices [8]. The higher doping at the source enhances the electron velocity at the source and lower doping in the channel region nearer to drain reduces the coulombic scattering causing improved transcondutances and f_T's in these devices. Besides these advantages, lower channel doping at the drain side decreases the electric field and thus reduces the DIBL. From Fig.1 one can notice that SH doping results in improved values for all the above parameters over a range of bias voltages.

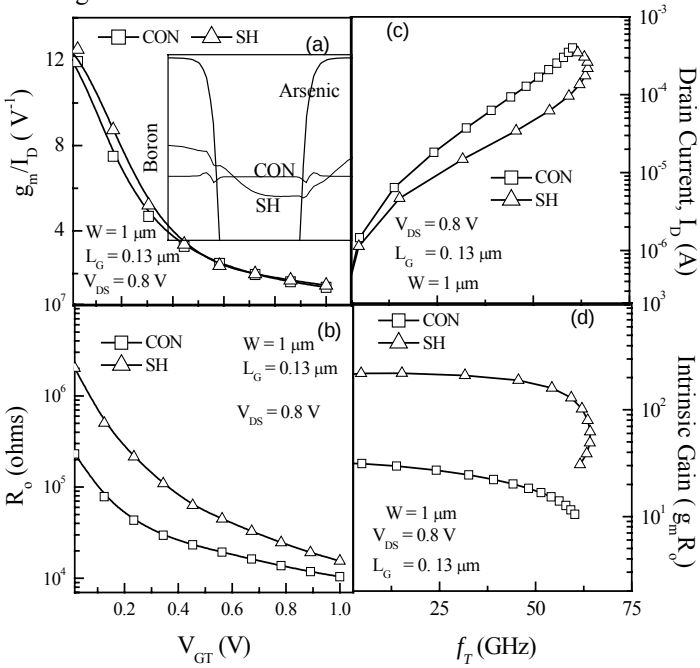

Figure 1. (a) Device g_m/I_D and (b) output resistance (R_o) as a function of gate overdrive (V_{GT}), (c) drain current requirement and (d) Intrinsic gain as a function of device cut-off frequency for both CON and SH devices.

Fig. 2(a) shows device intrinsic gain and body-sensitivity factor (g_{mb}/g_m) as a function of body-to-source voltage at a drain bias of 0.6 V and at a drain current of 0.1 mA. The results show that the SH devices are more sensitive to V_{BS}. This is because of the increased peak doping in the channel region at the source side. Higher doping at the source in the SH devices causes inversion charge profile to be more uniform in the channel resulting in a higher body bias factor, $\alpha = 1+dV_T/dV_{SB}$ for these devices [9]. This further increases the source-to-body (C_{sb}) and drain-to-body (C_{db}) capacitances for these devices as shown in Fig. 2(b). The improvement in the static performance of the device with SH doping with forward body bias can easily be seen and hence one would expect that this doping scheme is more suitable for improving the performance of DTMOS and BDMOS devices. We will look at this aspect in the following sub-sections with detailed process and device simulations.

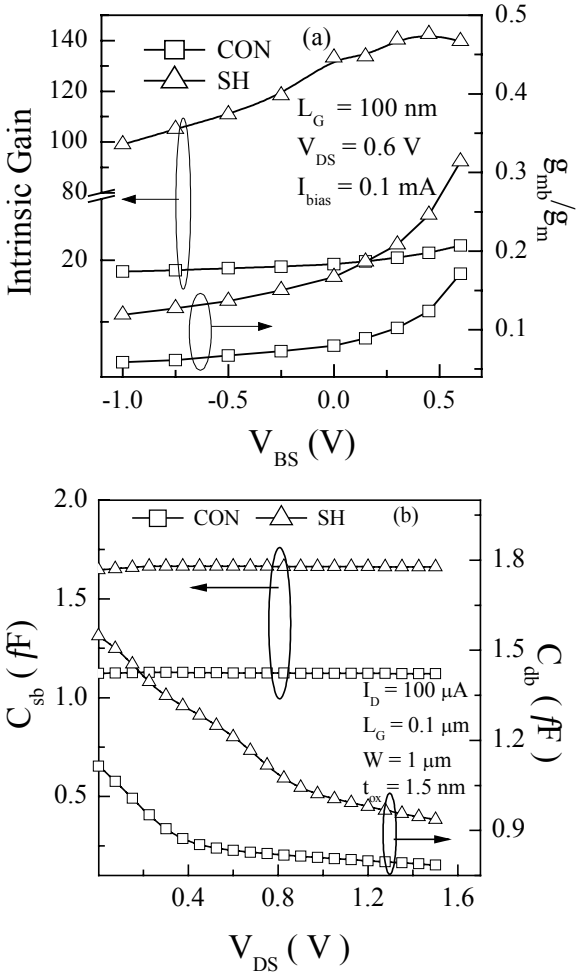

Figure 2(a) Device intrinsic gain and g_{mb}/g_m as a function of body bias, (b) source-to-body (C_{sb}) and drain-to-body capacitance (C_{db}) as a function of drain voltage for both CON and SH devices.

III. DYNAMIC THRESHOLD MOSFET (DTMOS)

In this section the effect of single halo doping on the DTMOS performance is discussed and compared with conventional devices. The SOI technology is used for the device processing. A silicon film thickness of 60nm is used for the simulations to ensure the device operation in partially depleted region, which is shown to be more suitable for DTMOS operation [10]. Fig. 3 shows the device transfer characteristics for all the devices PDSOI-CON, PDSOI-SH, DTMOS-CON and DTMOS-SH devices. The simulated device configuration is shown in the inset. One can see the higher improvement in the drive current for DTMOS with SH doping due to the higher body bias sensitivity at this channel length.

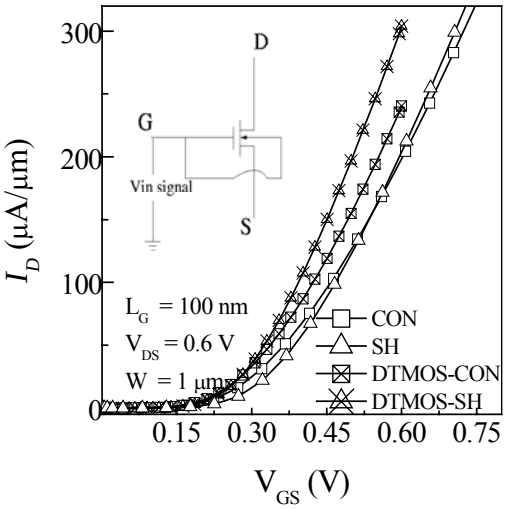

Figure 3. DTMOS device I_D-V_{GS} characteristics for all the technologies, *Inset*: Device configuration

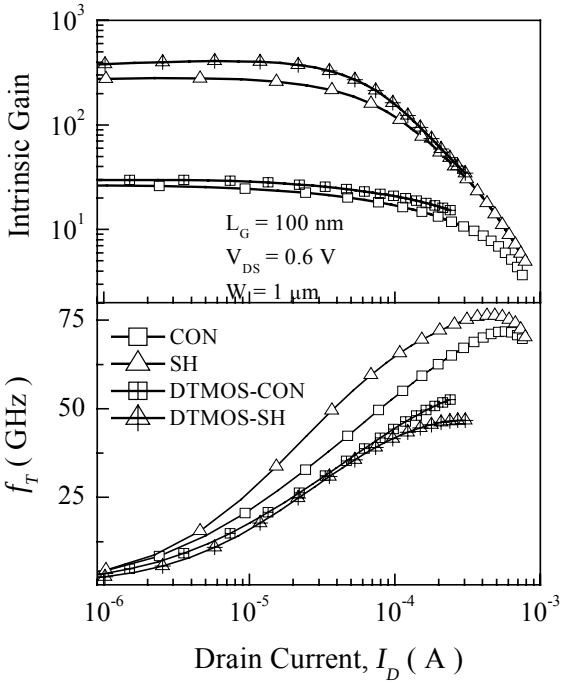

Figure 4. Device intrinsic gain and f_T as a function of bias current for all the devices with CON and SH doping. All the devices are simulated in PDSOI mode.

The analog performance of these devices is shown in Fig. 4. One can see the higher intrinsic voltage gains for DTMOS-SH devices compared to all other devices, but they result in slightly degraded cut-off frequencies due to higher body capacitances as shown in Fig. 2(b). The improvement in intrinsic gain of DTMOS device can be nearly more than 50% over PDSOI device with SH channel doping, however, DTMOS results into only 15 - 20% improvement over PDSOI with CON doping scheme. The improvement in the device intrinsic gain comes from the increased g_m and R_{out} due to a suppression of short channel effects which results in an increased effective gate control of the channel charge. Notice the higher improvement in R_{out} for DTMOS with SH doping again. Also, as the gate length is scaled, improvement

in these parameters with SH doping further becomes higher due to the reduced body effect in conventional devices, as shown in Fig. 5 (a). In Fig. 5(a) the device intrinsic gain and cut-off frequencies are plotted as a function of gate length at a normalized bias current of $I_D/W/L$ of 0.1 mA by keeping the drain bias constant at 0.8 V. The improvement in intrinsic gain is clearly seen for DTMOS-SH devices even at the gate lengths of 65 nm and 100 nm over DTMOS devices with conventional doping scheme. This is due to reduced DIBL as shown in Fig. 5(b). However, at all gate lengths, the cut-off frequency is degraded for DTMOS configurations due to the body capacitances. This degradation further becomes higher for the devices with SH doping scheme. Therefore the DTMOS-SH devices look suitable primarily for aggressively scaled low bandwidth Low-voltage analog circuits.

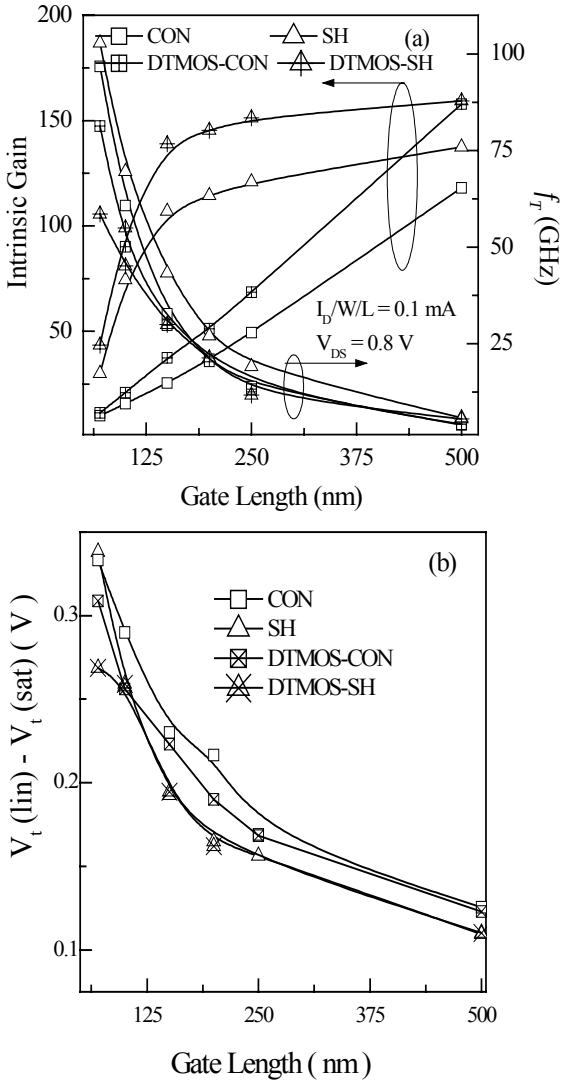

Figure 5(a) Device intrinsic gain and cut-off frequency as a function of gate length at I_D/W/L = 0.1 mA, (b) DIBL as of gate length for all the devices. DIBL is quantified as the change in the V_t for a change of 1V in drain voltage.

IV. BODY DRIVEN MOSFET (BDMOS)

For the MOS transistor to perform any signal processing, it needs to be biased. For a gate driven MOSFET, at the input terminal, a voltage greater than V_t needs to be applied for this purpose. As the feature sizes of modern CMOS transistors are scaling down, the maximum allowable power supply is also scaled. However, unfortunately, the threshold voltage cannot be scaled at the same rate, because of which the dynamic range of CMOS analog/mixed signal circuits deteriorates. The Body-Driven MOS transistor (BDMOS), the configuration shown in Fig. 6(a), is a good solution to threshold voltage scaling limitations for increasing the dynamic range of the LV analog circuits [5]. BDMOS device operates on the principle of modulating the drain current with the body voltage. When operating with positive body voltages, the mode of BDMOS is same as that of DTMOS except that the gate voltage is now fixed and the input is applied to the body. Since the input is applied to the body, this device shows poorer transconductance compared to conventional gate driven devices, and hence the device optimization strategy for BDMOS is not same as that of conventional devices. In this work, we use SH doping to improve the g_m of BDMOS and the effect of halo doping on the analog performance of these devices is systematically investigated.

Fig. 6(b) shows the BDMOS device transfer characteristics with Conventional and SH doping schemes. As expected SH doping results in a higher transconductance, nearly an improvement of 1.5 to 2 times over body-driven CON device, due to its higher body bias sensitivity. Fig. 6(c) shows the device output characteristics for BDMOS devices with Conventional and SH doping schemes with the bias voltages indicated in the figure. As usual SH doping results in better saturation of output characteristics, as discussed earlier in the context of DTMOS devices.

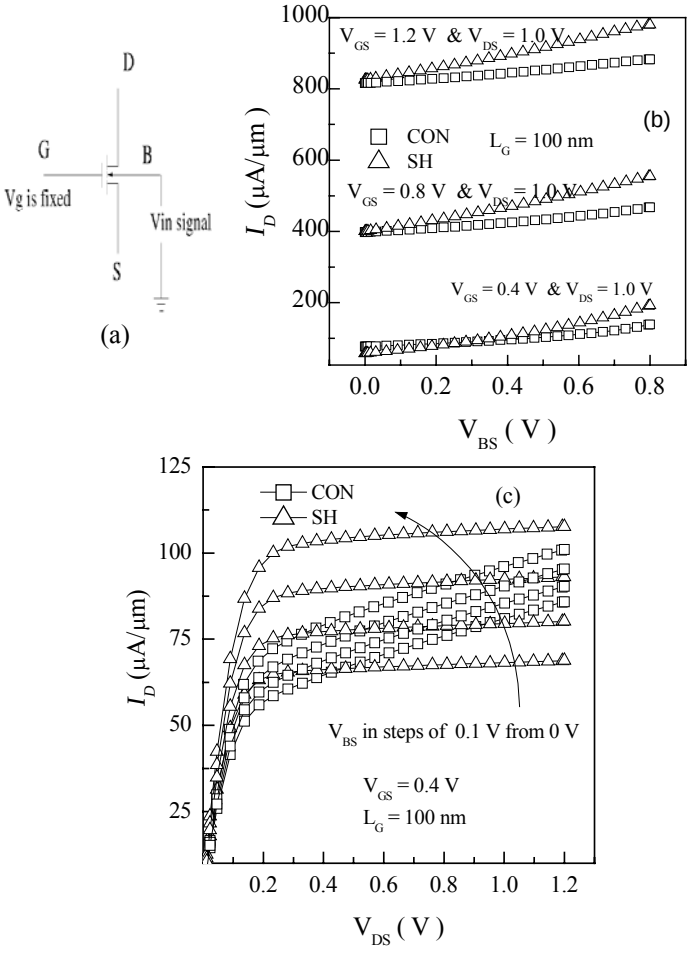

Fig. 6(a) Configuration of BDMOS device used for simulation, (b) its transfer characteristics, and (c) its output characteristics with CON and SH doping schemes.

Fig. 7 shows the device analog performance parameters as a function of drain current at a drain bias of 0.6 V for body-driven and gate-driven MOSFETs. The gate voltage of BDMOS device is kept at 0.4 V. The BDMOS devices show lower drain conductance at all drain currents due to the application of forward body bias. This is because, at the applied bias current, forward body bias reduces depletion depths in the devices causing reduction in the short channel effects. The higher body bias sensitivity in SH devices improves the R_{out} further. One can notice from the above results that SH BDMOS shows almost equivalent intrinsic gains to that of CON gate driven devices, though the transconductances are smaller than their gate-driven counterparts. However, due to the higher body capacitances, the SH devices have shown reduced cut-off frequencies at all biasing conditions. This makes the BDMOS with SH doping mainly suitable for low voltage low bandwidth applications with high signal swings.

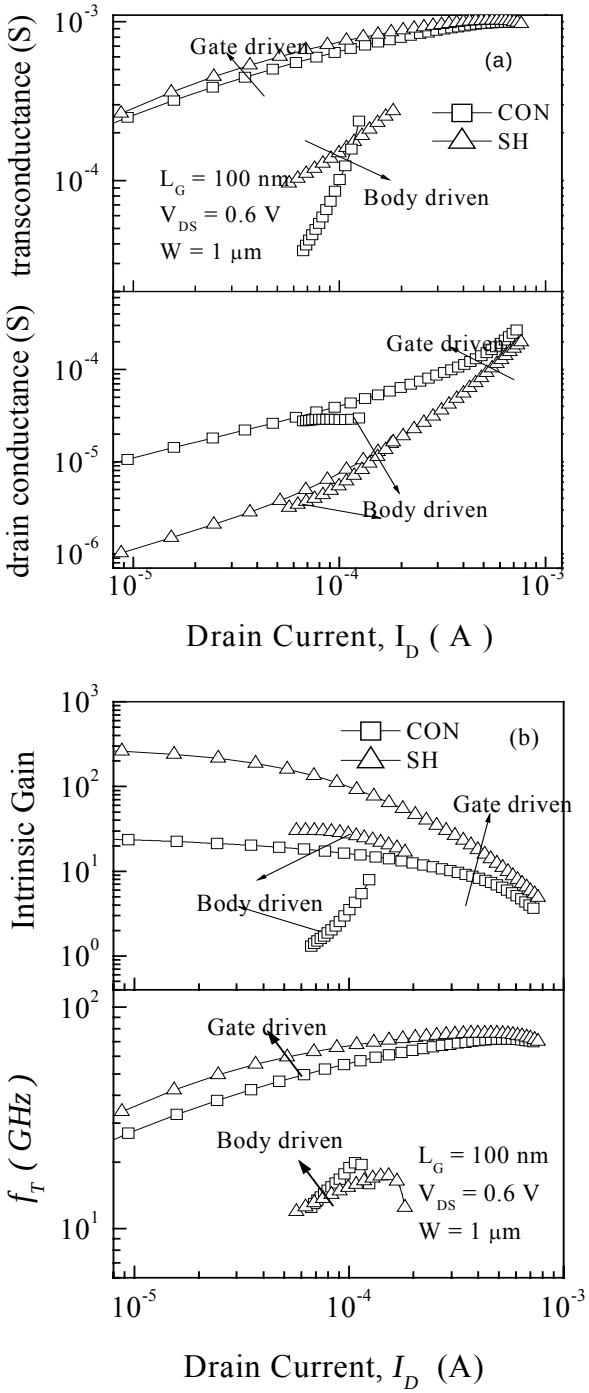

Figure 7(a) Device transconductance and drain output conductance, (b) Intrinsic gain and cut-off frequency (f_T) as a function of bias current for gate and bulk driven device with CON and SH doping. Transistor width is taken as 1 μm and drain bias is kept at 0.6 V.

V. CONCLUSIONS

The increased body-bias sensitivity of sub-100 nm MOSFETs with SH doping and its impact on the analog performance parameters are systematically investigated through 2D device and process simulations. We have shown that the higher body bias sensitivity of SH devices can be used as an advantage for improving the performance of DTMOS and BDMOS devices in scaled technologies. SH doping results in nearly a 50% improvement in voltage gain and about 1.5 to 2 times higher transconductance in DTMOS and BDMOS configurations. However, the increased parasitic capacitances significantly reduce the cut-off frequencies in these body driven transistors. Therefore body driven configurations with SH channel doping seem highly promising for low-voltage, low-bandwidth analog applications.

ACKNOWLEDGEMENTS

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