p_0 are the peak doping concentrations of the n- and p-type regions, respectively. $f_{n/p}(x)$ and $g_{n/p}(z)$ are the distribution functions defined by

$$f_{n/p}(x) = \begin{cases} \exp\left[-\left(\dfrac{x-\mu_x^{n/p}}{\sigma_x^{n/p}}\right)^2\right] & (|x| \le \mu_x^{n/p}) \\ 1 & (|x| > \mu_x^{n/p}) \end{cases}, \quad (3)$$

$$g_{n/p}(z) = \exp\left[-\left(\frac{z-\mu_z^{n/p}}{\sigma_z^{n/p}}\right)^2\right]. \quad (4)$$

Here, $\mu_x^{n/p}$ is the center of the half-Gaussian distribution along the x-direction and $\mu_z^{n/p}$ is the center of the Gaussian distribution along the z-direction. The constant distribution is assumed for $|x - x_c| \ge \mu_x^{n/p}$. $\sigma_x^{n/p}$ and $\sigma_z^{n/p}$ represent the standard deviations of the distribution along the x- and the z-direction, respectively. Changing these doping parameters, we simulated devices with various doping profiles.

3 Results and Discussion

Figure 2 shows the calculated I_d–V_g characteristics of 9 nm gate length MOSFETs at $V_d = 0.4$ V. Thickness of the gate oxide (SiO_2) layer is 0.93 nm and the gate electrode is assumed to be n-type poly-Si. The doping profile parameters are $n_0 = 2.0 \times 10^{20}\,\mathrm{cm}^{-3}$, $p_0 = 8.0 \times 10^{19}\,\mathrm{cm}^{-3}$, $\mu_x^n = 4.5$ nm and $\mu_z^n = \mu_z^p = 0$ nm. The p-type doping center along the x-direction, μ_x^p, is varied from 0.5 nm to 5.5 nm. Other parameters are $\sigma_x^n = 0.67$ nm, $\sigma_x^p = 1.33$ nm and $\sigma_z^n = \sigma_z^p = 9.0$ nm. The doping concentration of the p-type substrate is $10^{17}\,\mathrm{cm}^{-3}$. As shown in Fig. 2, the sub-threshold characteristics becomes better for smaller μ_x^p. The drive current is, however, very small for smaller μ_x^p. This is due to strong confinement at the channel region caused by high p-type doping concentrations for smaller μ_x^p. The left panel of Fig. 3 shows the lowest subband energy profiles along the x-direction at the off-state ($V_g = 0$ V). For smaller μ_x^p, the channel barrier becomes high enough for sufficiently small off-current, although this high channel barrier significantly reduces the on-current.

Figure 4 shows I_d–V_g curves of the same devices as Fig. 2 but with a constant $\mu_x^p = 3.5$ nm and various μ_x^n ranged from 2.5 nm to 6.5 nm. Trade-off relationship between the sub-threshold and the on-current characteristics can be seen in Fig. 4. In the right panel of Fig. 3, where the off-state lowest subband profiles for each μ_x^n are plotted, we see that μ_x^n affects not only the hight of the channel barrier but also the barrier thickness. As a result, μ_x^n influences the device characteristics more significantly than μ_x^p.

To find out what doping profiles are suitable for sub-10 nm bulk-MOSFETs, we have simulated μ_x^n dependence of device characteristics with a fixed off-current $I_{\mathrm{off}} = 5.45\,\mu$A/$\mu$m at $V_g = 0$ V. $I_{\mathrm{off}} = 5.45\,\mu$A/$\mu$m is obtained in the device with $\mu_x^n = 4.5$ nm and $\mu_x^p = 3.5$ nm as shown in Figs. 2 and 4, and the parameter μ_x^p is adjusted to obtain this value for each devices with varied μ_x^n. Other parameters are the same as those used in Figs. 2 and 4. In Fig. 5, μ_x^n dependence of the sub-threshold slope is plotted by closed circles. It can be seen that the sub-threshold slope is 150 mV/dec at $\mu_x^n = 9.5$ nm and it degrades to 260 mV/dec at $\mu_x^n = 3.5$ nm. This degradation of the sub-threshold slope can be attributed to the direct SD-tunneling current. Figure 6 shows μ_x^n dependence of the SD-tunneling current ratio to whole drain current (closed circles) and effective channel length (open circles) at $V_g = 0$ V. Here, we define the SD-tunneling current as the current component having the energy region below the maximum subband energy, E_{top}, and the effective channel length as the width of the channel barrier at the energy

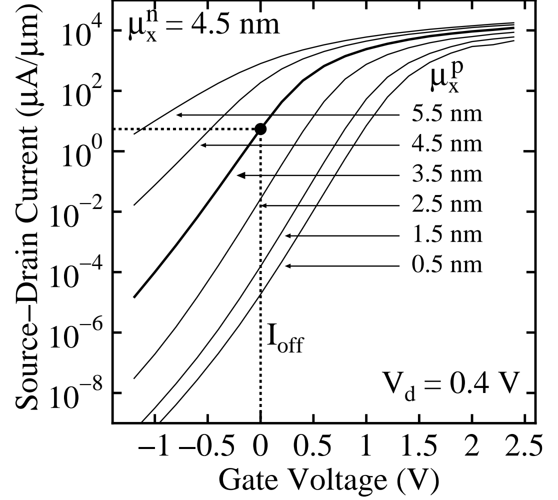

Figure 2: Simulated I_d–V_g curves of 9 nm gate length MOSFETs with $\mu_x^n = 4.5$ nm and $\mu_x^p = 0.5$ – 5.5 nm at $V_d = 0.4$ V. At $V_g = 0$ V, the off-current is $I_{\mathrm{off}} = 5.45\,\mu$A/$\mu$m for $\mu_x^n = 4.5$ nm and $\mu_x^p = 3.5$ nm.

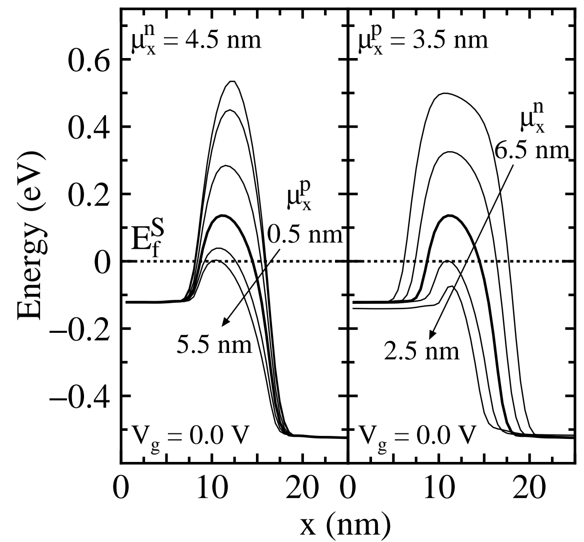

Figure 3: Lowest subband energy profiles at $V_g = 0$ V for the devices with $\mu_x^n = 4.5$ nm and $\mu_x^p = 0.5$ – 5.5 nm (left), and $\mu_x^n = 2.5$ – 6.5 nm and $\mu_x^p = 3.5$ nm (right). Dotted line represents the Fermi energy of the source reservoir.

of $(E_{\rm top} - E_{\rm source})/2$ with $E_{\rm source}$ being the subband energy at the source edge. For smaller μ_x^n, it is found that the SD-tunneling current dominates the off-state device characteristics with very short effective channel length. For example, at $\mu_x^n = 3.5$ nm, the effective channel length is 4 nm, and the tunneling current ratio exceeds 80 %. On the other hand, the tunneling current ratio is only 10 % at $\mu_x^n = 9.5$ nm with 12 nm effective channel length. Thus, in sub-10 nm MOSFETs, off-set doping profiles of $\mu_x^n > L_g/2$ is required in order to reduce the degradation of the sub-threshold characteristics.

Figure 5 shows μ_x^n dependence of the sub-threshold slope for $\sigma_z^n = 11$ nm and $\mu_z^p = 12$ nm (open squares) and for $\sigma_z^n = 7.0$ nm and $\mu_z^p = 8.0$ nm (open triangulars). It can be seen from Fig. 5 that almost the same sub-threshold slope is obtained for larger μ_x^n, although a better sub-threshold slope is obtained in devices with smaller σ_z^n and smaller μ_x^n. At $\mu_x^n = 3.5$ nm, the sub-threshold slopes are 220 mV/dec for $\sigma_z^n = 7.0$ nm, 260 mV/dec for $\sigma_z^n = 9.0$ nm, and 290 mV/dec for $\sigma_z^n = 11$ nm. In the device with smaller σ_z^n, the p-type doping concentration becomes relatively high at around the source/channel and the channel/drain boundaries due to the low n-type doping densities of the source and the drain regions. Thus, for smaller σ_z^n, the devices has less SD-tunneling current because the channel barrier rises and falls down a little closer to the source/drain regions. For instance, the SD-tunneling current ratios are 90 % for $\sigma_z^n = 11$nm, 84 % for $\sigma_z^n = 9.0$nm and 77 % for $\sigma_z^n = 7.0$nm at $\mu_x^n = 3.5$ nm. Note that this slight difference of the channel barrier around the source/channel and the channel/drain boundaries less affects for larger μ_x^n because of the long effective channel.

Figure 7 shows the on-current, $I_{\rm on}$, at $V_g = V_d = 0.4$ V as a function of μ_x^n for $\sigma_z^n = 11$ nm (open squares), $\sigma_z^n = 9.0$ nm (closed circles), and $\sigma_z^n = 7.0$ nm (open triangulars).

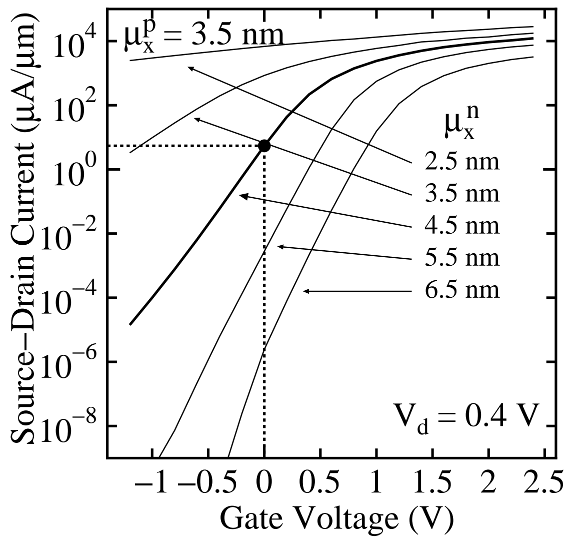

Figure 4: Simulated I_d–V_g curves of the devices with $\mu_x^n = 3.5$ nm and $\mu_x^p = 2.5 – 6.5$ nm at $V_d = 0.4$ V.

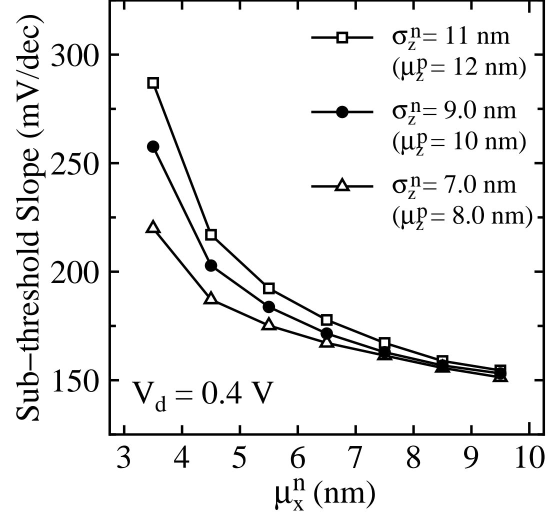

Figure 5: μ_x^n dependences of the sub-threshold slope of devices with $\sigma_z^n = 11$ nm and $\mu_z^p = 12$ nm (open squares), $\sigma_z^n = 9.0$ nm and $\mu_z^p = 10$ nm (closed circles), and $\sigma_z^n = 7.0$ nm and $\mu_z^p = 8.0$ nm (open triangulars). The parameter μ_x^p is adjusted to obtain $I_{\rm off} = 5.45\,\mu$A/μm at $V_g = 0$ V (see Fig. 2).

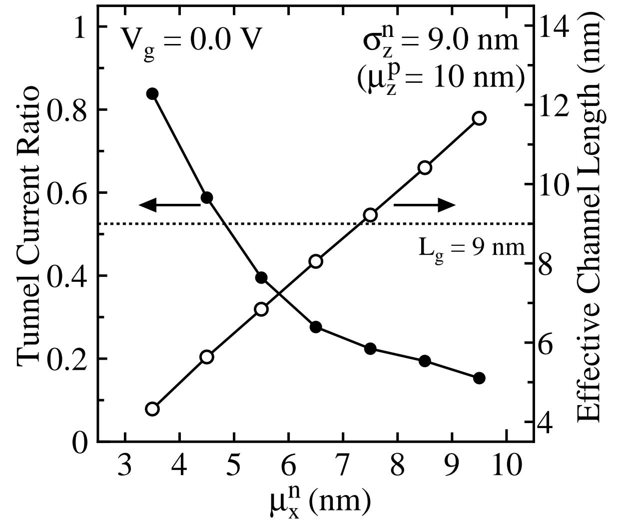

Figure 6: μ_x^n dependence of the SD-tunneling current ratio (closed circles) and the effective channel length (open circles) for $\sigma_z^n = 9.0$ nm and $\mu_z^p = 10$ nm at $V_g = 0$ V. Dotted line indicates the gate length $L_g = 9.0$ nm.

From Fig. 7, we see that $I_{\rm on}$ becomes maximum at $\mu_x^n = 6.5$ nm, and the maximum $I_{\rm on}/I_{\rm off}$ ratios of 50, 54 and 57 are achieved for $\sigma_z^n = 11$, 9.0, and 7.0 nm, respectively. For smaller μ_x^n, a high channel barrier with high p-type concentrations at the channel region is required in order to obtain the fixed off-current $I_{\rm off} = 5.45\,\mu$A/μm because of the large SD-tunneling current. As a result, effects of the subband channel barrier lowering by the gate electric field are less significant than that in the device with larger μ_x^n at the on-state. As seen in Fig. 8, where we plot $E_{\rm top}$ versus μ_x^n

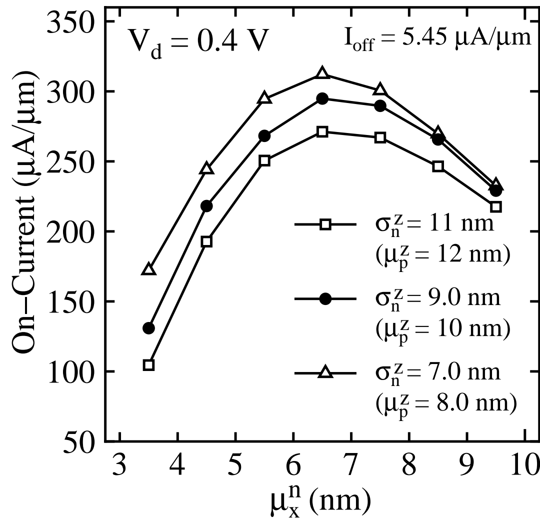

Figure 7: μ_x^n dependence of $I_{\rm on}$ at $V_g = 0.4$ V of the devices with $\sigma_z^n = 11$ nm (squares), $\sigma_z^n = 9.0$ nm (circles), and $\sigma_z^n = 7.0$ nm (triangulars). The parameter μ_x^p is adjusted so as to obtain $I_{\rm off} = 5.45\,\mu$A/μm at $V_g = 0$ V.

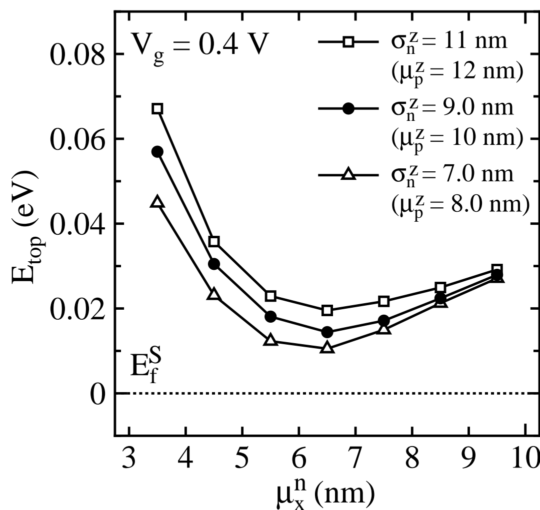

Figure 8: The maximum energies of the channel barrier, $E_{\rm top}$, versus μ_x^n at the on-state ($V_g = 0.4$ V). Doping parameters are the same as those in Fig. 7. Dotted line represents $E_f^S = 0$ eV.

at $V_g = 0.4$ V, the channel barrier remains high for smaller μ_x^n. For the same reason, lager $I_{\rm on}$ is obtained for smaller σ_z^n. On the other hand, for larger μ_x^n, because the effective channel length becomes longer than $L_g = 9.0$ nm as shown in Fig. 6, there are some parts of the channel barrier region which cannot be controlled by the gate electric field. This gate uncontrollable channel barrier suppresses $E_{\rm top}$ lowering at the on-state, resulting in degradation of the on-current characteristics.

4 Conclusion

We have investigated the doping profile effects on the device characteristics of sub-10 nm gate length bulk n-MOSFET by performing the NEGF transport simulation of bulk-MOSFETs with various doping profiles. We find that n-type offset doping for source/drain regions can significantly suppress the SD-tunneling current. The reduction of the SD-tunneling current by the off-set doping profile is effective to achieve large $I_{\rm on}/I_{\rm off}$ ratio. However, excessive off-set n-type doping degrades the on-current characteristics due to the existence of the gate uncontrollable channel barrier. Consequently, the best device characteristics have been obtained for the $\mu_x^n = 6.5$ nm off-set doping profile in the simulated $L_g = 9.0$ nm bulk n-MOSFETs. We also find that the device characteristics can be improved by the shallow doping profile, although the difference of the doping profile along the z-direction have little effects on the device characteristics of ultra-small devices.

Acknowledgment

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