Simulation Analysis of Series Resistance for SOI MOSFET in Nanometer Regime

Xinlin Wang, Phil Oldiges, Andres Bryant[†], Jin Cai[*], Qiqing (Christine) Ouyang[*], Ken Rim

IBM Semiconductor Research and Development Center
Microelectronics Division, Hopewell Junction, NY 12533, [†]Microelectronics Division, Essex Junction, VT, 05452
[*]Research Division, IBM T.J. Watson Research Center
Email: xinlinw@us.ibm.com Phone:(845)894-4740 Fax:(845)892-3039

***Abstract*—In this work, we simulated silicon-on-insulator (SOI) transistors with a design targeting for 45nm NFET. A detailed simulation and analysis of the series resistance (*Rs*) is performed to study the impact of the halo or extension dose, position and grading on *Rs*. It is shown that *Rs* depends on junction grading. Changing halo position appears to improve SCE without degrading *Rs*, while higher halo dose does degrade *Rs* due to halo compensating the extension doping.**

I. INTRODUCTION

CMOS transistor scaling is approaching the fundamental physical limits in the nanometer regime [1]. In order to maintain acceptable short channel performance, the source/drain extension junction depth for sub-50nm CMOS has to be scaled down to around 10nm. On the other hand, a shallow extension junction can give rise to high *Rs* which limits the current drive. The difficulty to scale *Rs* poses a serious limit for continued CMOS scaling [2]. In order to simultaneously optimize short channel effect and minimize series resistance, it is essential to understand how the device structure and the doping profiles in the extension and source/drain regions affect *Rs* [3]. In this work, we simulated silicon-on-insulator (SOI) transistors with a design targeting for 45nm NFET. Extension and halo profile, and spacer thickness are varied to evaluate their impact on R_S and short channel effect. Series resistance is extracted based on channel length dependence of NFET resistance in the linear mode under a fixed gate over-drive. We have performed detailed analysis on the impact of extension and halo dose, position and grading on *Rs*. Based upon these results, we explained why in experiments strained-silicon on silicon-germanium (SGOI) devices show higher series resistance than that of SOI devices [4].

II. SIMULATION METHODOLOGY

Analytical doping profiles are generated for SOI NFET's with channel lengths ranging from 30 ~100nm. Drift-diffusion simulations were performed on the structure shown in Fig. 1 (a) using the FIELDAY device simulator [5]. For the extension and halo doping profiles, in the lateral direction, a complimentary error function is used and in the vertical direction, a Gaussian function is used as shown in *Eq.* (a) and (b). *xchar* and *ychar* are used to control the abruptness of the doping profiles; N_{peak} defines the peak concentration and *xmax, xmin, ymin and ymax* define the location of the extension and halo doping profiles. Fig. 1(b) shows vertical extension profiles we used in the simulation. After we define the doping profiles, linear overdrive current *Iodlin* is calculated at $V_{gs}=Vt+0.7V$, $V_{ds}=50mV$ for different channel length devices. From the *Ron vs. Lgate* curve as shown on Fig (2), *Rs* is extracted and compared among the different cases.

$$dop_{lateral}(x) = N_{peak} \cdot \left[erfc\left(\frac{x - xmax}{xchar}\right) - erfc\left(\frac{x - xmin}{xchar}\right)\right] \Big/ 2 \quad \text{(a)}$$

$$dop_{vertical}(y) = N_{peak} \cdot \begin{cases} \exp\left[-\left(\dfrac{y - y\min}{ychar}\right)^2\right] & y < y\min \\ 1 & y\min \le y \le y\max \\ \exp\left[-\left(\dfrac{y - y\max}{ychar}\right)^2\right] & y\max < y \end{cases} \quad \text{(b)}$$

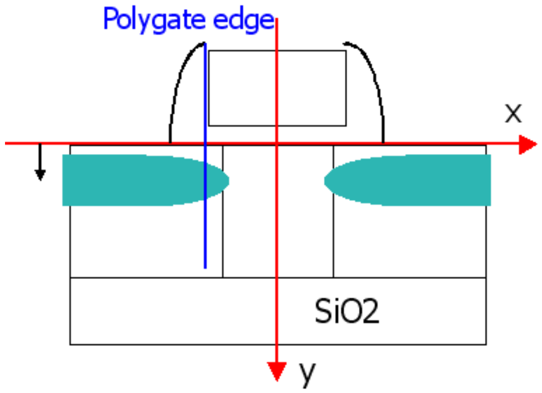

Fig.1 (a) simulated SOI structure.

III. SIMULATION RESULTS

(1) *Rs* dependence on extension profile

The resistance arising from the lateral drop in doping concentration from the peak of the junction to the channel concentration, extension-to-inversion-layer link up resistance, is a significant contributor to *Rs* [5]. By artificially modifying the lateral gradient in the simulations, Fig. 3 (a) shows when lateral extension abruptness is varied from “ultra” sharp *1nm/dec* to *8nm/dec*, *Rs* increase more than 20%, which means that the link-up resistance depended strongly on junction grading. Fig. 3 (b) shows that sharp vertical extension profile can also help reduce *Rs*. Fig. 4 (a) shows that sharper lateral extension profile gives better *Vt* roll-off due to relative longer *Leff* and Fig. 4 (b) shows sharper vertical extension profile does not help to improve short channel effect (SCE).

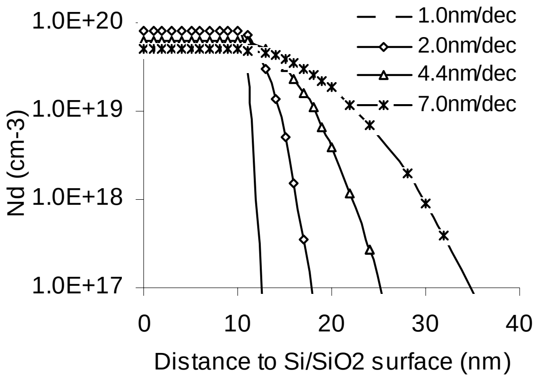

Fig.1 (b) 1D Vertical extension doping profiles used in the simulation. Gaussian function is used. Total extension dose is fixed; only gradient of the profile is varied.

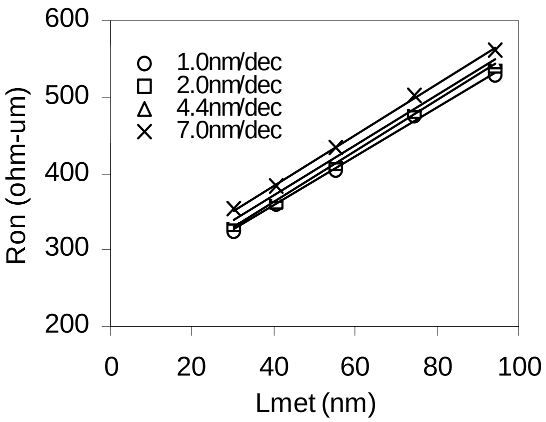

Fig. 2 (a) Ron *vs.* Lmet when vary lateral extension abruptness.

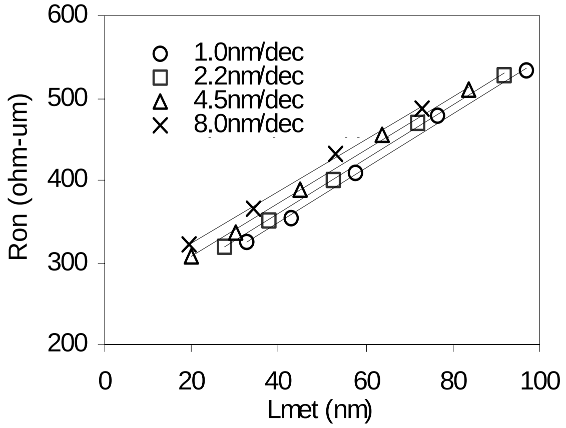

Fig. 2 (b) Ron *vs.* Lmet when vary vertical extension abruptness.

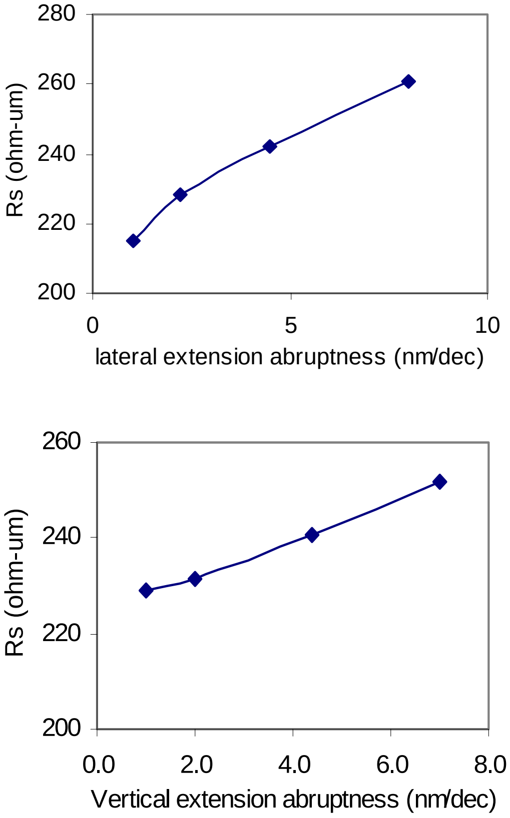

Fig. 3 *Rs* (extracted from Ron vs. Lmet curve) for different extension profiles. Sharper extension profiles in both lateral and vertical direction give smaller *Rs*.

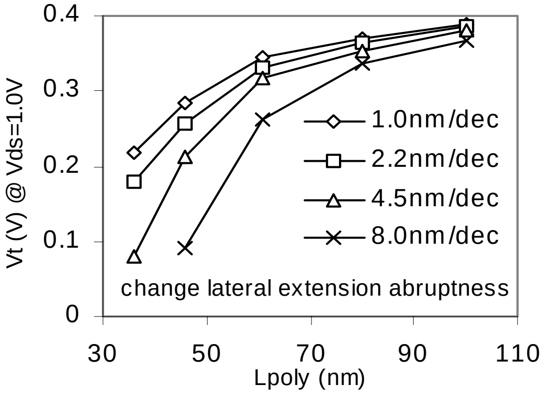

Fig4 (a) vary lateral extension abruptness

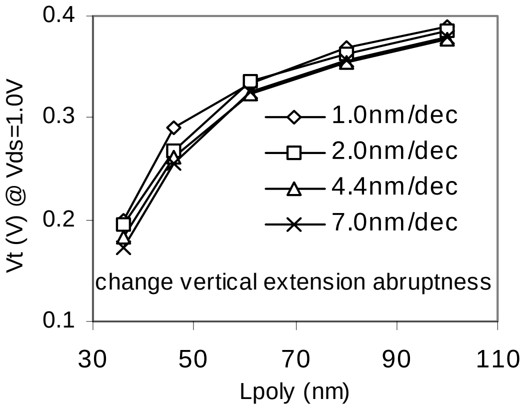

Fig.4 (b) vary vertical extension abruptness

Fig. 4 Vt roll-off for different extension profiles.

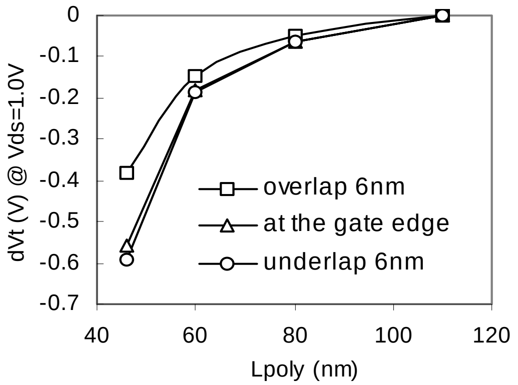

Fig. 5 Vt roll-off when the position of halo peak concentration is moved in the lateral direction.

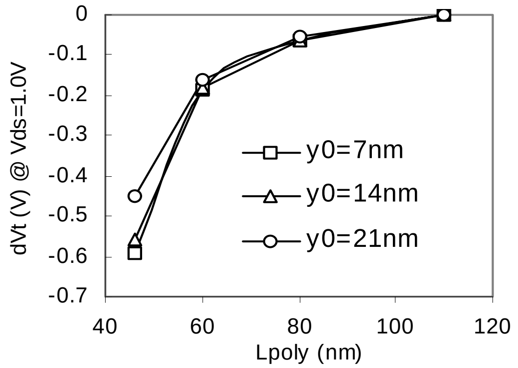

Fig. 6 Vt roll-off when the position of halo peak concentration is moved in the vertical direction.

x0 (nm)	Rs (ohm-um)
overlap 6nm	219
at the gate edge	210
underlap 6nm	207

Table 1 (a) vary x0

y0 (nm)	Rs (ohm-um)
7	215
14	210
21	205

Table 1 (b) vary y0

lateral profile abruptness	Rs (ohm-um)
2.1 nm/dec	210
5.1 nm/dec	210
10.5 nm/dec	212
14.5 nm/dec	211

Table 1 (c) vary lateral abruptness

Table 1 *Rs* when the position and the lateral abruptness of the halo profiles are varied.

(2) *Rs* dependence on halo profile

Here we provide detailed analysis on the impact of halo dose/position/grading on *Rs*. In the vertical direction, *ymax=ymin=y0* in *Eq*. (b), which defines the vertical position of the peak concentration of halo profile. Usually increasing overlap region between halo profile and gate improves SCE control as shown on Fig 5. On the other hand, Table 1(a) shows this also slightly increases *Rs* by ~ 4% due to compensating the extension doping. Table 1(b) shows that when the halo profile is close to the Si/SiO2 surface, *Rs* slightly increases (up to ~ 3% between y_0=7nm and y_0=21nm).

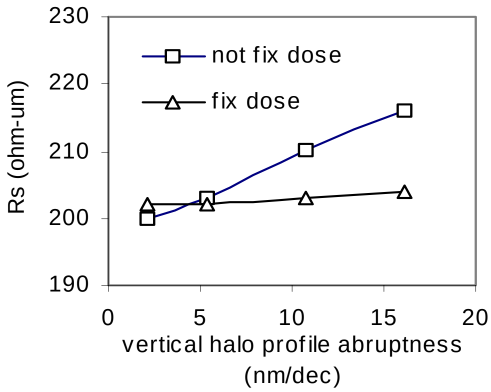

Fig. 7. *Rs* vs. vertical halo profile abruptness. When halo dose is fixed, *Rs* is not sensitive to the vertical halo grading.

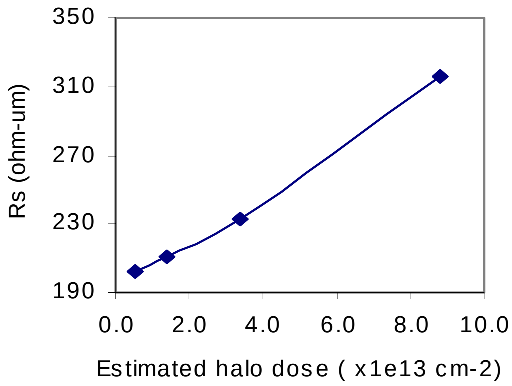

Fig.8 *Rs*. *vs*. halo dose. *Rs* is sensitive to halo dose. When halo dose is increased to improve SCE, *Rs* increases.

Figs. 5 and 6 show that changing halo position appears to improve SCE control without degrading *Rs*, which sets the direction for halo optimization for nanometer device scaling. *Rs* is not sensitive to the lateral and vertical halo profile abruptness, while high dose does degrades *Rs* as shown in Figs 7 and 8. Increasing halo dose compensates the extension dose, which increase *Rs*. In Fig. 9, we simulated three kinds of devices: (1) reference device (2) with 30% higher extension doping (3) with 30% higher extension and 30% higher halo doping. Fig. 9 shows that increasing extension dose reduces *Rs* and if both extension and halo doping increase by the same factor, *Rs* is not affected, which supports our previous conclusion that halo compensating the extension is the main reason for a higher *Rs* when halo dose is changed.

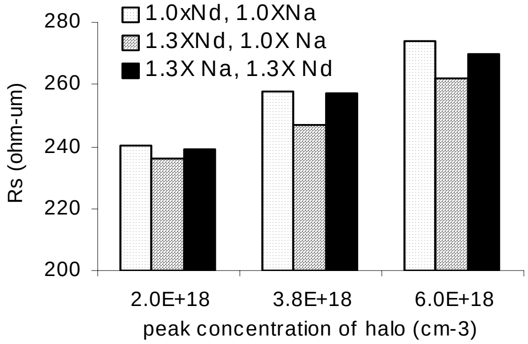

Fig. 9 *Rs*. *vs*. the peak concentration of halo profile.

(3) *Rs* dependence on Spacer

Extension resistance is part of total series resistance and Fig. 10 shows reducing spacer thickness can reduce extension resistance.

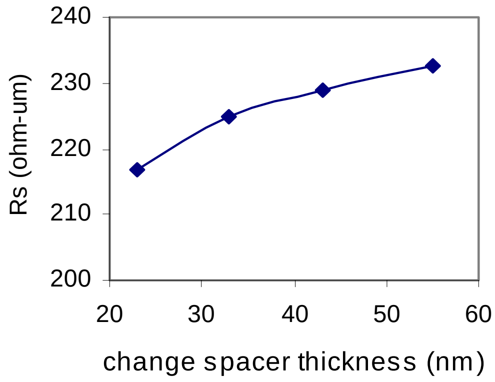

Fig.10 *Rs*. vs. the spacer thickness. Larger spacer gives slightly larger *Rs*.

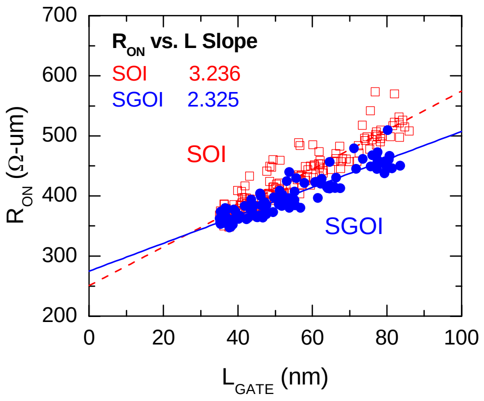

Fig. 11 NFET R_{ON} vs. gate lengths of SOI and SGOI NFETs. SGOI devices show larger *Rs* than that of SOI devices.

(4) Experiment Analysis

Experimental data show that strained Si SGOI NFET has larger *Rs* than that of SOI device as shown on Fig. 11, which dilutes strain-induced performance enhancement of SGOI over SOI devices. Our simulations explained why SGOI NFETs show larger *Rs*. There are two main reasons: (1) Due to arsenic diffusion enhancement in SiGe layers [6], the extension profile of SGOI is more graded compared to SOI; (2) more halo doping is used in SGOI to compensate for Vt-lowering effect. Higher halo dose increases *Rs* as we learned from previous simulations.

IV. CONCLUSIONS

Detailed analyses were performed on the impact of extension and halo dose, position and grading on *Rs*. The extension-to-inversion-layer link up resistance depends strongly on junction grading. Sharper extension profiles are preferred to minimizing *Rs* and improving SCE control. Changing halo position appears to improve SCE without degrading *Rs*, while higher halo dose does degrade *Rs* due to halo compensating the extension doping.

References:

[1] H.-S. P. Wong, et al., Proc. IEEE, vol. 87, pp. 537-570, 1999.
[2] S. Thompson, et al., Proc. Symp. VLSI Technol., pp. 132-133, 1998.
[3] K. K. Ng, et al., IEEE Trans. Electron Devises., vol. ED-33, pp. 965- 972, 1986.
[4] J. Cai, et al., IEDM Tech. Dig., pp. 165-168, 2004
[5] E. Buturla, et al., NASECODE VI, p. 291, 1989.
[6] P. Keys, et al., Superlatt. Microstruct., vol. 27, pp. 125-136, 2000.
[7] A. Pakfar, et al., SISPAD 2004, pp. 45-48, 2004.