Computer Simulation of Germanium Nanowire Field Effect Transistors

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***Abstract*— In this paper, electrical characteristics of germanium (Ge) nanowire field effect transistors (FETs) are computationally investigated. A calibrated three-dimensional (3D) density-gradient simulation is performed to explore the electrical characteristics of Ge omega-shaped-gate FETs. The examined nanodevices are with a 70% gate coverage ratio. By evaluating the threshold voltage roll-off, the transfer characteristics, and the leakage current, our numerical results have shown that the Ge nanowire FET has potentially higher driving-capability than that of the silicon (Si) one. Due to good channel controllability of the omega-shaped-gate FET with the 70% gate coverage ratio, compared with the Si nanowire FET, the high mobility Ge nanowire FET significantly suppresses the effect of band-gap narrowing on the transport characteristics. Leakage current of the Ge nanowire FET depends upon the thickness of the gate channel film. A thinner Ge film leads to a lower leakage current. Preliminary numerical study on the Ge Nanowire FET with a propoer selection on gate material provides interesting results for the design and fabrication of high performance nanodevices in nanoelectronics era.**

I. Introduction

Novel structures and materials for developing advanced nanoscale field effect transistors (FETs) have recently been of great interest [1], [2], [3], [4], [5], [6], [7], [8]; in particular, for the design and fabrication of ultra large scale integrated (ULSI) circuits using nanodevices. It is known that conventional germanium (Ge) bulk FETs, compared with silicon (Si) devices, have encountered the effect of band-gap narrowing on carriers' transport properties and may result in, such as significant leakage current [9]. To obtain good channel controllability and electrical performance, different cylindrical- and noncylindrical-shaped-gate Si FETs have been reported in recent years [1], [2], [3], [4], [5], [6], [7], [8]. Ge FETs possess higher mobility than that of silicon (Si) ones. Study on Ge nanowire FETs may provide promising electrical characteristics, compared with Si nanowire FETs.

In this paper, we numerically explore the electrical characteristics of nanoscale Si and Ge omega-shaped-gate FETs. According to our recent work on Si nanowire FETs [1], [7], [8], the explored Ge omega-shaped gate FET in this work is directly with a 70% coverage ratio. To compare the electrical characteristic difference on the Si and Ge nanowire FETs, a calibrated three-dimensional (3D) nanodevice simulation prototype with the density-gradient model is performed for the calculation of the threshold voltage roll-off, the leakage current, and the on state current, respectively. By evaluating the aforementioned physical quantities for the Si and Ge nanowire FETs with different gate length and thickness of channel film, it is found that the Ge nanowire FET has higher driving-capability than that of the Si one. Compared with the simulated results of the Si nanowire FET, due to good channel controllability of the omega-shaped-gate FET with the 70% gate coverage ratio, the high mobility Ge nanowire FET significantly suppress the effect of band-gap narrowing on the transport characteristics. The leakage current of Ge nanowire FET can be reduced by selecting a proper thickness of the channel film.

This paper is organized as follows. In Sec. II, we state the computational model and simulation methodology. In Sec. III, we discuss the numerical results of the terminal current, the threshold voltage roll-off, and the leakage current for the Si and Ge nanowire FETs with respect to different gate channel length and thickness of the channel films. Finally, we draw conclusions.

II. Simulation Methodology

Multidimensional density-gradient formulation is adopted in this work. It attracts more attention and successfully demonstrates its validity for efficient modeling the quantum mechanical effects in TCAD simulator using the first order quantum corrections. It is computationally effective for incorporating the quantum mechanical effect in a multidimensional nanodevice TCAD simulation. The 3D simulation quantitatively predicts the main tendency of electrical and physical properties for the examined device structures. We note that a full quantum mechanical methodology will input

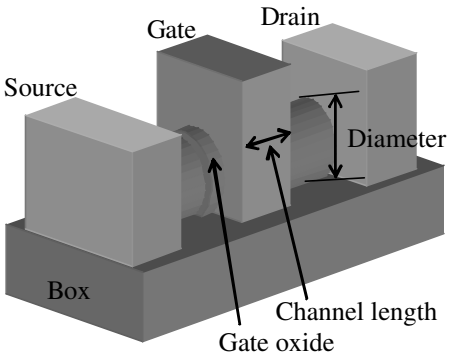

Fig. 1. A three-dimensional schematic plot of the studied device structure. The omega-shaped-gate FET is with the Si and Ge materials, where the band-gap is 0.66 eV for Ge and is 1.12 eV for Si. Mid-gap materials are selected for the gate of devices. The channel of nanodevice is with the 10^{18} cm^{-3} boron. The source and drain of the nanodevice are with the 5x10^{19} cm^{-3} arsenic and the thickness of oxide T_{ox} is equal to 1 nm. The channel length (L) ranges from 10 nm to 30 nm, and the thickness of the channel film ($T_{Si/Ge}$) is with 10 nm and 20 nm, respectively.

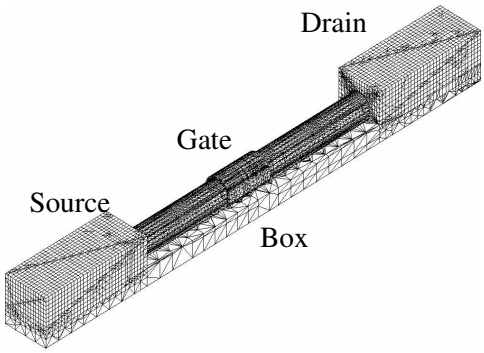

Fig. 2. The mesh structure of the simulated Ge omega-shaped-gate FET with the 70% coverage ratio of the gate, where $L = 20nm$ and $T_{Ge} = 10nm$. The device is biased at V_D=0.05 V and V_G=0.8 V.

more accurate estimation on the characteristics, but our simulation will not be altered. To calculate the numerical solution of the 3D density-gradient model for the studied device structures, a robust device simulation program is applied. Developing this computational prototype is mainly based on our recent work on semiconductor device simulation [9]. Firstly, we decouple the coupled partial differential equations (PDEs), each decoupled PDE is approximated with the finite volume method over nonuniform mesh. The corresponding system of the nonlinear algebraic equations is then solved with the mixed monotone iteration and Newton's iteration methods. Iterations will be terminated and postprocessing will be performed when the specified stopping criteria for both the inner and outer iteration loops are satisfied, respectively.

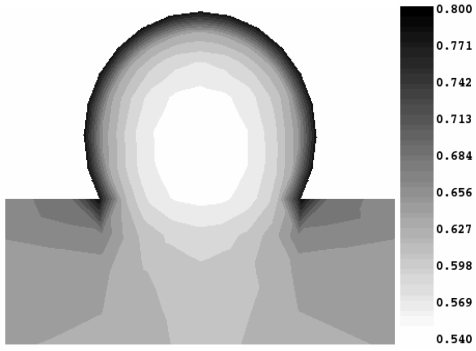

Fig. 3. A contour plot of the potential profile for the simulated Ge omega-shaped-gate FET with the 70% gate coverage ratio, where $L = 20nm$ and $T_{Ge} = 10nm$. The nanodevice is biased at V_D=0.05 V and V_G=0.8 V. The plot is cutting from the gate channel region. The bottom is the insulating box and the channel is with an omega shape.

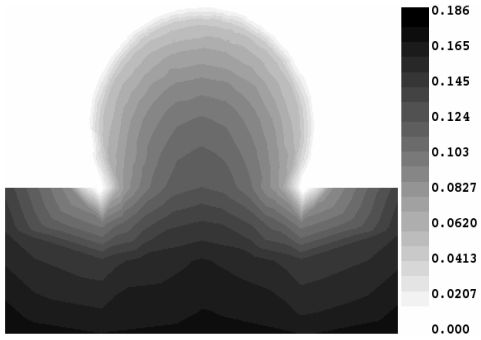

Fig. 4. A contour plot of the potential profile for the simulated Ge omega-shaped-gate FET with the 70% gate coverage ratio, where $L = 20nm$ and $T_{Ge} = 10nm$. The nanodevice is biased at V_D=0.8 V and V_G=0.0 V.

The electrical characteristics of the Si and Ge omega-shaped-gate FETs with different gate coverage ratio are calculated. As shown in the figure 1, first of all, the gate length of nanodevice is fixed at 20 nm, and the diameter, the thickness of channel film of Si or Ge, is equal to 10 nm. To determine an optimal coverage ratio of the Si and Ge omega-shaped-gate FETs for the following investigations, calculations of the Si omega-shaped-gate FETs with different gate coverage ratio ranging from 70% to 100% (i.e., the case of surrounding-gate) have been explored in our recent work [7]. Taking the surrounding-gate FET as the ideal sample, the intrinsic and terminal characteristics of the Si omega-shaped-gate FET with the 70% gate coverage ratio are similar with the results of the surrounding-gate FET. In this work, we do not explore the effect of gate coverage ratio on the Ge omega-shaped-gate FET. The selection of 70% gate coverage ratio directly follows the results of Si one. However, further clarification of effects of gate coverage ratio as well as the gate material will benefit the progress of Ge nanowire FETs.

III. Results and Discussion

The mesh structure of the simulated on-state Ge omega-shaped-gate FET is shown in Fig. 2. According to our adaptively computing algorithm, very fine mesh is automatically focused on the gate channel region based on the simulation and error estimation on computed solutions. We compare the simulated potential distributions of the Ge omega-shaped-gate FETs under the on- and off-state conditions, shown in Figs. 3 and 4, respectively. The contour plot of the potential is cutting from the gate channel region. Good channel controllability for the nanodevice operated at the on-state is observed shown in Fig. 3. A similar potential distribution is observed for the nanodevice at V_D=0.8 V and V_G=0.0 V shown in Fig. 4. For Si omega-shaped-gate FET, similar results were reported in [7].

As shown in Fig. 5, with the same device configuration, we find that the subthreshold behavior of the Ge omega-shaped-gate FET with the 70% gate coverage ratio is similar to the result of the Si one, though it has a lower threshold voltage. However, adjustments of the threshold voltage can be done by carefully selecting gate materials for Si and Ge FETs. Leakage current plays an important issue in design and fabrication of Ge nanowire FETs. As shown in Fig. 6, we find that the thickness of the channel film of the Ge nanowire FET dominates the device's leakage current. Small diameter suppresses the leakage current of the Ge nanowire FET. The leakage current of the Ge omega-shaped-gate nanowire FET with the 70% gate coverage ratio and the 10 nm diameter is at the order of 10^{-12} A. The leakage current of the FET with the 20 nm diameter is at the order of 10^{-8} A. The variation of the leakage current, shown in Fig. 6, strongly depends on the thickness of the Ge channel film. For example, for the Ge nanowire FET with the 20 nm diameter, more than 3-order variation on the leakage current is found for the nanodevice with the gate channel length varying from 10 to 30 nm. For the case of the 10 nm diameter, the variation is within one order magnitude. It is expected that a smaller diameter of the Ge nanowire FET has a good channel controllability and suppresses the channel leakage current. Optimal structure of the Ge omega-shaped-gate FET should be subject to further investigation to obtain high performance nanodevices.

Figure 7 shows the drain current versus the drain voltage for both the Si and Ge nanowire FETs. It reports the Ge omega-shaped-gate FET with the 70% gate coverage ratio has a relatively improved characteristics of the on-state current compared with the results of the Si one. For example, under the same gate coverage ratio and device configuration, the drain current of the Ge omega-shaped-gate FET is about 2.5 times larger than that of the Si one. The results are performed by assuming a simple field effect dependent carrier mobility. From industrial application point of view, calibration of the mobility plays a crucial role for developing the omega-shaped-gate FETs. Particularly, when we would like to accommodate more diverse materials in nanodevices.

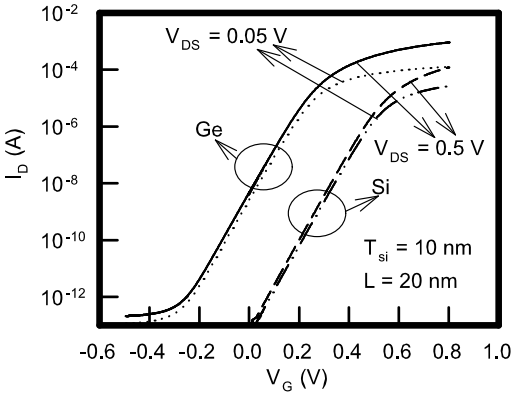

Fig. 5. A comparison of the transfer characteristics of the Si and Ge omega-shaped-gate FETs with the 70% gate coverage ratio. $L = 20nm$ and $T_{Si/Ge} = 10nm$.

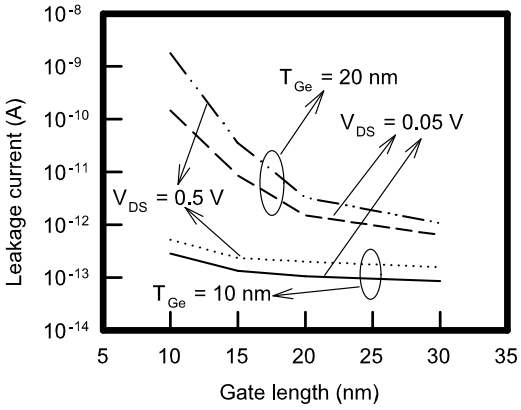

Fig. 6. A plot of the leakage current versus L for the Ge omega-shaped-gate FET with the 70% gate coverage ratio. Simulation is with $T_{Ge} = 10nm$ and $20nm$, and is with $V_{DS} = 0.5V$ and $0.05V$, respectively.

Scaling property of the studied nanodevice is explored by calculating the characteristics of the threshold voltage roll-off, shown in Fig. 8. The threshold voltage roll-off of the Ge omega-shaped-gate FET with the 70% gate coverage ratio and the 10 nm thickness of the channel film is similar to the result of the Si one. It is found that there is about 12% variation on the threshold voltage versus the gate channel length for both the Si and Ge nanowire FET. We further compare the leakage current versus the gate length for the Si and Ge omega-shaped-gate with the 70% gate coverage ratio. The 10 nm and 20 nm diameters of the nanowire FETs are calculated shown in Fig. 9. The leakage current of Si nanowire FET is lower than that of

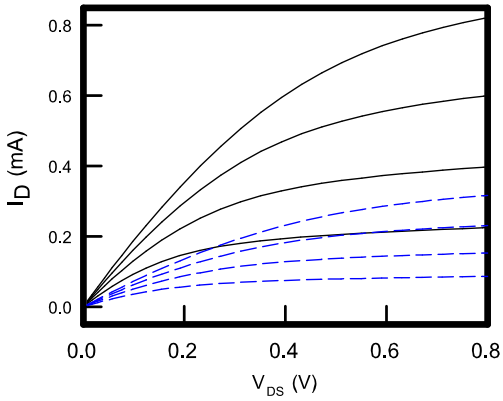

Fig. 7. The output characteristics of the Si (blue dashed lines) and Ge (solid lines) omega-shaped-gate FETs with the 70% gate coverage ratio. $V_{GS} - V_{th}$ varies from 0.2 V to 0.8 V (top line) with 0.2 V increment.

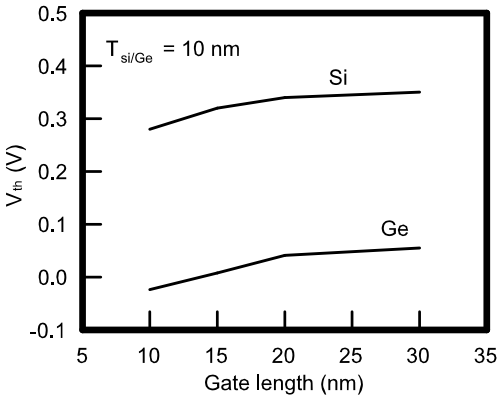

Fig. 8. The characteristics of threshold voltage roll-off for the 70% omega-shaped-gate Si and Ge nanowire FETs.

Ge one. However, the leakage current of the Ge nanowire FET is significantly reduced when the diameter is equal to 10 nm, due to the nature of the omega-shaped gate. This results also implies that reduction of the leakage current depends upon the channel material.

IV. Conclusions

In this work, electrical characteristics of Ge nanowire FETs have been explored with our own calibrated 3D density-gradient simulation prototype. For nanodevice with a 70% gate coverage ratio, results have shown that the Ge nanowire FET has potentially higher driving-capability than that of the Si one. It has implied a good channel controllability, compared with the Si nanowire FET. It has been found that the high mobility Ge nanowire FET will suppress the effect of band-gap narrowing on the transport characteristics. A thinner Ge channel film has resulted in a lower leakage current. We note that the 70%

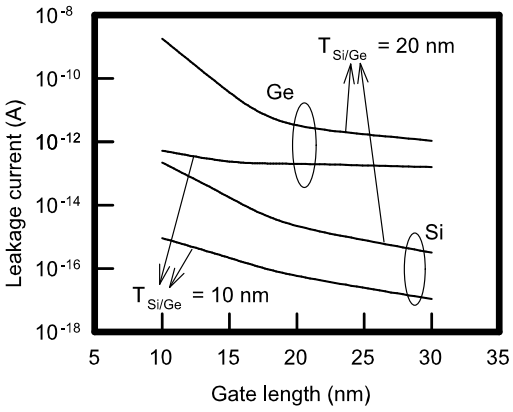

Fig. 9. The leakage current versus L for the Si and Ge nanowire FETs, where $T_{Si/Ge} = 10nm$ and $20nm$, and V_{DS} = 0.5 V.

coverage ratio has been directly adopted. However, the effect of gate coverage ratio should be subject to further investigation for more proper estimation on Ge nanowire FET. Full quantum mechanical modeling and simulation theoretically will provide us an insight into the fundamental physics of nanodevices and benefit more accurately quantitative estimation. Calibration between the simulation and measurement; in particular, the model formulation and parameter extraction of carrier mobility still plays a central role in the device application of semiconductor industry.

Acknowledgments

This work is supported in part by the National Science Council (NSC) of Taiwan under Contract NSC-93-2215-E-429-008 and Contract NSC-94-2752-E-009-003-PAE, by the Ministry of Economic Affairs, Taiwan under Contract 93-EC-17-A-07-S1-0011, and by the Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, under grants in 2004-2005.

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