Simulation of Drain Current Reduction Caused by Process-Induced Stress

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I. Introduction

As device dimensions are scaled down, the effects of process-induced stress on device characteristics are becoming significant. Scott et al. [1] reported that the stress caused by shallow trench isolation (STI) reduces drain current of NMOS and that MOS parameters can be affected by transistor layout. For accurate circuit simulation, transistor models like BSIM4 [2] have come to incorporate stress effects. The stress effects model used in BSIM4 was constructed using process and device simulation [3]. However, the simulation used was quite a simple one. Only the stress induced by STI was included and the stress from the deposited materials was ignored. In addition, only the stress at the channel center was used and the stress distribution along the channel was ignored. In this work, the necessity of more precise treatment is examined.

II. Simulation

A. Stress Calculation

We simulated process-induced stress using a three-dimensional process simulator, HySyProS [4]. An example of the simulated structures is shown in Fig. 1. Stress generated in sacrificial and gate oxidation is calculated using the viscoelastic oxidation model and the numerical solution method is given elsewhere [5]. Stress dependence of oxide viscosity, crystallographic anisotropy of elastic coefficients of silicon and orientation dependence of surface reaction constant of oxidant are incorporated in oxidation simulation. However, stress dependence of the surface reaction constant and oxidant diffusivity is not included in the present calculation.

In addition to the oxidation-induced stress, the stress from the deposited materials is included. The values of the intrinsic stresses in the deposited materials are listed in Table I. Typical values measured at room temperature are used in the present calculations.

Since model-parameter calibration was not performed prior to the present calculation, the calculated stress values are only rough estimates.

B. Drain Current Calculation

The stress distribution obtained by HySyProS was given to a HyDeLEOS device simulator and the drain current of NMOS was simulated.

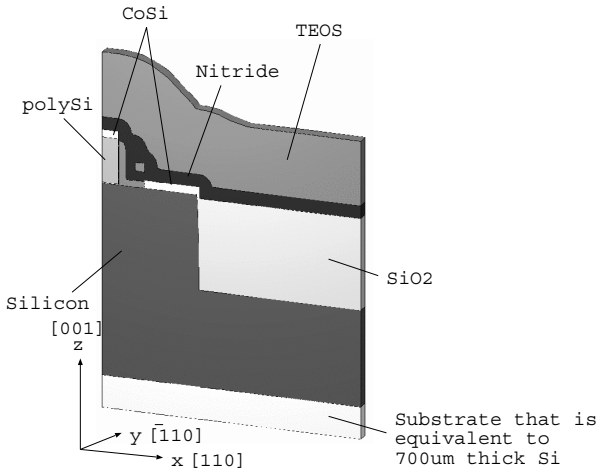

Fig. 1. Simulated structure. Crystallographic anisotropy of silicon is incorporated. A substrate with stiffness equivalent to that of Si substrate having a thickness of 700 μm is attached at the bottom of the structure according to Saito et al. [6] and expansion along x and y axes is allowed.

TABLE I
Typical values of intrinsic stresses in deposited materials

Material	Stress [dynes/cm^2]
poly Si	$\sim 5 \times 10^9$ (tensile)
nitride	$\sim 1 \times 10^{10}$ (tensile)
CoSi	$\sim 1 \times 10^{10}$ (tensile)
TEOS	$\sim 5 \times 10^8$ (tensile)

The stress-dependent electron mobility μ_n is calculated as

$$\mu_n = \begin{cases} \mu_n^{high} \cdot f_{stress}^n & \text{(model 1)} \\ \mu_n^{high} & \text{(model 2)} \end{cases} \quad (1)$$

$$\mu_n^{high} = \frac{\mu_n^{low'}}{\sqrt{1 + \frac{\left(\mu_n^{low'} E/V_c\right)^2}{\left(\mu_n^{low'} E/V_c\right)+G} + \left(\mu_n^{low'} E/V_c\right)^2}} \quad (2)$$

$$\mu_n^{low'} = \begin{cases} \mu_n^{low} & \text{(model 1)} \\ \mu_n^{low} \cdot f_{stress}^n & \text{(model 2)} \end{cases}. \quad (3)$$

where μ_n^{high} is high field mobility and calculated from low field mobility $\mu_n^{low'}$ using eq. (2) [7]. E is horizontal field, V_c and G are model parameters. μ_n^{low} is low field mobility without

TABLE II

PARAMETERS OF STRESS-DEPENDENT MOBILITY MODEL.

Ξ_d [eV]	Ξ_u [eV]	m_l/m_t
-8.6	9.5	5.158

stress effect. μ_n^{low} arises from phonon, Coulomb and surface-roughness scattering and includes the effect of the vertical field.

f_{stress}^n is a stress-dependent factor and calculated as

$$f_{stress}^n = \frac{\sum_{i=1}^{3} c_i \exp\left(-\frac{\delta E_c^{(i)}}{kT}\right)}{\sum_{i=1}^{3} \exp\left(-\frac{\delta E_c^{(i)}}{kT}\right)} \quad (4)$$

$$c_1 = \frac{3}{1+2m_l/m_t}\cos^2\phi + \frac{3m_l/m_t}{1+2m_l/m_t}\sin^2\phi \quad (5)$$

$$c_2 = \frac{3m_l/m_t}{1+2m_l/m_t}\cos^2\phi + \frac{3}{1+2m_l/m_t}\sin^2\phi \quad (6)$$

$$c_3 = \frac{3m_l/m_t}{1+2m_l/m_t} \quad (7)$$

where $\delta E_c^{(i)}$ is the shift of the conduction band minimum due to strain. The superscript i denotes the i-th pair of ellipsoids of the conduction band. k is the Boltzmann constant and T is the temperature. m_l and m_t are longitudinal and transverse effective mass of the electrons, respectively. ϕ is the angle between current flow and [100] axis. $\delta E_c^{(i)}$ is calculated from strain as,

$$\delta E_c^{(i)} = \Xi_t(\varepsilon_{11}+\varepsilon_{22}+\varepsilon_{33}) + \Xi_u\varepsilon_{ii} \quad (8)$$

where ε_{ij} $(i,j=1,2,3)$ is strain in the crystal-axis coordinate system.

The eqs. (1)-(8) are obtained by simplifying Egley's model [8], which was proposed for bulk mobility. In the simplification, the gradient of quasi-Fermi level was assumed to be parallel to current flow and Boltzmann distribution was used. The values of the parameters used are listed in Table II. In the present model, f_{stress}^n does not depend on dopant concentration.

C. Dopant Distribution

In the previous work of our group [9], we measured the layout dependence of mobility using the charge-based capacitance measurement(CBCM) technique. In the experiments, MOS devices were fabricated using 130 nm technology. The process flow of those devices was simulated in this work. A point-defect-based diffusion model was used to solve dopant diffusion. However, the number of initial point defects, which are introduced by implantation, was set to be zero in these calculations. This is because recombination at the side of STI is too fast using HySyProS point-defect parameters, and this causes unexpected layout dependence of the dopant profile. For simplicity, the number of implantation-induced defects was set to be zero in the present calculation and V_{th} roll-off curve was fitted by adjusting the doses of channel and halo implants.

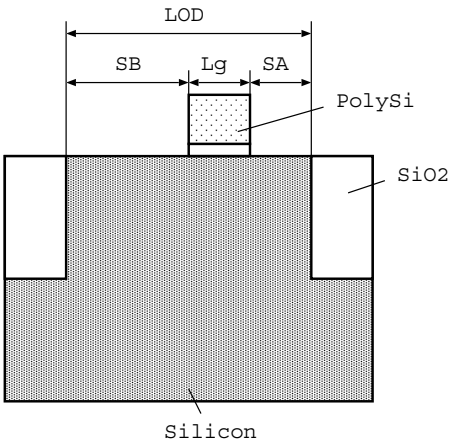

Fig. 2. Parameters for transistor layout definition

III. RESULTS AND DISCUSSION

A. LOD and SA dependences

We simulated the layout dependence of the drain current of NMOS. The parameters that define transistor layout are given in Fig. 2. LOD is the length of thin oxide definition area (OD). SA and SB are the distances from each edge of OD to gate poly Si. L_g is the gate length.

The simulated LOD dependence of the drain current I_{ds} is shown in Fig. 3. Circles represent the results that are obtained when only oxidation is included. Triangles correspond to the results when the stress from poly Si is added. The results show that the stress from poly Si slightly reduces the LOD dependence by modulating strain distribution around the gate as shown in Figs. 4 and 5, however, the change in LOD dependence is small. Furthermore, when the stress from all deposited materials listed in Table I is considered (crosses in Fig. 3), the effects of the deposited materials become negligible. This means that the treatment by Su et al. [3] is acceptable. The simulated SA dependence of the drain current I_{ds} is shown in Fig. 6. This also shows that the effect of deposited poly Si is small.

Since the stress-dependent diffusion model [10] was not used in the present calculation, threshold voltage was almost constant for LOD variation in all calculations.

B. Lg dependence

The gate-length dependence of the drain current reduction was simulated and the results are shown in Fig. 7. Although the stress from poly Si reduces the magnitude of the drain current reduction for short channel devices, it is not sufficient to reproduce the strong reduction that was experimentally observed by Su et al. [3] (Fig. 8).

It has been reported by experiments adopting the four-point bending technique that effective piezoresistive coefficient is reduced for short channel devices due to parasitic resistance [11], [12], and the effect of this parasitic resistance was simulated. The results are shown in Fig. 9 and it can be seen that the effect is very small in the present calculation.

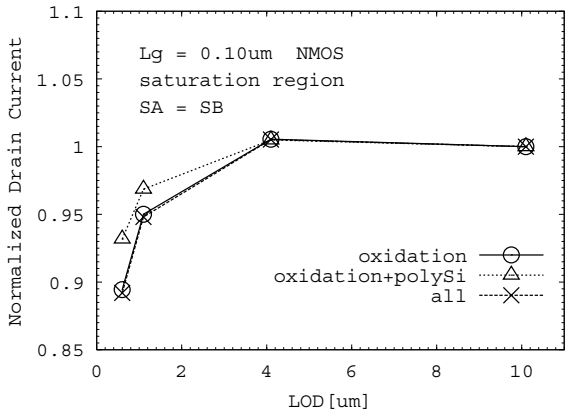

Fig. 3. Simulated LOD dependence of drain current. Drain current is normalized to a value of LOD=10.1μm. Model 1 in eqs. (1) and (3) is used. The stress from poly Si slightly reduces the LOD dependence, however, its effect is small. When the stress from all deposited materials listed in Table I is considered, the effects of the deposited materials become negligible.

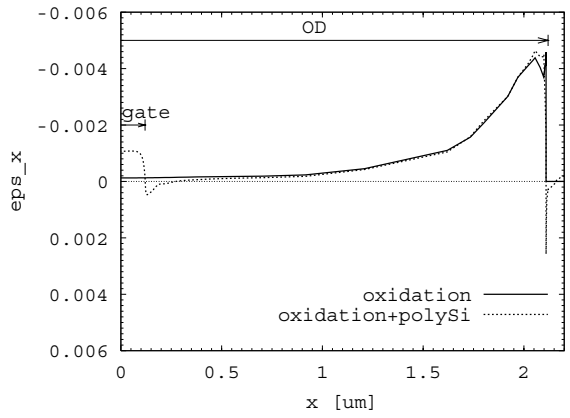

Fig. 4. Distribution of strain component ε_x at silicon surface.

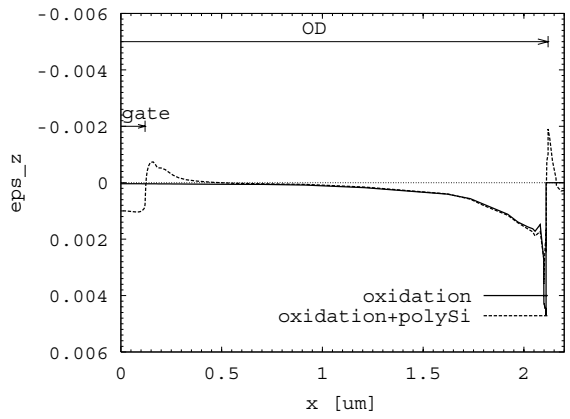

Fig. 5. Distribution of strain component ε_z at silicon surface.

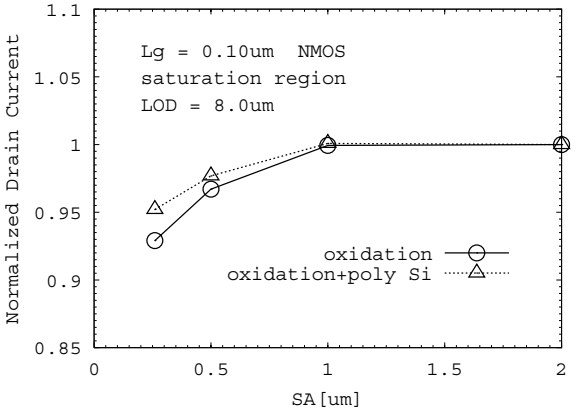

Fig. 6. Simulated SA dependence of drain current. SA is the distance on the drain side. Drain current is normalized to a value of SA=2.0μm. Model 1 in eqs. (1) and (3) is used. The stress from deposited poly Si slightly reduces the SA dependence, however, its effect is small.

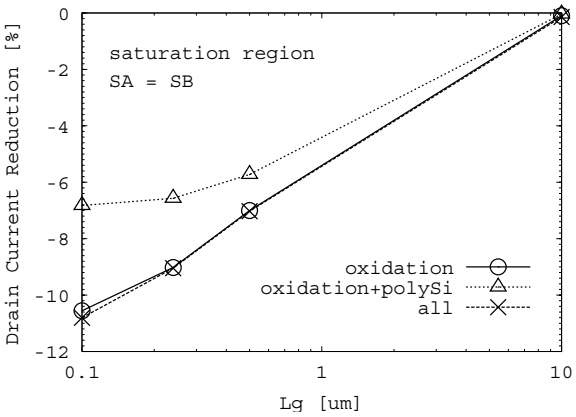

Fig. 7. Simulated L_g dependence of drain current reduction. Drain current reduction is defined as $[I_{ds}(SA = 0.25\mu m) - I_{ds}(SA = 5.0\mu m)]/I_{ds}(SA = 5.0\mu m)$. Model 1 in eqs. (1) and (3) is used.

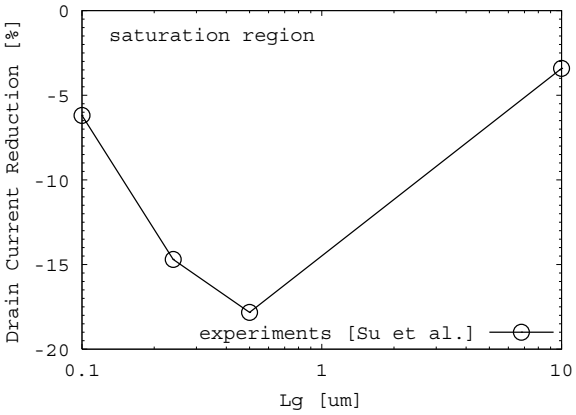

Fig. 8. Experimentally obtained L_g dependence of drain current reduction reported by Su et al. [3].

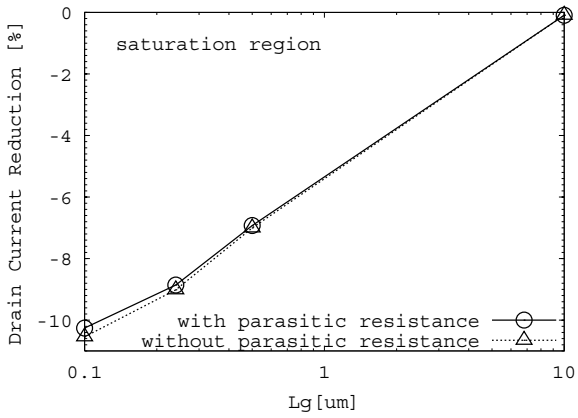

Fig. 9. Effects of parasitic resistance. Model 1 in eqs. (1) and (3) is used.

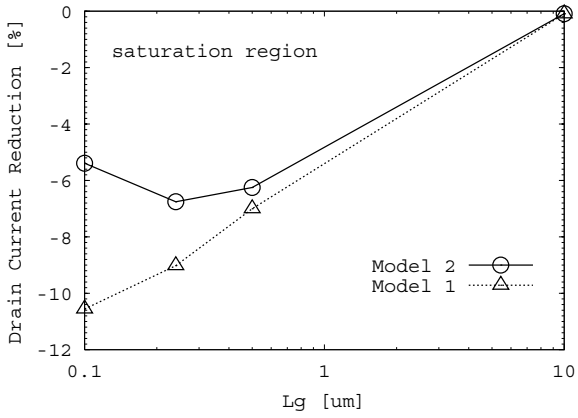

Fig. 10. Effects of horizontal field(saturation region).

It is also reported that the stress dependence of the mobility is reduced when the electric field in the direction of current flow is large [13], [14]. In order to incorporate this effect, the stress-dependent factor f^n_{stress} was multiplied by low field mobility μ^{low}_n [model 2 in eq. (3)] instead of high field mobility μ_{high} [model 1 in eq. (1)] as it is done in a commercial simulator. The results are shown in Figs. 10 and 11. Although model 2 creates a local minimum around $L_g = 0.2\,\mu$m in the results of the saturation region(Fig. 10), its effect is very small in the linear region(Fig. 11). Since a local minimum is experimentally observed in the linear region, model 2 is still not sufficient.

The discrepancy is inferred to arise from the incompleteness of the model used. It is known that the piezoresistive coefficient depends on dopant concentration [15]. Monte Carlo simulation also shows that the stress-effect on inversion layer mobility is reduced at high doping concentrations [16]. In addition, it has been pointed out that high-dose halo implants reduce stress effects on mobility [17]. However, the stress-dependent mobility model used in this study doesn't include dopant-concentration dependence. Improvement of the stress-dependent mobility model may be necessary.

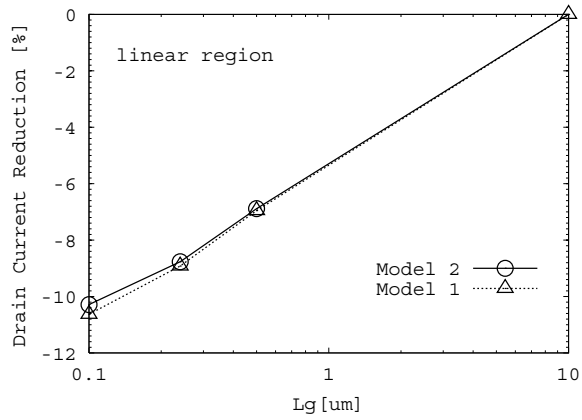

Fig. 11. Effects of horizontal field(linear region).

IV. Conclusion

Layout dependence of the drain current of NMOS is simulated. The results show that the stress from deposited materials can be neglected when simulating LOD and SA dependence. However, another mechanism has to be included to simulate the gate-length dependence of drain current reduction correctly.

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