

Applications of Three-Dimensional Topography Simulation in the Design of Interconnect Lines

A. Sheikholeslami[◦], F. Parhami[†], R. Heinzl^{*}, E. Al-Ani[◦], C. Heitzinger[◦], F. Badrieh[†],
H. Puchner[†], T. Grasser^{*}, and S. Selberherr[◦]

[◦] Institute for Microelectronics, TU Vienna, Gußhausstraße 27–29/E360, 1040 Wien, Austria
Phone: +43-1-58801/36034, Fax: +43-1-58801/36099, E-mail: sheikholeslami@iue.tuwien.ac.at

[†] Cypress Semiconductor, San Jose, CA 95134, USA

^{*} Christian Doppler Laboratory for TCAD in Microelectronics at the Institute for Microelectronics

Abstract— We present an analysis of deposition of silicon nitride and silicon dioxide layers into three-dimensional interconnect structures. The investigations have been performed using our general purpose topography simulator ELSA (Enhanced Level Set Applications). We predict void formation and its characteristics, which play an important role for the formation of cracks which are observed during the passivation of layers covering IC chips.

I. INTRODUCTION

Cracks are observed in the passivation layers that cover IC chips in the areas where top metalization layout geometry yields a three dimensional profile for passivation deposition. To avoid such cracking and the subsequent device failure, it is essential to characterize the passivation deposition profile as a function of layout geometry. This characterization can then be used to establish a set of layout design rules to mitigate crack formation. An easy and fast approach is the use of deposition simulation tools.

Our two-dimensional investigations have predicted very well the void profile for the calculation of capacitance contributing in RC timing delays stemming from metal lines in interconnect structures [1]. The parameters for calibration and optimization of simulation results with measurements were extracted by SIESTA (Simulation Environment for Semiconductor technology Analysis) [2].

However, for the prediction of cracking effects two-dimensional void characteristics are not sufficient and the three-dimensional behavior of voids must be considered. Therefore, having a general purpose topography simulator in three dimensions capable of handling different physical etching and deposition models is essential. For this purpose, we have developed a very fast general purpose topography simulator ELSA in three dimensions [3]. The topography simulator is based on the level set method [4] which is the best technique to track moving boundaries.

The outline of this paper is as follows. First, we describe briefly the level set method and related techniques for obtaining an accurate and fast topography simulator. Second, we explain the deposition processes which are relevant for our industrial applications. Finally, we present the simulation results.

II. THE LEVEL SET METHOD

The level set method [4] provides means for describing boundaries, i.e., curves, surfaces or hypersurfaces in arbitrary dimensions and their evolution in time which is caused by forces or fluxes normal to the surface. The basic idea is to view the curve or surface in question at a certain time t as the zero level set (with respect to the space variables) of a certain function $\varphi(t, \mathbf{x})$, the so called level set function. Thus the initial surface is the set $\{\mathbf{x} \mid \varphi(0, \mathbf{x}) = 0\}$.

Each point on the surface is moved with a certain speed normal to the surface and this determines the time evolution of the surface. The speed normal to the surface will be denoted by $F(t, \mathbf{x})$. For points on the zero level set $F(t, \mathbf{x})$ is usually determined by physical models and in our case by the etching and deposition processes, or more precisely by the fluxes of certain gas species and subsequent surface reactions. The speed function $F(t, \mathbf{x})$ generally depends on the space variables and time.

The surface at a later time t_1 shall also be considered as the zero level set of the function $\varphi(t, \mathbf{x})$, namely $\{\mathbf{x} \mid \varphi(t_1, \mathbf{x}) = 0\}$. As shown in [4], this leads to the level set equation

$$\varphi_t + F(t, \mathbf{x}) \|\nabla_{\mathbf{x}} \varphi\| = 0, \quad \varphi(0, \mathbf{x}) \text{ given,}$$

in the unknown variable φ , where $\varphi(0, \mathbf{x})$ determines the initial surface. Having solved this equation the zero level set of the solution is the sought curve or surface at all later times.

After calculation of the initial level set function, the speed function values on the whole grid are used to update the level set function in a finite difference or finite element scheme. Usually the values of the speed function are not determined on the whole domain by the physical models and, therefore, have to be extrapolated suitably from the values provided on the boundary, i.e., the zero level set. This can be carried out iteratively by starting from the points nearest to the surface.

The idea leading to fast level set algorithms stems from observing that only the values of the level set function near its zero level set are essential, and thus only the values at the grid points in a narrow band around the zero level set have to be calculated. Both improvements, extension of the speed function and narrow banding, require the construction of the distance function from the zero level set in the order of increasing distance. But calculation of the exact distance

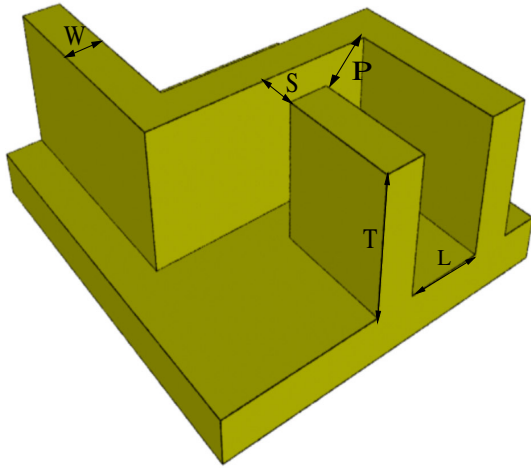


Figure 1: Schematic of the investigated three-dimensional structure.

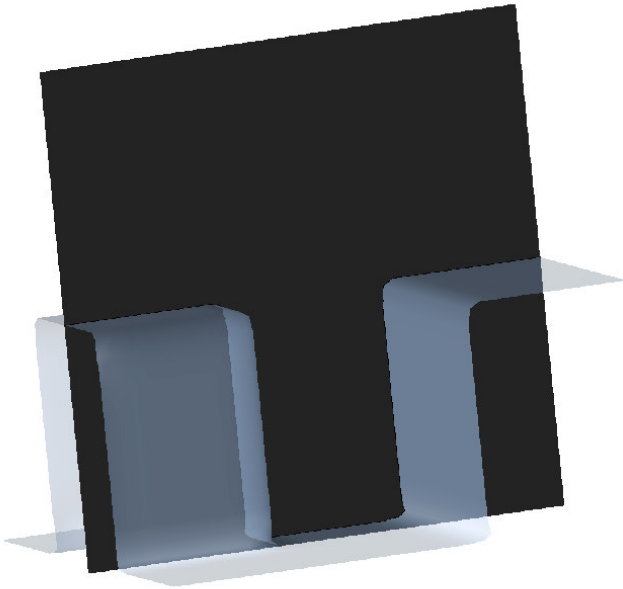


Figure 2: Initial structure for $T = 1.045\mu\text{m}$ and $S = 0.72\mu\text{m}$.

function from a surface consisting of a large number of small triangles is computationally expensive and can be only justified for the initialization. An approximation to the distance function is computed by a special fast marching method [4, 5].

III. DEPOSITED LAYERS

In the processes considered the transport of particles happens in the radiosity regime [4]. The deposition processes are governed by luminescent reflection. The films deposited are silicon nitride and silicon dioxide films.

The silicon nitride films were deposited by PECVD from silane and NH_3 and were not doped. The reaction is $\text{SiH}_4 + \text{NH}_3 \rightarrow \text{SiNH} + 3\text{H}_2$ [6]. For simulation purposes this was considered the essential reaction.

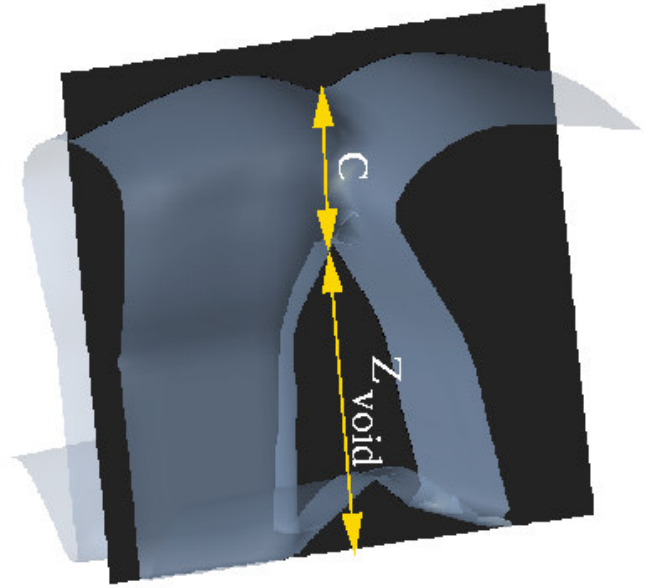


Figure 3: Void formation during the deposition into the initial structure shown in Figure 2.

The silicon dioxide films were deposited by pyrolytic decomposition of TEOS in an LPCVD process [7]. In order to calculate the thickness Δd of the film deposited during a time interval of length Δt , we observe that Δd is proportional to Δt , to an Arrhenius term, and to the deposition rate R corresponding to the deposition model chosen. This implies $\Delta d = R \cdot \Delta t \cdot k_e \exp(-E/kT)$. Here $k_e \exp(-E/kT)$ is Arrhenius term with activation energy E , absolute temperature T , and pre-exponential constant k_e [8].

When modeling topography processes it is generally possible to write down quite complicated reaction paths. However, it is not straightforward to determine the vital reactions and their coefficients. Therefore it is mandatory to reduce the possible reaction paths to an essential minimum which reproduces the observed phenomena.

For three-dimensional deposition simulation we have used the same parameters which were extracted with SIESTA for two-dimensional simulations [1]. These parameters led to very good agreement of simulation results with measurements.

IV. THREE-DIMENSIONAL SIMULATION RESULTS

Figure 1 shows a schematic of the three-dimensional structure used in our investigations. The geometrical parameters for which we obtain the void characteristics are the line-to-line spacing (S), the metal thickness (T), the metal width (W), the displacement parameter (L), and a diagonal parameter (P). The last two parameters demonstrate the real three-dimensional effects.

Since our simulations have shown [3] that the metal width does not play an important role for void characteristics, it will be held constant during all investigations. The first set of

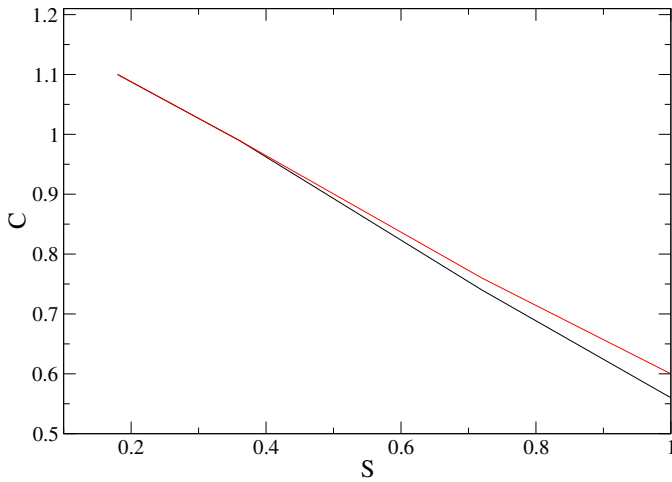


Figure 4: Dependence of C on S for T_1 and T_2 . The lower and upper curve stands for T_1 and T_2 , respectively.

simulations was performed for different line-to-line spacing holding the metal thickness at $T_1 = 0.845\mu\text{m}$ and $T_2 = 1.045\mu\text{m}$. As mentioned in Section III the deposited layers were silicon dioxide and silicon nitride with a thickness of $D_1 = 0.1\mu\text{m}$ and $D_2 = 0.9\mu\text{m}$, respectively.

For analyzing cracking effects we introduce C which is calculated as follows:

$$C(S, T, D, L, P) = T + D - Z_{\text{void}}(S, T, D, L, P)$$

where Z_{void} (the Z coordinate of top of the void) and C are shown in Figure 3 which illustrates the simulation result for the initial structure shown in Figure 2.

In order to investigate how C depends on the line-to-line spacing and the metal thickness, we have performed simulations at $S = 0.18, 0.36, 0.72$, and $1\mu\text{m}$, for T_1 and T_2 . The results of this set of simulations is indicated in Figure 4.

To see the void formation more clearly, two-dimensional cuts in the YZ plane are given. Figure 5 and Figure 6 show the void formation for $S = 1\mu\text{m}$ at T_1 and T_2 , respectively, and indicate which role the metal thickness T can play during void formation. Comparing these two figures shows that increasing the metal thickness leads to increasing void dimensions and whereas for small line-to-line spacing the metal thickness does not play an important role, its effect as shown in Figure 4 becomes more important with increasing S , i.e., the thicker the metal the larger C .

Furthermore, the simulations have shown that the voids are shifted upwards as the line-to-line spacing is increased. This can be clearly seen by comparing Figure 3 with Figure 6.

All above simulations have been performed in three dimensions. However, approximately the same result could have been obtained with two-dimensional simulations. In the following we will discuss results which cannot be obtained using only two-dimensional simulations. First we begin with a variation of L , where the other parameters are held constant. The simulation results have shown that increasing L like increasing

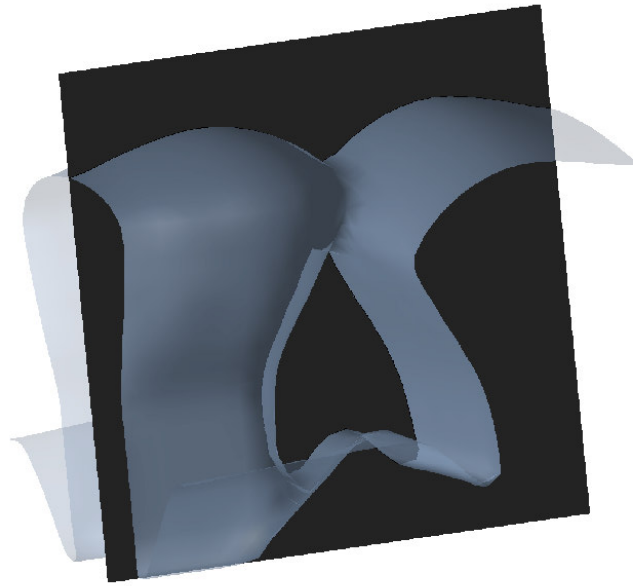


Figure 5: Deposition simulation for $S = 1\mu\text{m}$ at T_1 .

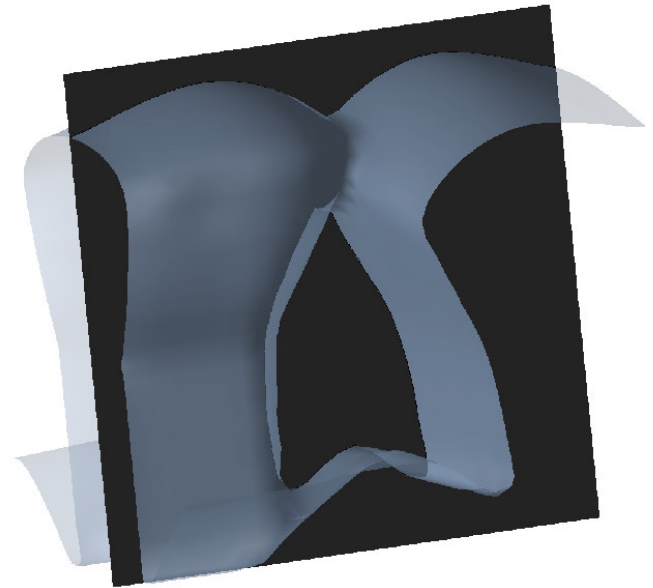


Figure 6: Deposition simulation for $S = 1\mu\text{m}$ at T_2 .

S shifts the voids upwards, although the shape of the voids does not change compared to the case when S is increased.

The most important result has been obtained with simultaneous variation of S and L . Note that P is implicitly given for a chosen pair S and L . Figure 7, Figure 8, and Figure 9 show three from many investigations for different S and L . These investigations have led to a profile of C as shown in Figure 10. The profile predicts C , and the smaller C the more

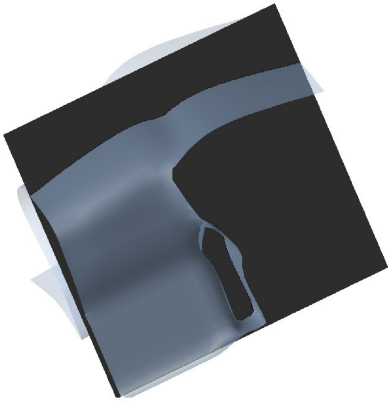


Figure 7: Void formation for T_1 and $S = L = 0.3\mu\text{m}$.

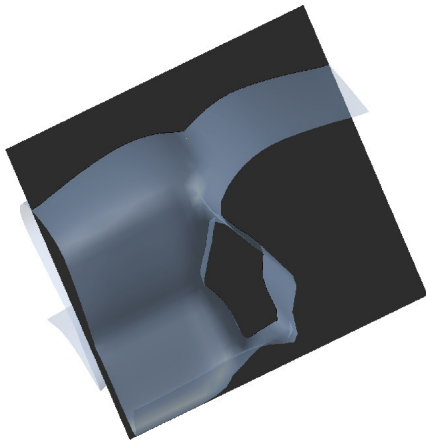


Figure 8: Void formation for T_1 and $S = L = 0.6\mu\text{m}$.

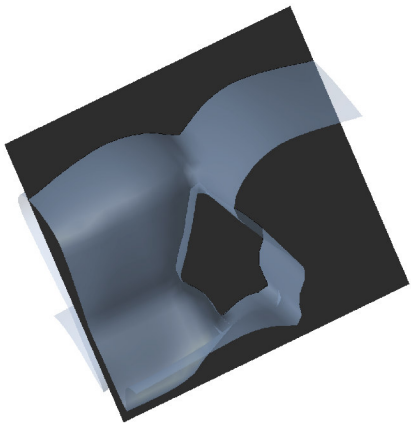


Figure 9: Void formation for T_1 and $S = L = 0.9\mu\text{m}$.

probable cracking effects will occur. Therefore, this profile enables process engineers to choose the optimal geometrical parameters to avoid cracks.

V. CONCLUSION

State of the art algorithms for surface evolution processes like deposition and etching processes in three dimensions have

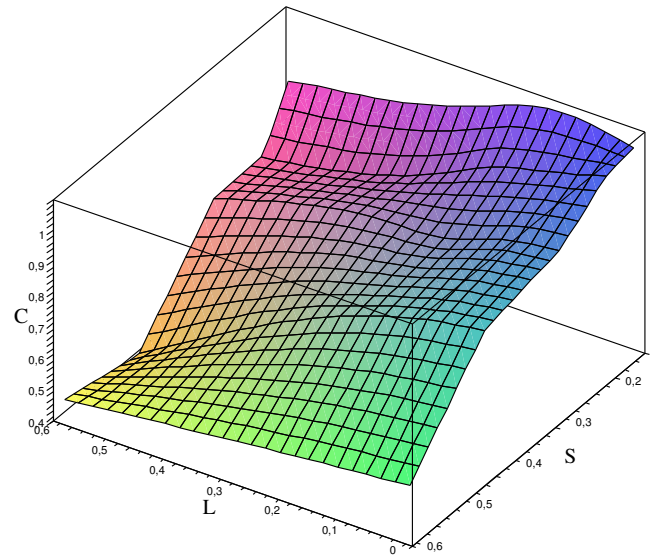


Figure 10: Three-dimensional profile of C depending on S and L .

been implemented. A general purpose topography simulator was developed based on the level set method combining narrow banding and fast marching methods for higher efficiency. The application has been presented for three-dimensional interconnect processes. A set of three-dimensional investigations for different geometrical parameters has been performed and presented. How different geometrical parameters affect void characteristics and subsequently C has been presented. We can predict when cracking effects happen, since C determines how close is the top of void to the top of flat deposited layer, and the smaller C the more probable cracking effects will occur.

ACKNOWLEDGEMENT

The authors acknowledge the support from M. Spevak.

REFERENCES

- [1] C. Heitzinger *et al.*, IEEE Trans.Electron Devices **51**, p.1129 (2004).
- [2] S. Holzer *et al.*, in *Symposium on Nano Device Technology* (Hsinchu,Taiwan, 2004), pp. 113–116.
- [3] A. Sheikholeslami *et al.*, in *International Conference on Ultimate Integration of Silicon* (IEEE, Bologna, Italy, 2005), pp. 139–142.
- [4] J. Sethian, *Level Set Methods and Fast Marching Methods* (Cambridge University Press, Cambridge, 1999).
- [5] A. Sheikholeslami, C. Heitzinger, T. Grasser, and S. Selberherr, in *Proc. 24th International Conference on Microelectronics (MIEL)* (IEEE, Nis, Serbia and Montenegro, 2004), pp. 241–244.
- [6] G. Schumicki and P. Seegebrecht, *Prozess-technologie* (Springer, 1991).
- [7] D. Smith *et al.*, J.Electrochem.Soc. **137**, p.614 (1990).
- [8] G. Raupp, F. Shemansky, and T. Cale, J.Vac.Sci.Technol.B **10**, p.2422 (1992).